

# PSMN3R5-80ES

N-channel 80 V, 3.5 mΩ standard level MOSFET in I2PAK

Rev. 02 — 19 April 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in I2PAK package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switch
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

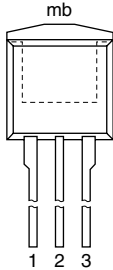
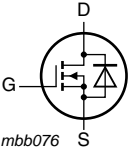
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	80	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	<a href="#">[1]</a>	-	120	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	338	W
T <sub>j</sub>	junction temperature		-55	-	175	°C
Static characteristics						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 100 °C; see <a href="#">Figure 12</a>	-	5	5.8	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>	<a href="#">[2]</a>	-	3	3.5
Dynamic characteristics						
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 75 A;	-	27	-	nC
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 40 V; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	139	-	nC
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 80 V; R <sub>GS</sub> = 50 Ω; unclamped	-	-	676	mJ



- [1] Continuous current is limited by package.
- [2] Measured 3 mm from package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	drain		

SOT226 (I2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R5-80ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

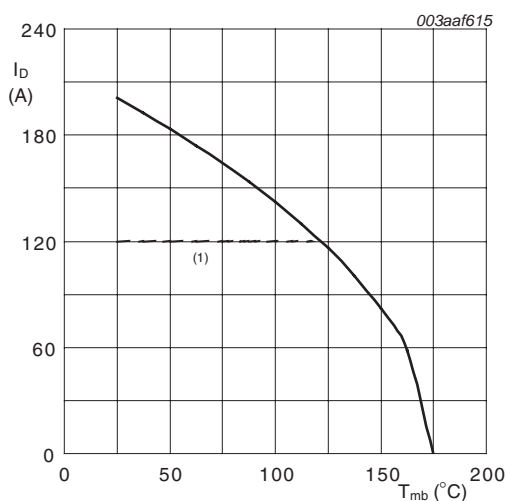
## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

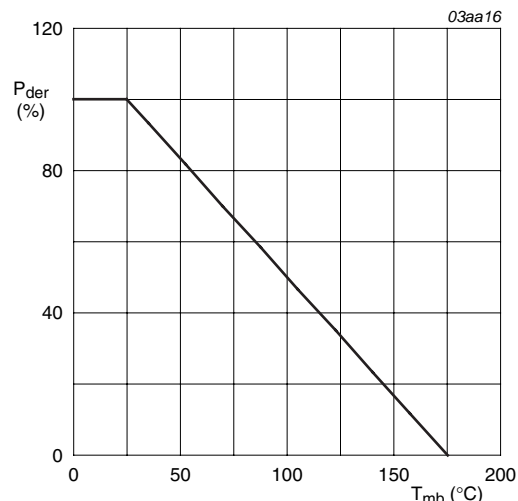
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	120	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	120	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	803	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	338	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[1]	120	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	803	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 120\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	676	mJ

[1] Continuous current is limited by package.



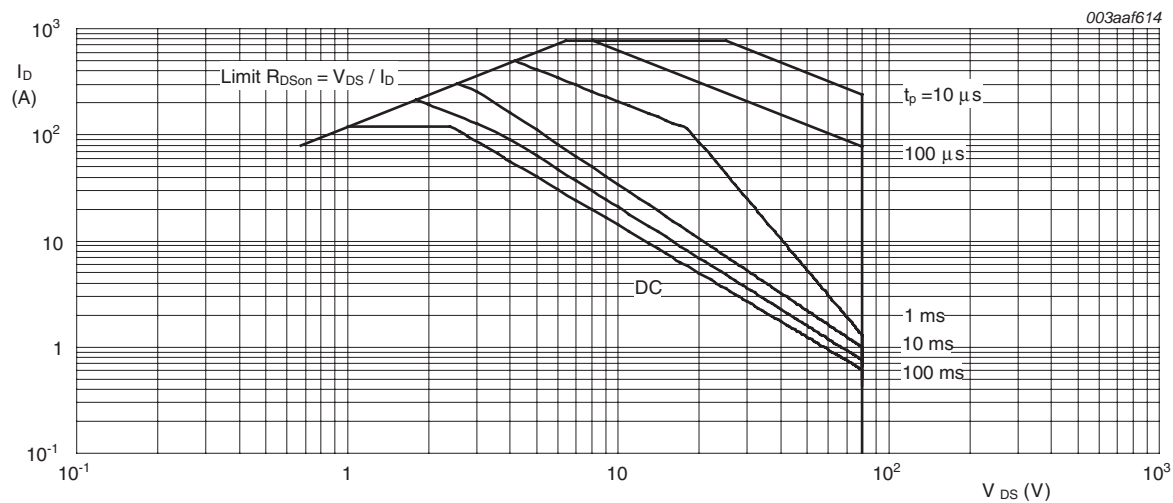
$V_{GS} \geq 10\text{ V}$ ; (1) capped at 120 A due to package.

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



$T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{DM}$  is a single pulse; Capped at 120 A due to package

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.22	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Vertical in free air	-	60	-	K/W

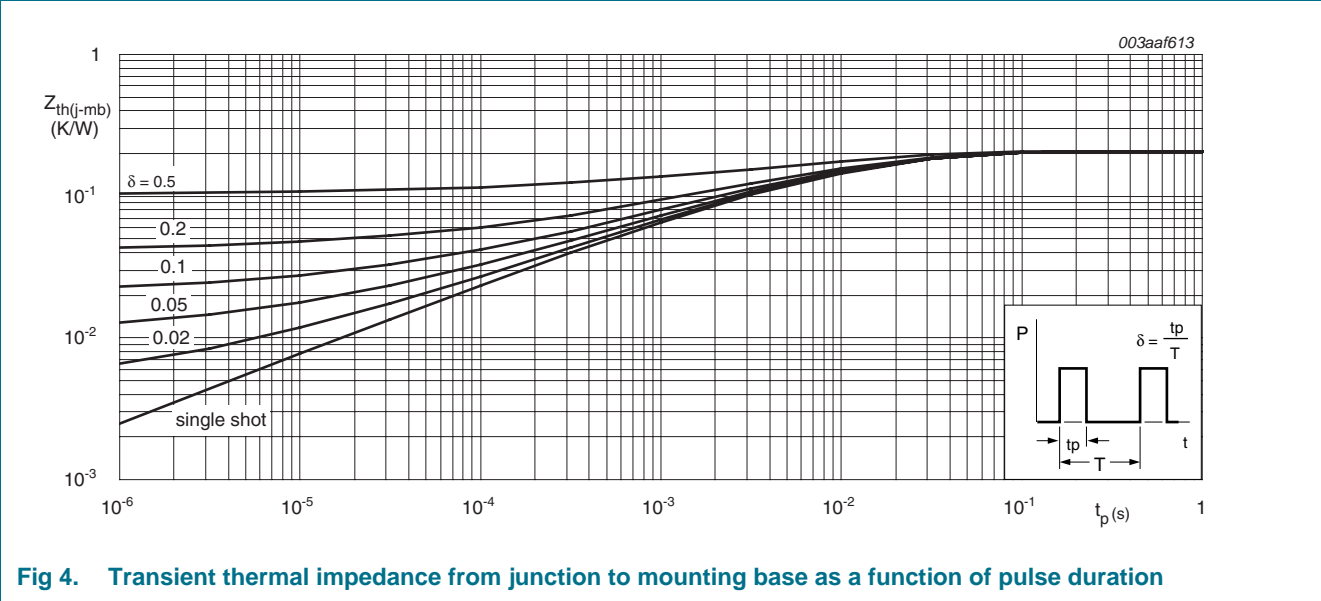


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = -55\ ^\circ\text{C}$	73	-	-	V
		$I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 175\ ^\circ\text{C}$ ; see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55\ ^\circ\text{C}$ ; see <a href="#">Figure 10</a>	-	-	4.6	V
		$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\ ^\circ\text{C}$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$	-	0.02	10	$\mu\text{A}$
		$V_{DS} = 80\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = 175\ ^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20\ \text{V}$ ; $V_{DS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{GS} = 20\ \text{V}$ ; $V_{DS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$ ; $I_D = 25\ \text{A}$ ; $T_j = 175\ ^\circ\text{C}$ ; see <a href="#">Figure 12</a>	-	7.2	8.4	mΩ
		$V_{GS} = 10\ \text{V}$ ; $I_D = 25\ \text{A}$ ; $T_j = 100\ ^\circ\text{C}$ ; see <a href="#">Figure 12</a>	-	5	5.8	mΩ
		$V_{GS} = 10\ \text{V}$ ; $I_D = 25\ \text{A}$ ; $T_j = 25\ ^\circ\text{C}$ ; see <a href="#">Figure 13</a>	<a href="#">[1]</a> -	3	3.5	mΩ
$R_G$	internal gate resistance (AC)	$f = 1\ \text{MHz}$	-	0.9	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 0\ \text{A}$ ; $V_{DS} = 0\ \text{V}$ ; $V_{GS} = 10\ \text{V}$	-	135	-	nC
		$I_D = 75\ \text{A}$ ; $V_{DS} = 40\ \text{V}$ ; $V_{GS} = 10\ \text{V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	139	-	nC
$Q_{GS}$	gate-source charge		-	51	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	30	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	21	-	nC
$Q_{GD}$	gate-drain charge		-	27	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\ \text{A}$ ; $V_{DS} = 40\ \text{V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	5.8	-	V
$C_{iss}$	input capacitance	$V_{DS} = 40\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ ; $f = 1\ \text{MHz}$ ; $T_j = 25\ ^\circ\text{C}$ ; see <a href="#">Figure 16</a>	-	9961	-	pF
$C_{oss}$	output capacitance		-	847	-	pF
$C_{rss}$	reverse transfer capacitance		-	401	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40\ \text{V}$ ; $R_L = 0.53\ \Omega$ ;	-	41	-	ns
$t_r$	rise time	$V_{GS} = 10\ \text{V}$ ; $R_{G(ext)} = 10\ \Omega$ ; $I_D = 75\ \text{A}$	-	43	-	ns
$t_{d(off)}$	turn-off delay time		-	109	-	ns
$t_f$	fall time		-	44	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_J = 25\text{ °C}$ ; see Figure 17	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $dI_S/dt = 100\text{ A/}\mu\text{s}$ ;	-	63	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$	-	121	-	nC

[1] Measured 3 mm from package.

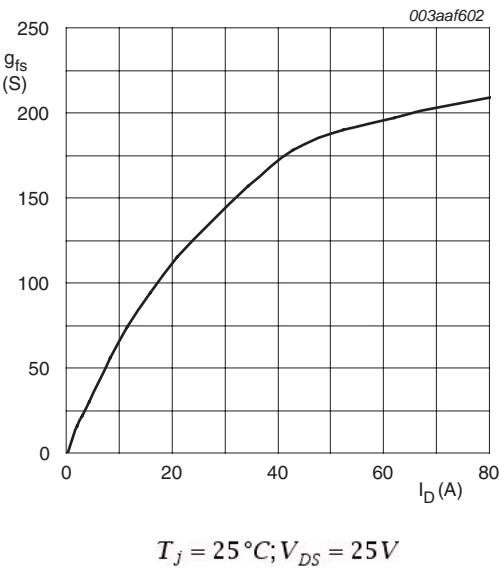


Fig 5. Forward transconductance as a function of drain current; typical values

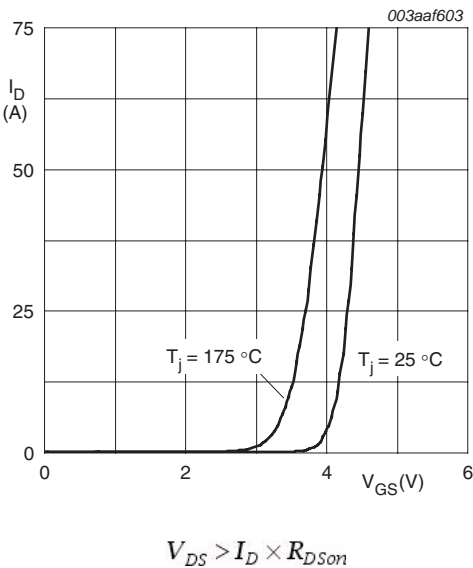


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

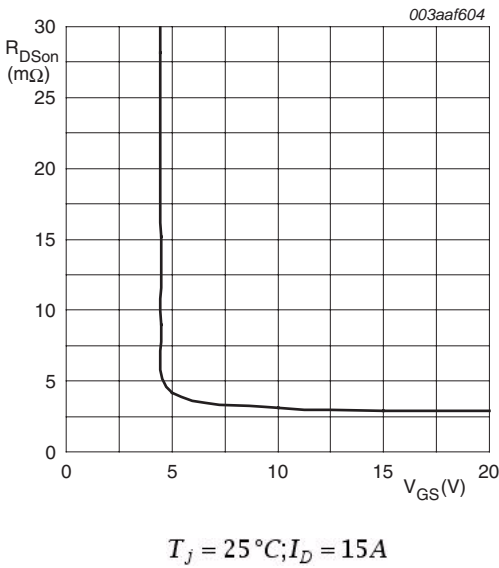


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

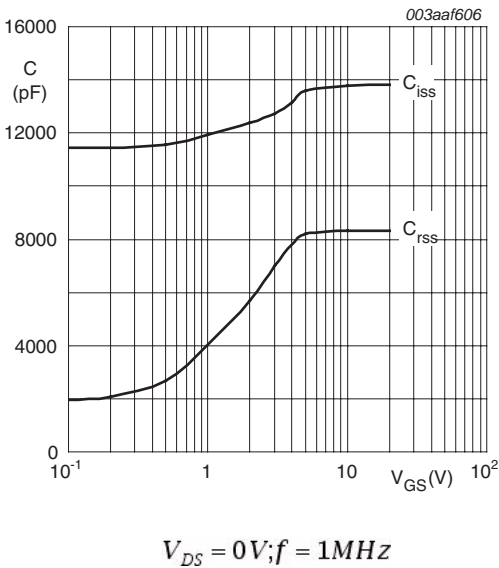
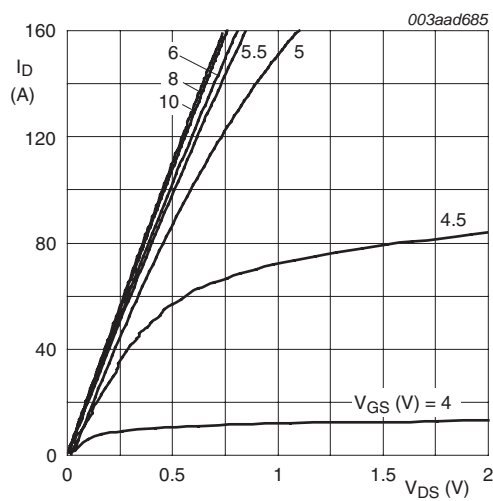
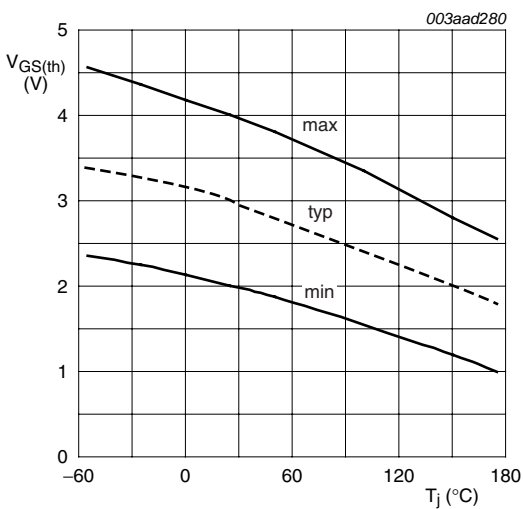


Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



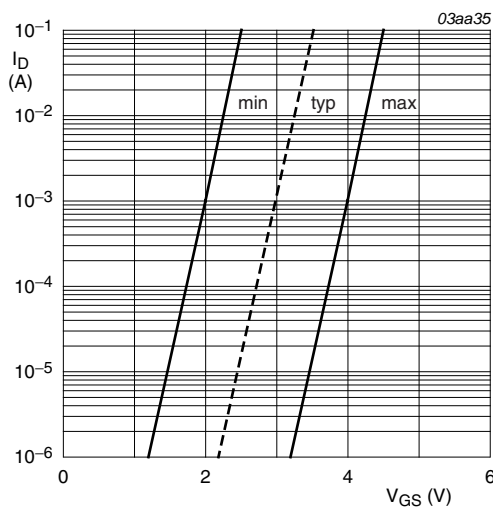
$T_j = 25\text{ }^{\circ}\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



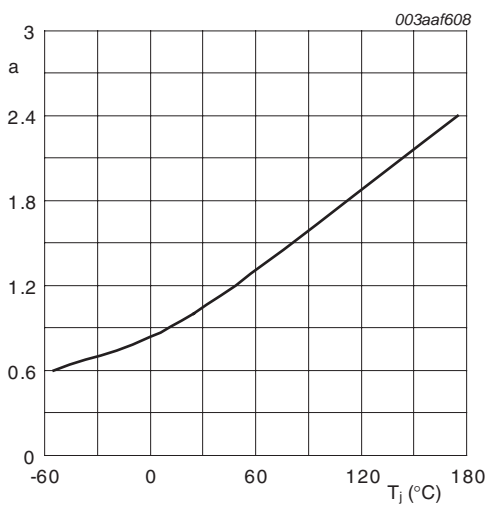
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^{\circ}\text{C}}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



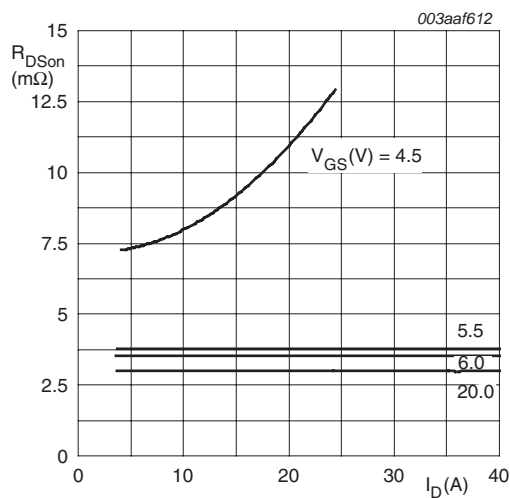


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

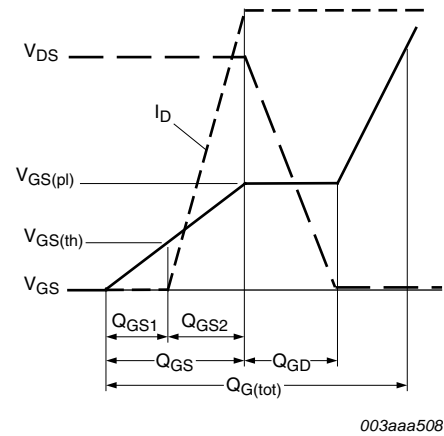
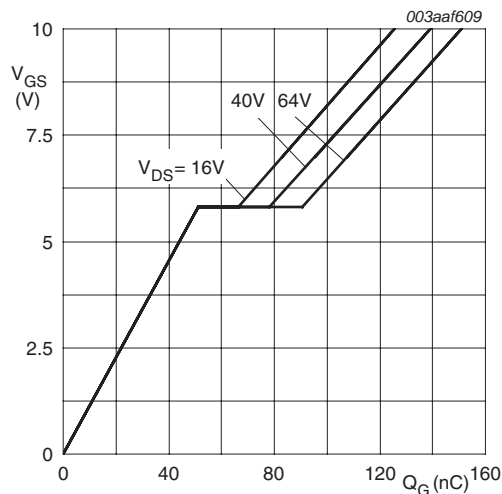
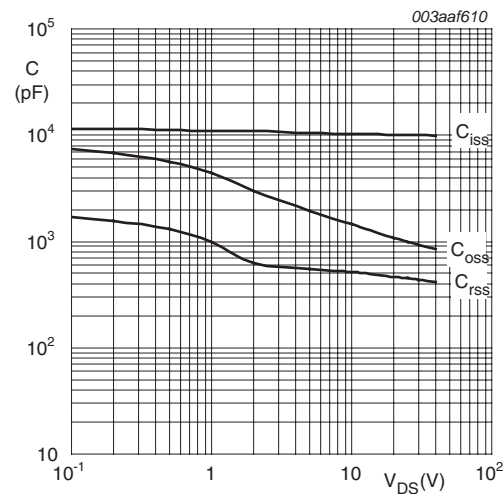


Fig 14. Gate charge waveform definitions



$T_j = 25\text{ }^{\circ}\text{C}; I_D = 75\text{ A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1\text{ MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

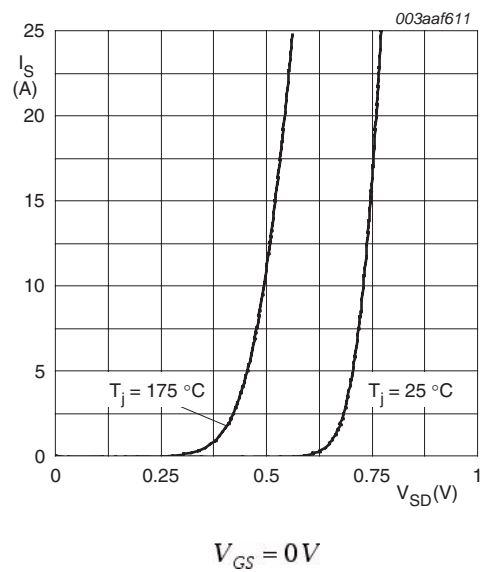


Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-262

SOT226

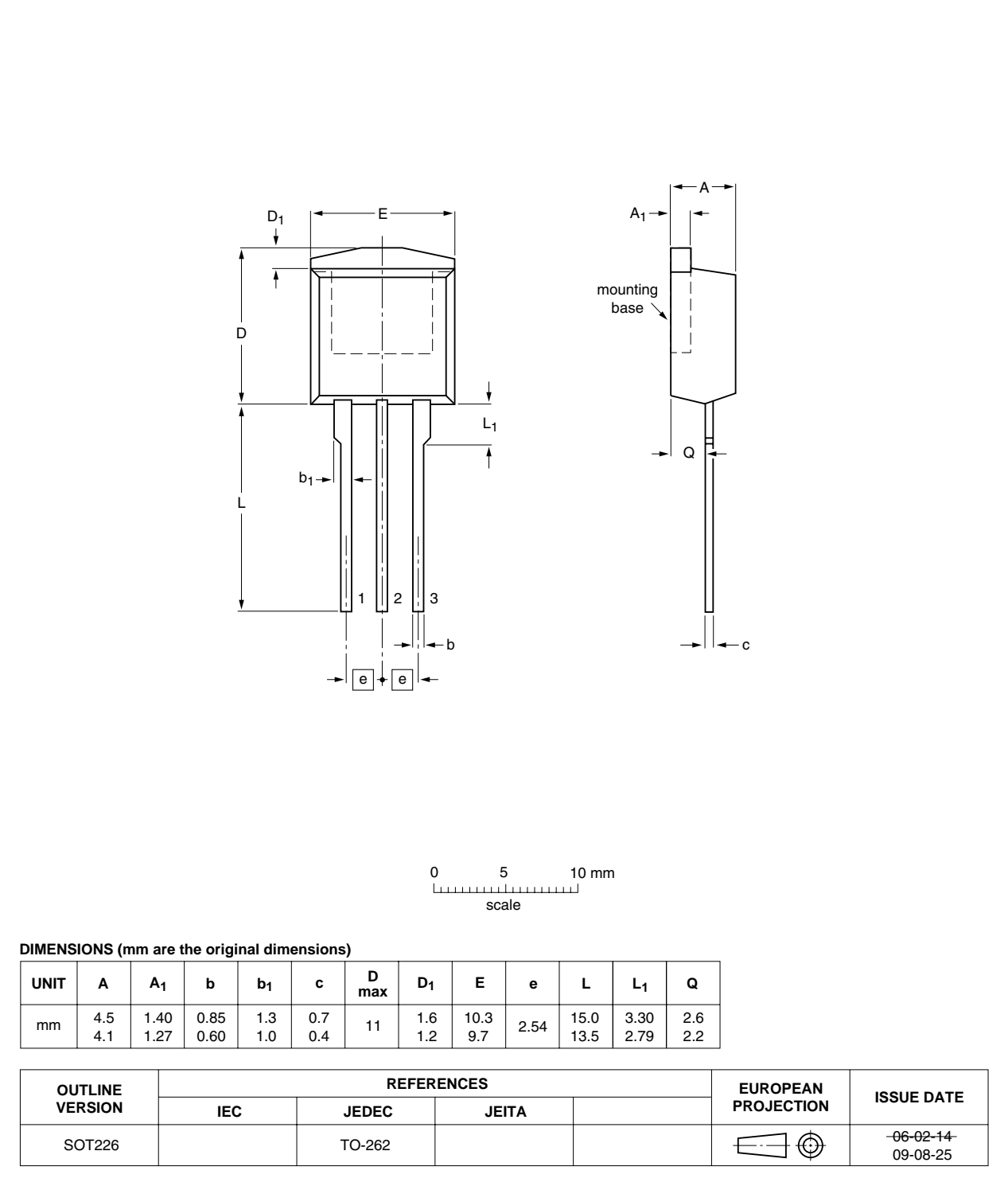


Fig 18. Package outline SOT226 (I2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN3R5-80ES v.2	20110419	Product data sheet	-	PSMN3R5-80ES v.1
Modifications:	<ul style="list-style-type: none"><li>• Status changed from objective to product.</li><li>• Various changes to content.</li></ul>			
PSMN3R5-80ES v.1	20101224	Objective data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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