



# PSMN7R0-100BS

N-channel 100V 6.8 mΩ standard level MOSFET in D2PAK.

Rev. 2 — 2 March 2012

Objective data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference data

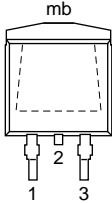
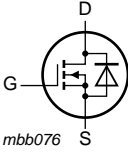
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	100	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	[1]	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	269	W
T <sub>j</sub>	junction temperature		-55	-	175	°C
Static characteristics						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 100 °C; see <a href="#">Figure 12</a>	-	-	12	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 15 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 13</a>	-	5.4	6.8	mΩ
Dynamic characteristics						
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; see <a href="#">Figure 15</a> ; see <a href="#">Figure 14</a>	-	36	-	nC
Q <sub>G(tot)</sub>	total gate charge	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 50 V; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	125	-	nC
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> = 100 V; unclamped; R <sub>GS</sub> = 50 Ω	-	-	315	mJ

[1] Continuous current is limited by package.



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT404 (D2PAK)**

[1] It is not possible to make connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN7R0-100BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

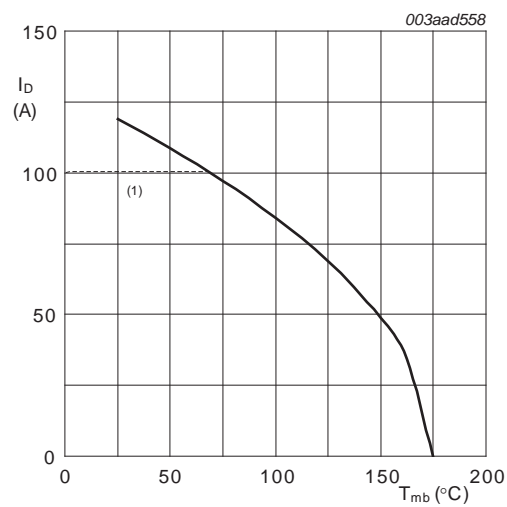
## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

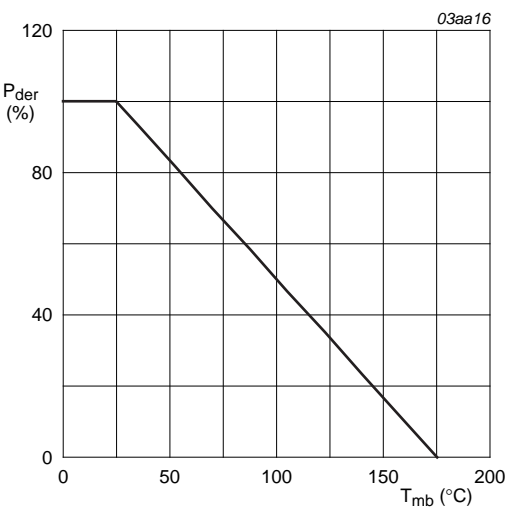
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \leq 175\text{ °C}$ ; $T_j \geq 25\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	85	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	[1]	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	475	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	269	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	[1]	100	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	475	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} = 100\text{ V}$ ; unclamped; $R_{GS} = 50\text{ }\Omega$	-	315	mJ

[1] Continuous current is limited by package.



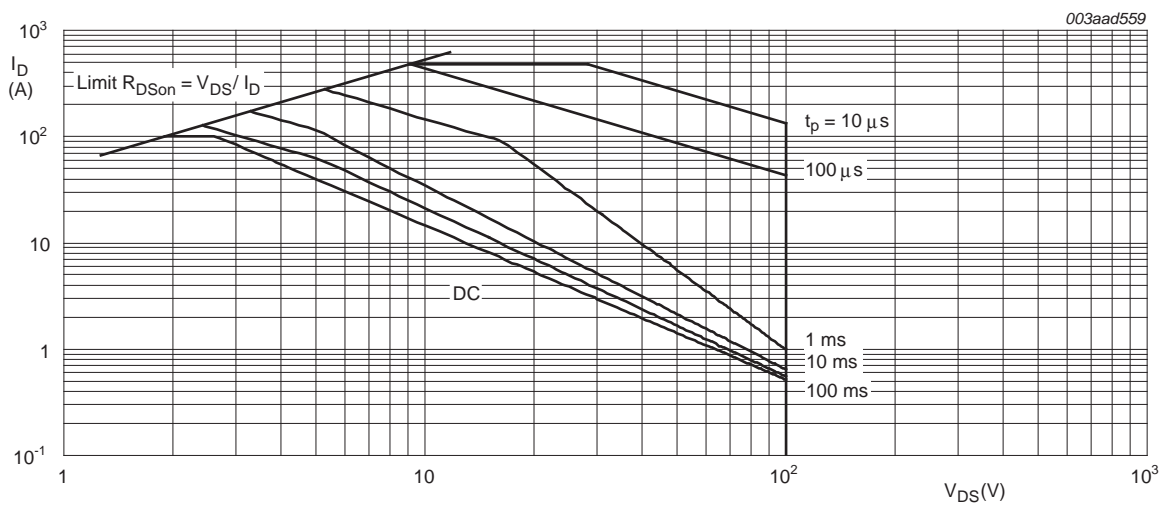
$V_{GS} \geq 10$  V; (1) capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.3	0.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	60	-	K/W

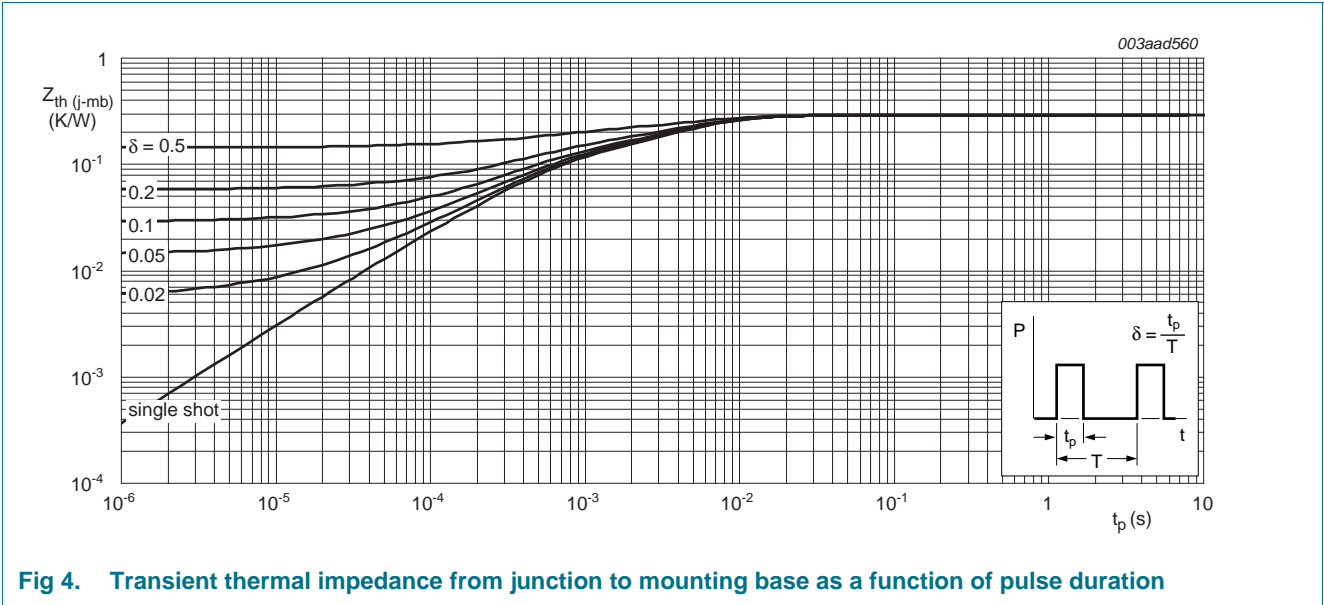


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^{\circ}\text{C}$	90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^{\circ}\text{C};$ see <a href="#">Figure 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^{\circ}\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 10</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^{\circ}\text{C};$ see <a href="#">Figure 10</a>	-	-	4.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^{\circ}\text{C}$	-	-	150	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	0.08	5	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^{\circ}\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^{\circ}\text{C};$ see <a href="#">Figure 12</a>	-	-	12	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^{\circ}\text{C};$ see <a href="#">Figure 12</a>	-	15	19	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^{\circ}\text{C};$ see <a href="#">Figure 13</a>	-	5.4	6.8	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.74	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	125	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	100	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 15</a> ; see <a href="#">Figure 14</a>	-	28	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 15</a>	-	19.4	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	9	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 15</a> ; see <a href="#">Figure 14</a>	-	36	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V};$ see <a href="#">Figure 15</a> ; see <a href="#">Figure 14</a>	-	4.3	-	V
$C_{iss}$	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	6686	-	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^{\circ}\text{C};$ see <a href="#">Figure 16</a>	-	438	-	pF
$C_{rss}$	reverse transfer capacitance		-	272	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 4.7 Ω; T <sub>j</sub> = 25 °C	-	34.6	-	ns
t <sub>r</sub>	rise time		-	45.6	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	103.9	-	ns
t <sub>f</sub>	fall time		-	49.5	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 17</a>	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = 100 A/μs; V <sub>GS</sub> = 0 V;	-	64	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 50 V	-	167	-	nC

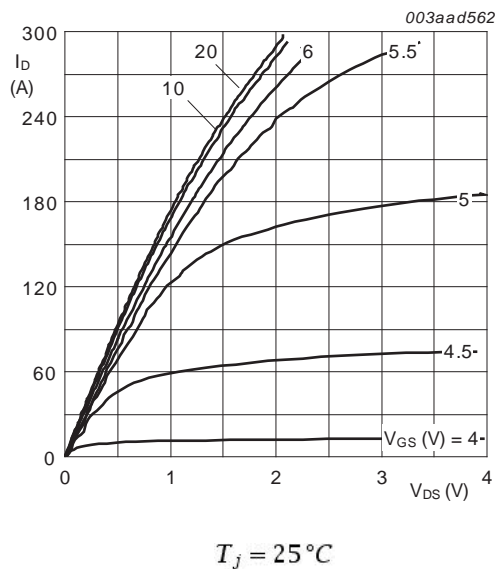


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

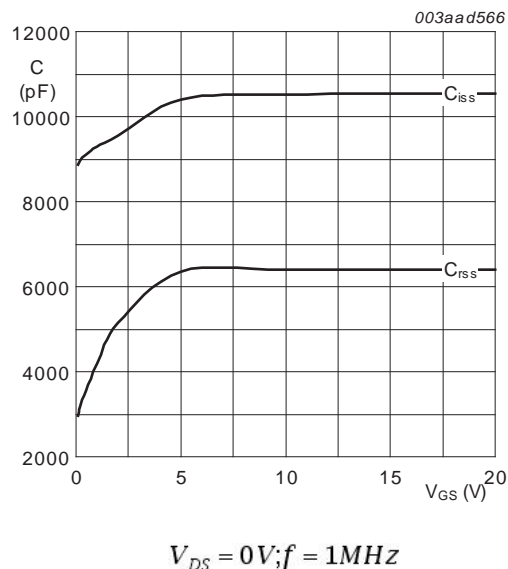


Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

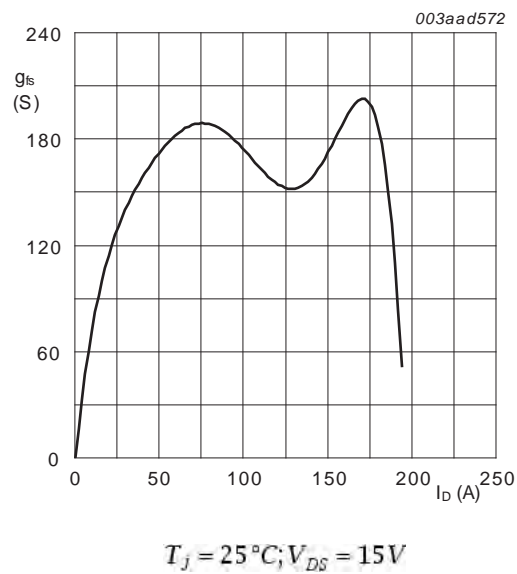


Fig 7. Forward transconductance as a function of drain current; typical values

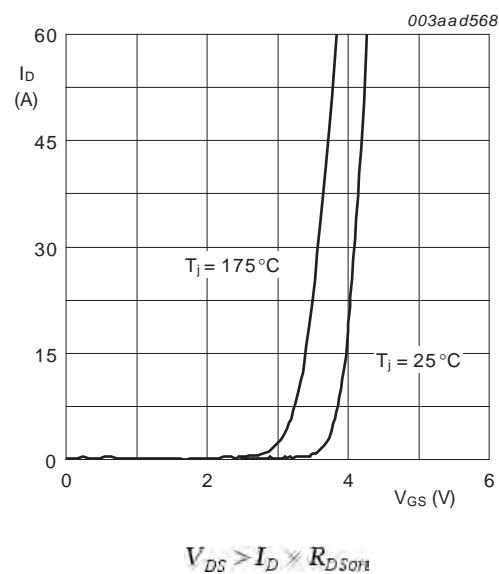


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

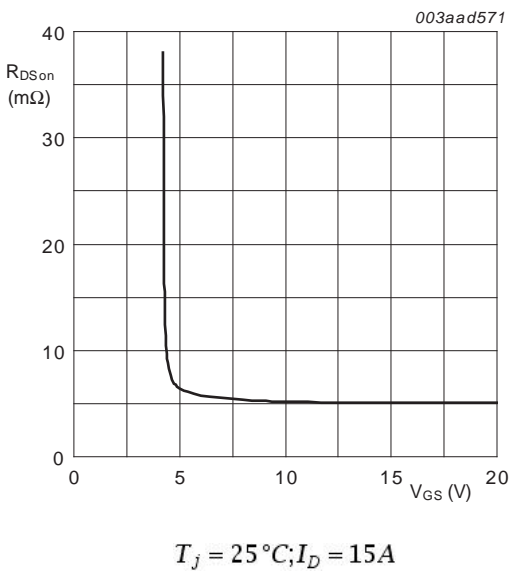


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

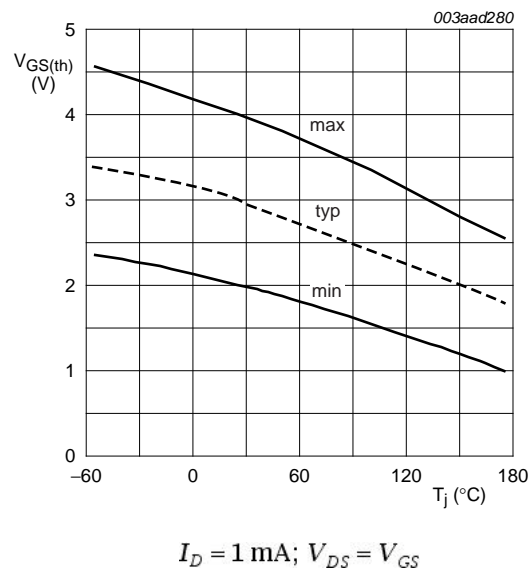
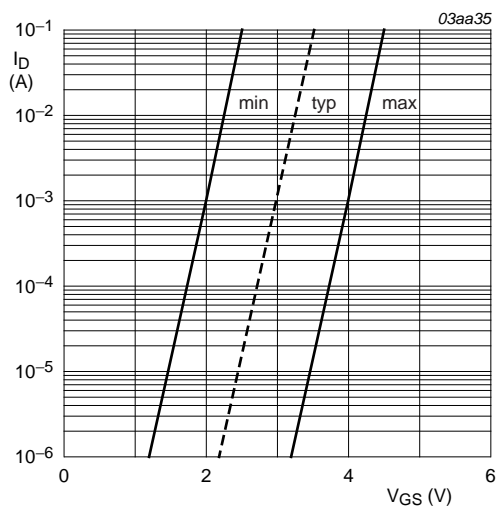
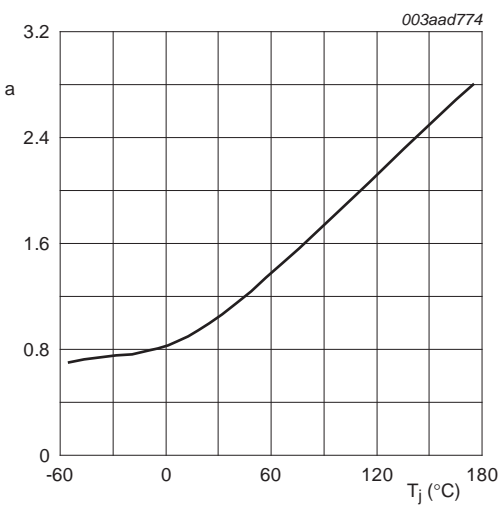


Fig 10. Gate-source threshold voltage as a function of junction temperature



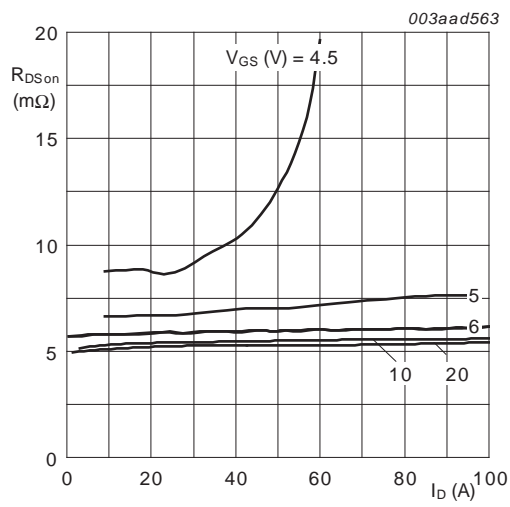
$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



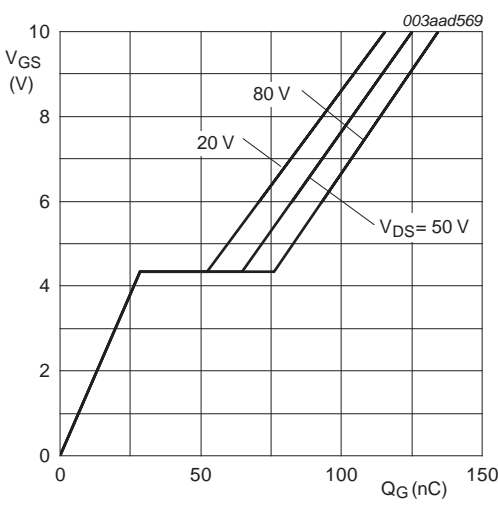
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}\text{C}$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values



$T_j = 25^{\circ}\text{C}; I_D = 25\text{A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



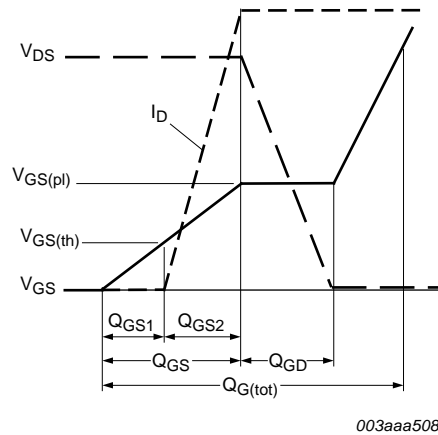
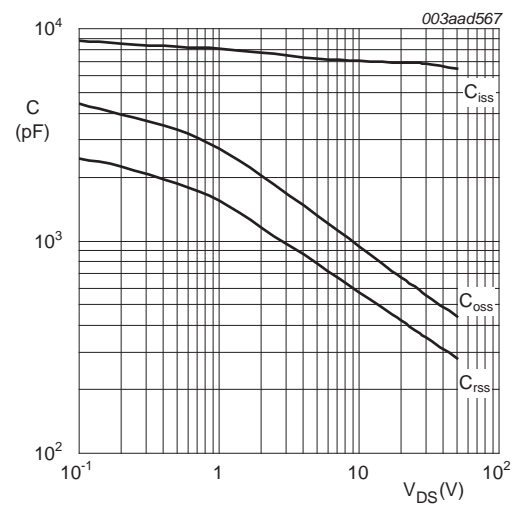
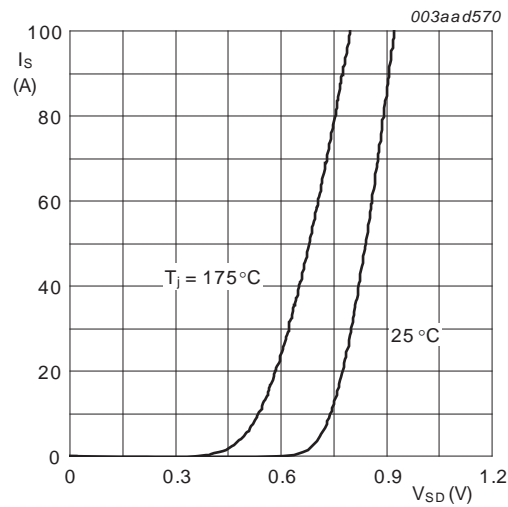


Fig 15. Gate charge waveform definitions



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404

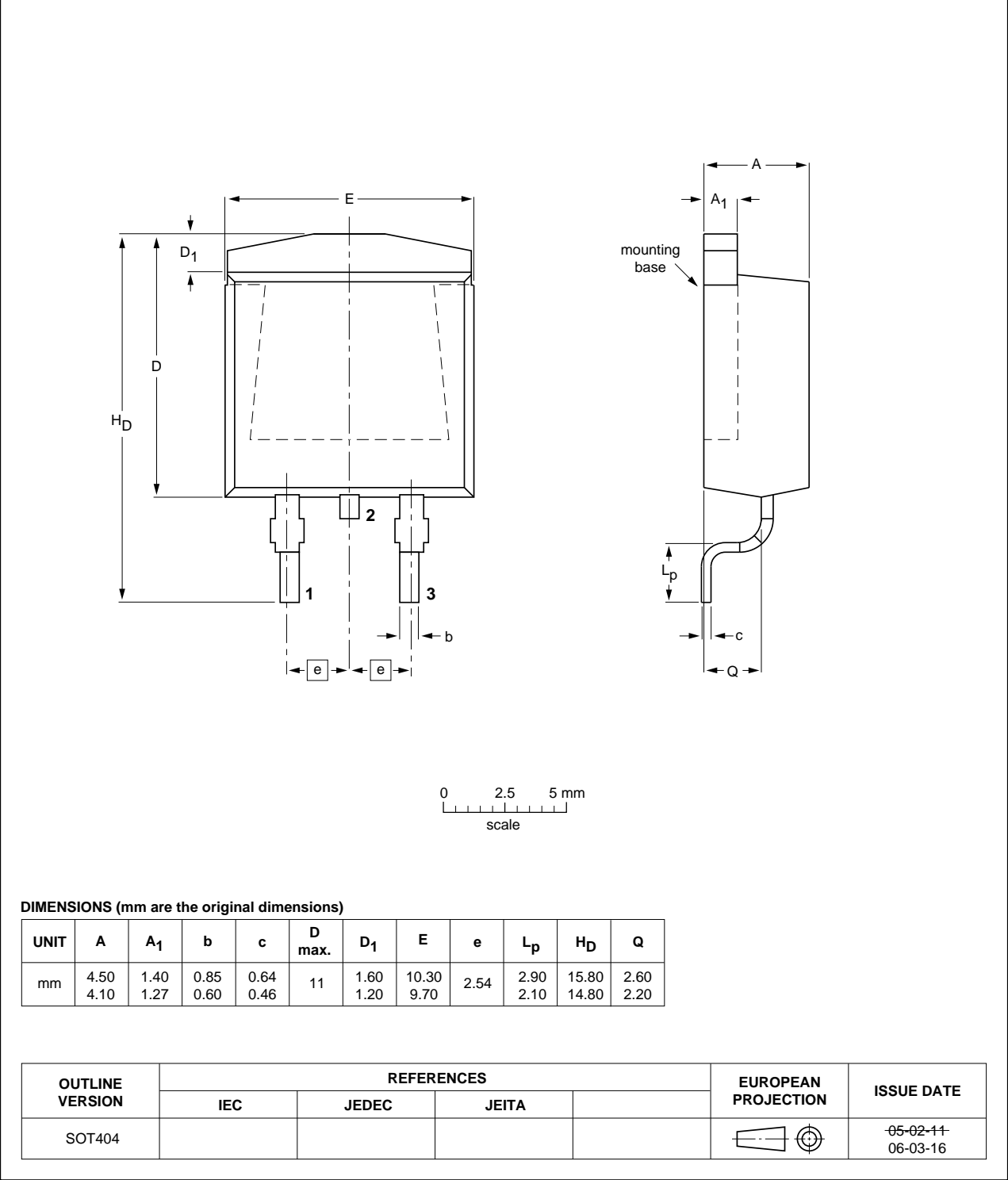


Fig 18. Package outline SOT404 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN7R0-100BS v.2	20120302	Objective data sheet	-	PSMN7R0-100BS v.1
Modifications:	• Various changes to content.			
PSMN7R0-100BS v.1	20111025	Objective data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 11. Contents

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