SC16C852L

1.8 V dual UART, 5 Mbit/s (max.) with 128-byte FIFOs, infrared (IrDA) and 16 mode or 68 mode bus interface

Rev. 4 — 1 February 2011 Product data sheet

1. General description

The SC16C852L is a 1.8 V, low power, dual channel Universal Asynchronous Receiver and Transmitter (UART) used for serial data communications. Its principal function is to convert parallel data into serial data and vice versa. The UART can handle serial data rates up to 5 Mbit/s. The SC16C852L is pin compatible with the SC16C652B. SC16C852L can be programmed to operate in extended mode (see Section 6.2) where additional advanced UART features are available. The SC16C852L UART provides enhanced UART functions with 128-byte FIFOs, modem control interface, DMA mode data transfer, and IrDA encoder/decoder. The DMA mode data transfer is controlled by the FIFO trigger levels and the $\overline{\text{TXRDYx}}$ and $\overline{\text{RXRDYx}}$ signals. On-board status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by software to meet specific user requirements. An internal loopback capability allows on-board diagnostics. Independent programmable baud rate generators are provided to select transmit and receive baud rates.

The SC16C852L with Intel (16 mode) or Motorola (68 mode) bus host interface operates at 1.8 V and is available in plastic LQFP48, TFBGA36 and very small (Micro-UART) HVQFN32 packages.

2. Features and benefits

- Dual channel high performance UART
- Intel or Motorola bus interface selectable using 16/$\overline{68}$ pin
- 1.8 V operation
- Up to 5 Mbit/s data rate
- 128-byte transmit FIFO to reduce the bandwidth requirement of the external CPU
- 128-byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU
- 128 programmable Receive and Transmit FIFO interrupt trigger levels
- 128 Receive and Transmit FIFO reporting levels (level counters)
- Automatic software (Xon/Xoff) and hardware ($\overline{\text{RTS}}$/$\overline{\text{CTS}}$ or $\overline{\text{DTR}}$/$\overline{\text{DSR}}$) flow control
- Industrial temperature range (−40 °C to +85 °C)
- Pin, function, and software compatible to SC16C652B in LQFP48 package
- 128 hardware and software trigger levels
- Automatic 9-bit mode (RS-485) address detection
- Automatic RS-485 driver turn-around with programmable delay
- Dual channel concurrent write
- UART software reset

- High resolution clock prescaler, from 0 to 15 with granularity of $^{1}/_{16}$ to allow non-standard UART clock to be used
- Programmable Xon/Xoff characters
- Software selectable baud rate generator
- Support IrDA version 1.0 (up to 115.2 kbit/s)
- Standard modem interface or infrared IrDA encoder/decoder interface
- Enhanced Sleep mode and low power feature
- Modem control functions ($\overline{CTS}$, $\overline{RTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$, $\overline{CD}$)
- Independent transmitter and receiver enable/disable
- Pb-free, RoHS compliant packages offered

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SC16C852LIB	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
SC16C852LIBS	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1
SC16C852LIET	TFBGA36	plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 × 3.5 × 0.8 mm	SOT912-1

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4. Block diagram

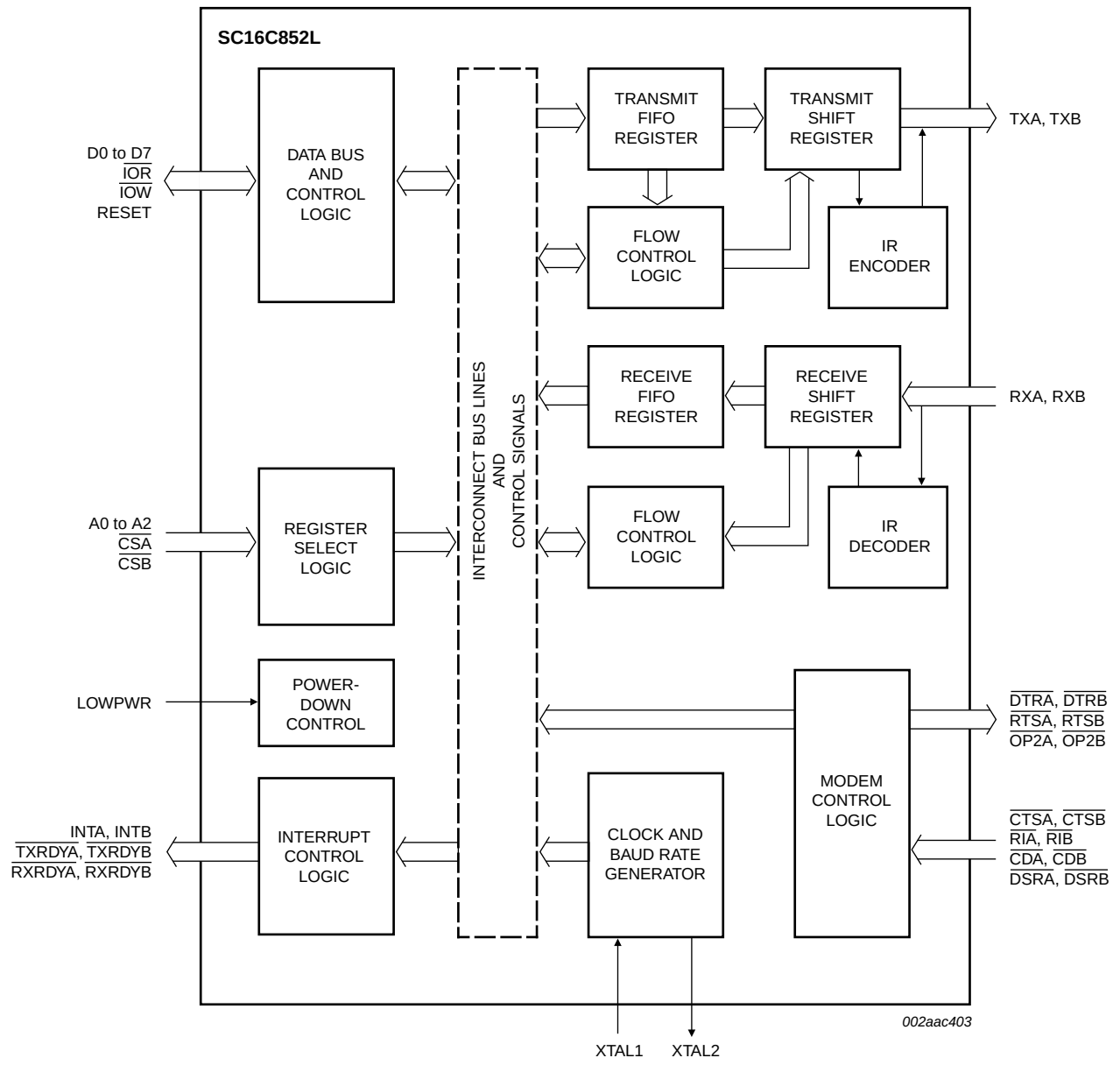

Fig 1. Block diagram of SC16C852L (16 mode)

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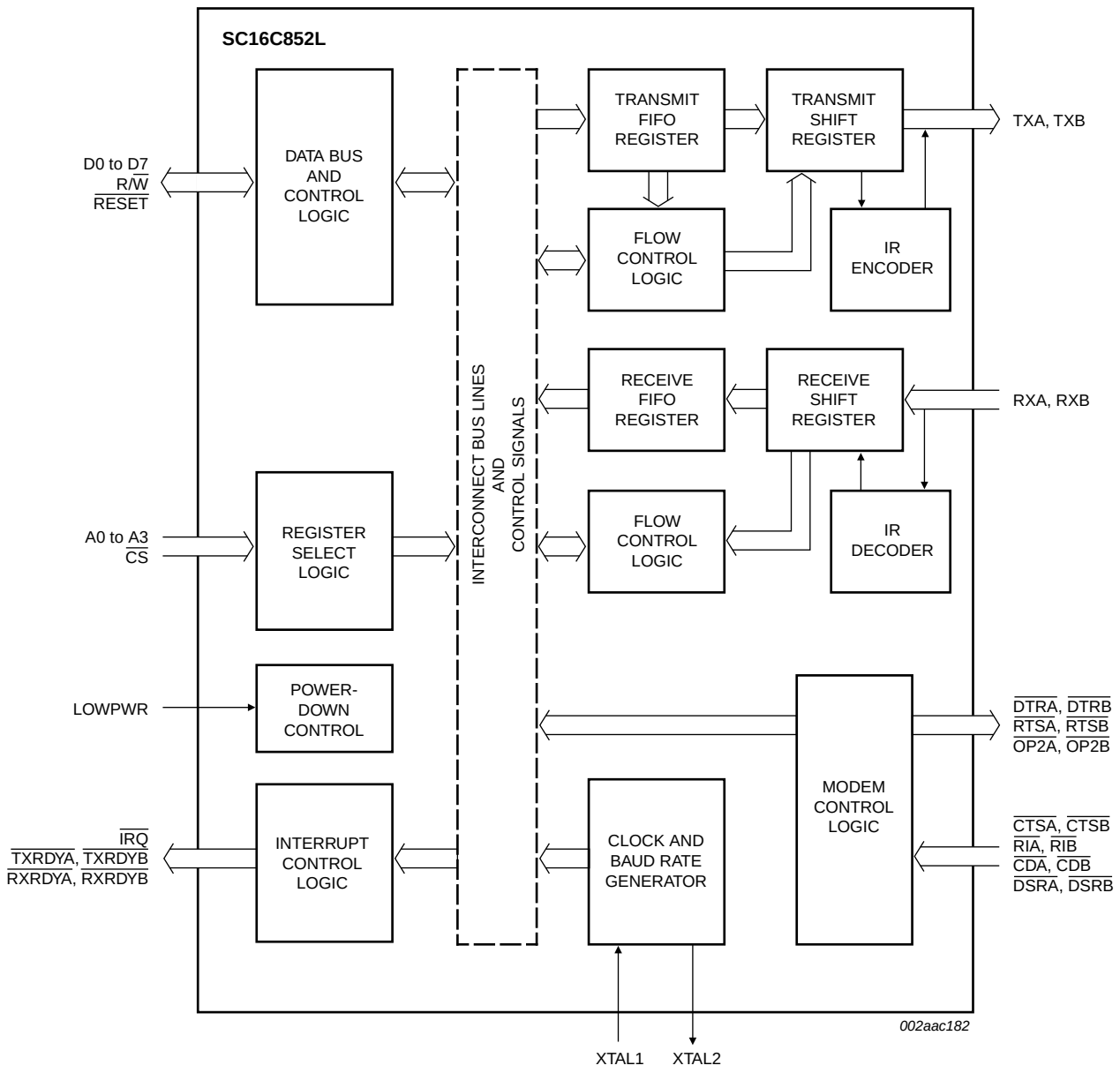

Fig 2. Block diagram of SC16C852L (68 mode)

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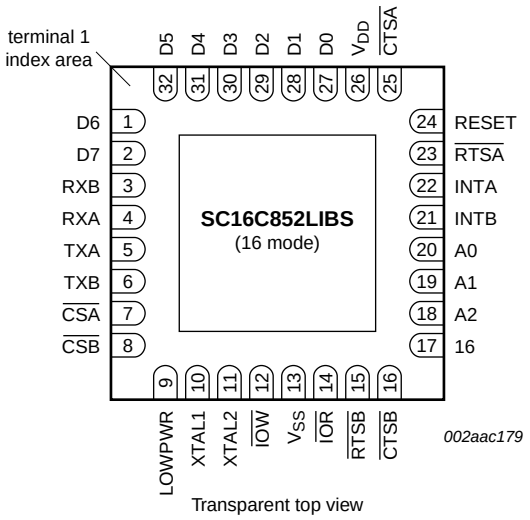
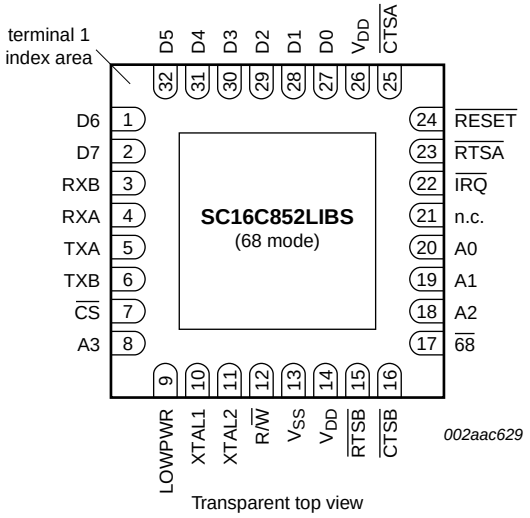
5. Pinning information

5.1 Pinning



a. 16 mode



b. 68 mode

Fig 3. Pin configuration for HVQFN32

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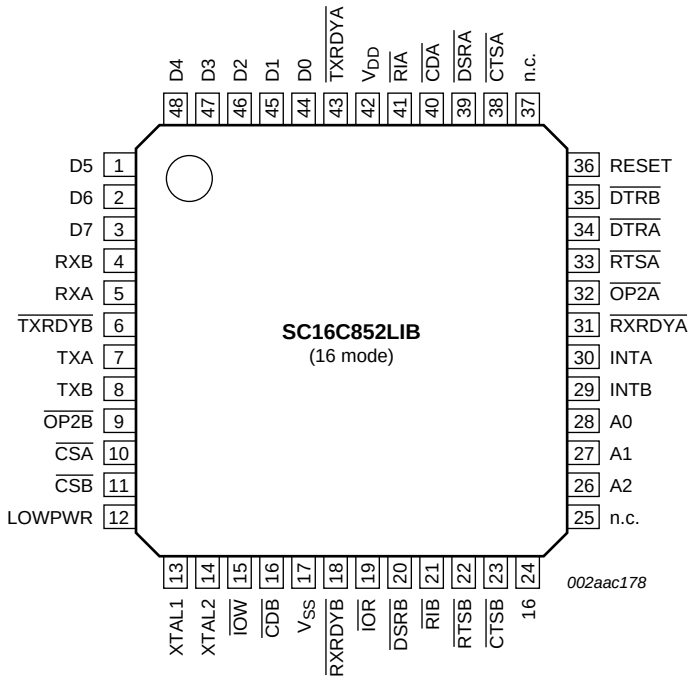
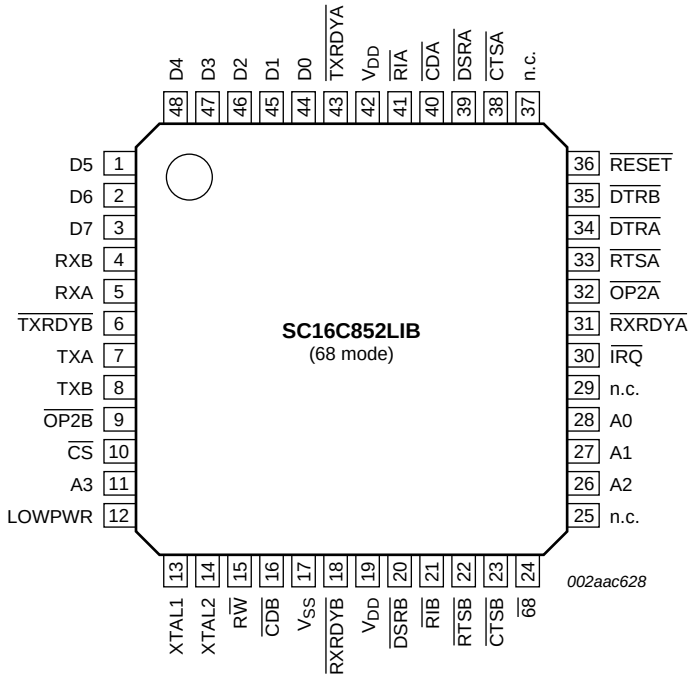


a. 16 mode



b. 68 mode

Fig 4. Pin configuration for LQFP48

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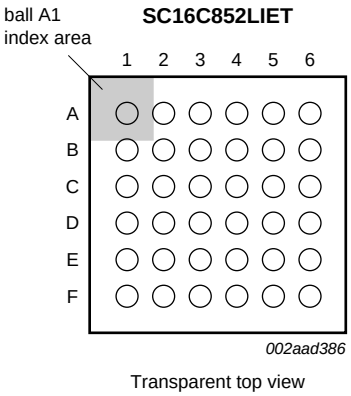

Fig 5. Pin configuration for TFBGA36

	1	2	3	4	5	6
A	D4	D2	D0	n.c.	$\overline{CTSA}$	RESET
B	D5	D3	D1	n.c.	n.c.	$\overline{RTSA}$
C	D7	RXB	D6	V_{DD}	INTA	INTB
D	RXA	TXA	LOWPWR	V_{SS}	A0	A1
E	TXB	$\overline{CSA}$	XTAL2	n.c.	$\overline{CTSB}$	A2
F	$\overline{CSB}$	XTAL1	$\overline{IOW}$	$\overline{IOR}$	$\overline{RTSB}$	16

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a. 16 mode

	1	2	3	4	5	6
A	D4	D2	D0	n.c.	$\overline{CTSA}$	$\overline{RESET}$
B	D5	D3	D1	n.c.	n.c.	$\overline{RTSA}$
C	D7	RXB	D6	V_{DD}	$\overline{IRQ}$	n.c.
D	RXA	TXA	LOWPWR	V_{SS}	A0	A1
E	TXB	$\overline{CS}$	XTAL2	n.c.	$\overline{CTSB}$	A2
F	A3	XTAL1	R/$\overline{W}$	V_{DD}	$\overline{RTSB}$	$\overline{68}$

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b. 68 mode

Fig 6. TFBGA36 ball mapping (transparent top view)

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5.2 Pin description

Table 2. Pin description

Symbol	Pin			Type	Description
	LQFP48	HVQFN32	TFBGA36		
A0	28	20	D5	I	**Address 0 select bit.** Internal register address selection.
A1	27	19	D6	I	**Address 1 select bit.** Internal register address selection.
A2	26	18	E6	I	**Address 2 select bit.** Internal register address selection.
$\overline{CDA}$	40	-	-	I	**Carrier Detect (active LOW).** These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
$\overline{CDB}$	16	-	-	I	
$\overline{CSA}$/$\overline{CS}$	10	7	E2	I	When 16/$\overline{68}$ pin is at logic 1 (or unconnected), this input is chip select for channel A. When 16/$\overline{68}$ pin is at logic 0, this input becomes the chip select for both channels (Motorola mode).
$\overline{CSB}$/A3	11	8	F1	I	When 16/$\overline{68}$ pin is at logic 1 (or unconnected), this input is chip select for channel B. When 16/$\overline{68}$ pin is at logic 0, this input becomes the address line A3 which is used for channel selection; a logic 0 selects channel A and a logic 1 selects channel B.
$\overline{CTSA}$	38	25	A5	I	**Clear to Send (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{CTSx}$ pin indicates the modem or data set is ready to accept transmit data from the SC16C852L. Status can be tested by reading MSR[4].
$\overline{CTSB}$	23	16	E5	I	
$\overline{DSRA}$	39	-	-	I	**Data Set Ready (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem or data set is powered-on and is ready for data exchange with the UART. Status can be tested by reading MSR[5].
$\overline{DSRB}$	20	-	-		
$\overline{DTRA}$	34	-	-	O	**Data Terminal Ready (active LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates that the SC16C852L is powered-on and ready. This pin can be controlled via the modem control register. Writing a logic 1 to MCR[0] will set the $\overline{DTRx}$ output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR[0], or after a reset.
$\overline{DTRB}$	35	-	-		
D0	44	27	A3	I/O	**Data bus (bidirectional).** These pins are the 8-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
D1	45	28	B3	I/O	
D2	46	29	A2	I/O	
D3	47	30	B2	I/O	
D4	48	31	A1	I/O	
D5	1	32	B1	I/O	
D6	2	1	C3	I/O	
D7	3	2	C1	I/O	

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Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	HVQFN32	TFBGA36		
INTA/$\overline{IRQ}$	30	22	C5	O	When 16/$\overline{68}$ pin is at logic 1 or unconnected, this output becomes channel A interrupt output. The output state is defined by the user through the software setting of MCR[3]. INTA is set to the active mode and $\overline{OP2A}$ output to a logic 0 when MCR[3] is set to a logic 1. INTA is set to the 3-state mode and $\overline{OP2A}$ is set to a logic 1 when MCR[3] is set to a logic 0. When 16/$\overline{68}$ pin is at logic 0, this output becomes device interrupt output (active LOW, open-drain). An external pull-up resistor to V_{DD} is required.
INTB/n.c.	29	21	C6	O	When 16/$\overline{68}$ pin is at logic 1 or unconnected, this output becomes channel B interrupt output. The output state is defined by the user through the software setting of MCR[3]. INTB is set to the active mode and $\overline{OP2B}$ output to a logic 0 when MCR[3] is set to a logic 1. INTB is set to the 3-state mode and $\overline{OP2B}$ is set to a logic 1 when MCR[3] is set to a logic 0. When 16/$\overline{68}$ pin is at logic 0, this output is not used.
$\overline{IOR}$/V_{DD}	19	14	F4	I	When 16/$\overline{68}$ pin is at logic 1, this input becomes the read strobe (active LOW). When 16/$\overline{68}$ pin is at logic 0, this input pin is not used and should be connected to V_{DD}.
$\overline{IOW}$/R/$\overline{W}$	15	12	F3	I	When 16/$\overline{68}$ pin is at logic 1 or unconnected, this input becomes the write strobe (active LOW). When 16/$\overline{68}$ pin is at logic 0, this input becomes read strobe when it is at logic HIGH, and write strobe when it is at logic LOW.
$\overline{OP2A}$	32	-	-	O	**Output 2 (user-defined).** This function is associated with individual channels, A through B. The state at these pin(s) are defined by the user and through MCR register bit 3. INTA, INTB are set to the active mode and $\overline{OP2x}$ to logic 0 when MCR[3] is set to a logic 1. INTA, INTB are set to the 3-state mode and $\overline{OP2x}$ to a logic 1 when MCR[3] is set to a logic 0 (see Table 21 "Modem Control Register bits description", bit 3). Since these bits control both the INTA, INTB operation and $\overline{OP2x}$ outputs, only one function should be used at one time, INT or $\overline{OP2}$.
$\overline{OP2B}$	9	-	-	O	
RESET/ $\overline{RESET}$	36	24	A6	I	**Master Reset.** When 16/$\overline{68}$ pin is at logic 1 or unconnected, this input becomes the RESET pin (active HIGH). When 16/$\overline{68}$ pin is at logic LOW, this input pin becomes $\overline{RESET}$ (active LOW). (See Section 7.23 "SC16C852L external reset condition and software reset" for initialization details.)
$\overline{RIA}$	41	-	-	I	**Ring Indicator (active LOW).** These inputs are associated with individual UART channels, A through B. A logic 0 on this pin indicates the modem has received a ringing signal from the telephone line. A logic 1 transition on this input pin will generate an interrupt if modem status interrupt is enabled.
$\overline{RIB}$	21	-	-	I	
$\overline{RTSA}$	33	23	B6	O	**Request to Send (active LOW).** These outputs are associated with individual UART channels, A through B. A logic 0 on the $\overline{RTSx}$ pin indicates the transmitter has data ready and waiting to send. Writing a logic 1 in the modem control register MCR[1] will set this pin to a logic 0, indicating data is available. After a reset this pin will be set to a logic 1.
$\overline{RTSB}$	22	15	F5	O	

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Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	HVQFN32	TFBGA36		
RXA	5	4	D1	I	**Receive data A, B.** These inputs are associated with individual serial channel data to the SC16C852L receive input circuits, A through B. The RXx signal will be a logic 1 during reset, idle (no data), or when not receiving data. During the local loopback mode, the RXA/RXB input pin is disabled and transmit data is connected to the UART receive input, internally.
RXB	4	3	C2	I	
$\overline{\text{RXRDYA}}$	31	-	-	O	**Receive Ready A, B (active LOW).** This function provides the receive FIFO/RHR status for individual receive channels (A to B). $\overline{\text{RXRDYx}}$ is primarily intended for monitoring DMA mode 1 transfers for the receive data FIFOs. A logic 0 indicates there is a receive data to read/upload, that is, receive ready status with one or more RX characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been reached. This signal can also be used for single mode transfers (DMA mode 0).
$\overline{\text{RXRDYB}}$	18	-	-	O	
TXA	7	5	D2	O	**Transmit data A, B.** These outputs are associated with individual serial transmit channel data from the SC16C852L. The TXx signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loopback mode, the TXA/TXB output pin is disabled and transmit data is internally connected to the UART receive input.
TXB	8	6	E1	O	
$\overline{\text{TXRDYA}}$	43	-	-	O	**Transmit Ready A, B (active LOW).** These outputs provide the transmit FIFO/THR status for individual transmit channels (A to B). $\overline{\text{TXRDYx}}$ is primarily intended for monitoring DMA mode 1 transfers for the transmit data FIFOs. An individual channel's $\overline{\text{TXRDYA}}$, $\overline{\text{TXRDYB}}$ buffer ready status is indicated by logic 0, that is, at lease one location is empty and available in the FIFO or THR. This pin goes to a logic 1 (DMA mode 1) when there are no more empty locations in the FIFO or THR. This signal can also be used for single mode transfers (DMA mode 0).
$\overline{\text{TXRDYB}}$	6	-	-	O	
V_{DD}	42	26	C4	I	**Power supply input.**
V_{SS}	17	13[1]	D4	I	**Signal and power ground.**
XTAL1	13	10	F2	I	**Crystal or external clock input.** Functions as a crystal input or as an external clock input. A crystal can be connected between this pin and XTAL2 to form an internal oscillator circuit. Alternatively, an external clock can be connected to this pin to provide custom data rates (see Section 6.9 "Programmable baud rate generator"). See Figure 8.
XTAL2	14	11	E3	O	**Output of the crystal oscillator or buffered clock.** (See also XTAL1.) Crystal oscillator output or buffered clock output. Should be left open if an external clock is connected to XTAL1.

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Table 2. Pin description *...continued*

Symbol	Pin			Type	Description
	LQFP48	HVQFN32	TFBGA36		
LOWPWR	12	9	D3	I	**Low Power.** When asserted (active HIGH), the device immediately goes into low power mode. The oscillator is shut-off and some host interface pins are isolated from the host's bus to reduce power consumption. The device only returns to normal mode when the LOWPWR pin is de-asserted. On the negative edge of a de-asserting LOWPWR signal, the device is automatically reset and all registers return to their default reset states. This pin has an internal pull-down resistor, therefore, it can be left unconnected.
16/$\overline{68}$	24	17	F6	I	**Bus select.** Intel or Motorola bus select. When 16/$\overline{68}$ pin is at logic 1 or left unconnected (internally pulled-up) the device will operate in Intel bus type of interface. When 16/$\overline{68}$ pin is at logic 0, the device will operate in Motorola bus type of interface.
n.c.	25, 37	-	A4, B4, B5, E4	-	not connected

[1] HVQFN32 package die supply ground is connected to both V_{SS} pin and exposed center pad. V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

6. Functional description

The SC16C852L provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stop bits to the transmit data to form a data character (character orientated protocol). Data integrity is ensured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex, especially when manufactured on a single integrated silicon chip. The SC16C852L represents such an integration with greatly enhanced features. The SC16C852L is fabricated with an advanced CMOS process.

The SC16C852L is an upward solution to the SC16C652B that provides a dual UART capability with 128 bytes of transmit and receive FIFO memory, instead of 32 bytes for the SC16C652 and 16 bytes in the SC16C2550. The SC16C852L is designed to work with high speed modems and shared network environments that require fast data processing time. Increased performance is realized in the SC16C852L by the transmit and receive FIFOs. This allows the external processor to handle more networking tasks within a given time. In addition, the four selectable receive and transmit FIFO trigger interrupt levels are provided in SC16C652 mode, or 128 programmable levels are provided in the extended mode for maximum data throughput performance especially when operating in a multi-channel environment (see Section 6.2 "Extended mode (128-byte FIFO)"). The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU and increases performance. A low power pin (LOWPWR) is provided to further reduce power consumption by isolating the host bus interface.

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The SC16C852L is capable of operation up to 5 Mbit/s with an external 80 MHz clock. With a crystal, the SC16C852L is capable of operation up to 1.5 Mbit/s.

The rich feature set of the SC16C852L is available through internal registers. These features are: selectable and programmable receive and transmit FIFO trigger levels, selectable TX and RX baud rates, and modem interface controls, and are all standard features. Following a power-on reset, an external reset, or a software reset, the SC16C852L is software compatible with the previous generation, SC16C2550, SC16C652B, and ST16C2450.

6.1 UART A-B functions

The UART provides the user with the capability to bidirectionally transfer information between an external CPU, the SC16C852L package, and an external serial device. A logic 0 (LOW) on chip select pins $\overline{CSA}$ and/or $\overline{CSB}$ allows the user to configure, send data, and/or receive data via UART channels A, B. Individual channel select functions are shown in Table 3 and Table 4.

Table 3. Serial port selection (Intel interface)
H = HIGH; L = LOW.

Chip Select	Function
$\overline{CSA}$ = H, $\overline{CSB}$ = H	none
$\overline{CSA}$ = L	UART channel A
$\overline{CSB}$ = L	UART channel B

Table 4. Serial port selection (Motorola interface)
H = HIGH; L = LOW.

Chip Select	Function
$\overline{CS}$ = H	none
$\overline{CS}$ = L, A3 = L	UART channel A
$\overline{CS}$ = L, A3 = H	UART channel B

6.2 Extended mode (128-byte FIFO)

The device is in the extended mode when any of these four registers contains any value other than 0: FLWCNTH, FLWCNTL, TXINTLVL, RXINTLVL.

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6.3 Internal registers

The SC16C852L provides two sets of internal registers (A and B) consisting of 25 registers each for monitoring and controlling the functions of each channel of the UART. These registers are shown in Table 5.

Table 5. Internal registers decoding

A2	A1	A0	Read mode	Write mode
General register set (THR/RHR, IER/ISR, MCR/MSR, FCR, LCR/LSR, SPR)[1]				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1	Interrupt Enable Register	Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1	Line Control Register	Line Control Register
1	0	0	Modem Control Register	Modem Control Register
1	0	1	Line Status Register	Extra Feature Control Register (EFCR)
1	1	0	Modem Status Register	n/a
1	1	1	Scratchpad Register	Scratchpad Register
Baud rate register set (DLL/DLM)[2]				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Second special register set (TXLVLCNT/RXLVLCNT)[3]				
0	1	1	Transmit FIFO Level Count	n/a
1	0	0	Receive FIFO Level Count	n/a
Enhanced feature register set (EFR, Xon1/Xon2, Xoff1/Xoff2)[4]				
0	1	0	Enhanced Feature Register	Enhanced Feature Register
1	0	0	Xon1 word	Xon1 word
1	0	1	Xon2 word	Xon2 word
1	1	0	Xoff1 word	Xoff1 word
1	1	1	Xoff2 word	Xoff2 word
First extra feature register set (TXINTLVL/RXINTLVL, FLWCNTH/FLWCNTL)[5]				
0	1	0	Transmit FIFO Interrupt Level	Transmit FIFO Interrupt Level
1	0	0	Receive FIFO Interrupt Level	Receive FIFO Interrupt Level
1	1	0	Flow Control Count High	Flow Control Count High
1	1	1	Flow Control Count Low	Flow Control Count Low
Second extra feature register set (CLKPRES, RS485TIME, AFCR2, AFCR1)[6]				
0	1	0	Clock Prescaler	Clock Prescaler
1	0	0	RS-485 turn-around Timer	RS-485 turn-around Timer
1	1	0	Additional Feature Control Register 2	Additional Feature Control Register 2
1	1	1	Additional Feature Control Register 1	Additional Feature Control Register 1

[1] These registers are accessible only when LCR[7] is a logic 0.

[2] These registers are accessible only when LCR[7] is a logic 1.

[3] Second special registers are accessible only when EFCR[0] = 1.

[4] Enhanced feature registers are only accessible when LCR = 0xBF.

[5] First extra feature registers are only accessible when EFCR[2:1] = 01b.

[6] Second extra feature registers are only accessible when EFCR[2:1] = 10b.

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6.4 FIFO operation

6.4.1 32-byte FIFO mode

When all four of these registers (TXINTLVL, RXINTLVL, FLWCNTH, FLWCNTL) in the 'First extra feature register set' are empty (0x00) the transmit and receive trigger levels are set by FCR[7:4]. In this mode the transmit and receive trigger levels are backward compatible to the SC16C652B (see Table 6), and the FIFO sizes are 32 entries. The transmit and receive data FIFOs are enabled by the FIFO Control Register bit 0 (FCR[0]). It should be noted that the user can set the transmit trigger levels by writing to the FCR, but activation will not take place until EFR[4] is set to a logic 1. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU (see Section 6.8). Please refer to Table 13 and Table 14 for the setting of FCR[7:4].

Table 6. Interrupt trigger level and flow control mechanism

FCR[7:6]	FCR[5:4]	INTA/INTB pin activation		Negate $\overline{RTS}$ or send Xoff	Assert $\overline{RTS}$ or send Xon
		RX	TX		
00	00	8	16	8	0
01	01	16	8	16	7
10	10	24	24	24	15
11	11	28	30	28	23

6.4.2 128-byte FIFO mode

When either TXINTLVL, RXINTLVL, FLWCNTH or FLWCNTL in the 'first extra feature register set' contains any value other than 0x00, the transmit and receive trigger levels are set by TXINTLVL and RXINTLVL registers. TXINTLVL sets the trigger levels for the transmit FIFO, and the transmit trigger levels can be set to any value between 1 and 128 with granularity of 1. RXINTLVL sets the trigger levels for the receive FIFO, the receive trigger levels can be set to any value between 1 and 128 with granularity of 1.

When the effective FIFO size changes (that is, when FCR[0] toggles or when the combined content of TXINTLVL, RXINTLVL, FLWCNTH and FLWCNTL changes between equal and unequal to 0x00), both RX FIFO and TX FIFO will be reset (data in the FIFO will be lost).

6.5 Hardware flow control

When automatic hardware flow control is enabled, the SC16C852L monitors the $\overline{CTSA}$/$\overline{CTSB}$ pin for a remote buffer overflow indication and controls the $\overline{RTSA}$/$\overline{RTSB}$ pin for local buffer overflows. Automatic hardware flow control is selected by setting EFR[6] (RTS) and EFR[7] (CTS) to a logic 1. If $\overline{CTS}$ transitions from a logic 0 to a logic 1 indicating a flow control request, ISR[5] will be set to a logic 1 (if enabled via IER[7:6]), and the SC16C852L will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the $\overline{CTSx}$ input returns to a logic 0, indicating more data may be sent.

When AFCR1[2] is set to logic 1 then the function of $\overline{CTSA}$/$\overline{CTSB}$ pin is mapped to the $\overline{DSRA}$/$\overline{DSRB}$ pin, and the function of $\overline{RTSA}$/$\overline{RTSB}$ is mapped to $\overline{DTRA}$/$\overline{DTRB}$ pin. $\overline{DSRx}$ and $\overline{DTRx}$ pins will behave as described above for $\overline{CTS}$ and $\overline{RTS}$.

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With the automatic hardware flow control function enabled, an interrupt is generated when the receive FIFO reaches the programmed trigger level. The RTSx (or DTRx) pin will not be forced to a logic 1 (RTS off), until the receive FIFO reaches the next trigger level. However, the RTSx (or DTRx) pin will return to a logic 0 after the receive buffer (FIFO) is unloaded to the next trigger level below the programmed trigger level. Under the above described conditions, the SC16C852L will continue to accept data until the receive FIFO is full.

When the TXINTLVL, RXINTLVL, FLWCNTH and FLWCNTL in the 'first extra feature register set' are all zeroes, the hardware and software flow control trigger levels are set by FCR[7:4]; see Table 6.

When the TXINTLVL, RXINTLVL, FLWCNTH or FLWCNTL in the 'first extra feature register set' contain any value other than 0x00, the hardware and software flow control trigger levels are set by FLWCNTH and FLWCNTL. The content in FLWCNTH determines how many bytes are in the receive FIFO before RTS (or DTR) is de-asserted or Xoff is sent. The content in FLWCNTL determines how many bytes are in the receive FIFO before RTS (or DTR) is asserted, or Xon is sent.

In 128-byte FIFO mode, hardware and software flow control trigger levels can be set to any value between 1 and 128 in granularity of 1. The value of FLWCNTH should always be greater than FLWCNTL. The UART does not check for this condition automatically, and if this condition is not met, spurious operation of the device might occur. When using FLWCNTH and FLWCNTL, these registers must be initialized to proper values before hardware or software flow control is enabled via the EFR register.

6.6 Software flow control

When software flow control is enabled, the SC16C852L compares one or two sequentially received data characters with the programmed Xon or Xoff character value(s). If the received character(s) match the programmed Xoff values, the SC16C852L will halt transmission (TX) as soon as the current character(s) has completed transmission. When a match occurs, ISR bit 4 will be set (if enabled via IER[5]) and the interrupt output pin (if receive interrupt is enabled) will be activated. Following a suspension due to a match of the Xoff characters' values, the SC16C852L will monitor the receive data stream for a match to the Xon1/Xon2 character value(s). If a match is found, the SC16C852L will resume operation and clear the flags (ISR[4]).

Reset initially sets the contents of the Xon/Xoff 8-bit flow control registers to a logic 0. Following reset, the user can write any Xon/Xoff value desired for software flow control. Different conditions can be set to detect Xon/Xoff characters and suspend/resume transmissions (see Table 26). When double 8-bit Xon/Xoff characters are selected, the SC16C852L compares two consecutive receive characters with two software flow control 8-bit values (Xon1, Xon2, Xoff1, Xoff2) and controls TX transmissions accordingly. Under the above described flow control mechanisms, flow control characters are not placed (stacked) in the receive FIFO. When using software flow control, the Xon/Xoff characters cannot be used for data transfer.

In the event that the receive buffer is overfilling, the SC16C852L automatically sends an Xoff character (when enabled) via the serial TX output to the remote UART. The SC16C852L sends the Xoff1/Xoff2 characters as soon as the number of received data in

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the receive FIFO passes the programmed trigger level. To clear this condition, the SC16C852L will transmit the programmed Xon1/Xon2 characters as soon as the number of characters in the receive FIFO drops below the programmed trigger level.

6.7 Special character detect

A special character detect feature is provided to detect an 8-bit character when EFR[5] is set. When an 8-bit character is detected, it will be placed on the user-accessible data stack along with normal incoming RX data. This condition is selected in conjunction with EFR[3:0] (see Table 26). Note that software flow control should be turned off when using this special mode by setting EFR[3:0] to all zeroes.

The SC16C852L compares each incoming receive character with Xoff2 data. If a match occurs, the received data will be transferred to the FIFO, and ISR[4] will be set to indicate detection of a special character. Although Table 10 “SC16C852L internal registers” shows Xon1, Xon2, Xoff1, Xoff2 with eight bits of character information, the actual number of bits is dependent on the programmed word length. Line Control Register bits LCR[1:0] define the number of character bits, that is, either 5 bits, 6 bits, 7 bits or 8 bits. The word length selected by LCR[1:0] also determines the number of bits that will be used for the special character comparison. Bit 0 in Xon1, Xon2, Xoff1, Xoff2 corresponds with the LSB bit for the received character.

6.8 Interrupt priority and time-out interrupts

The interrupts are enabled by IER[7:0]. Care must be taken when handling these interrupts. Following a reset, if Interrupt Enable Register (IER) bit 1 = 1, the SC16C852L will issue a Transmit Holding Register interrupt. This interrupt must be serviced prior to continuing operations. The ISR indicates the current singular highest priority interrupt only. A condition can exist where a higher priority interrupt masks the lower priority interrupt(s) (see Table 15). Only after servicing the higher pending interrupt will the lower priority interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

Receive Data Ready and Receive Time-Out have the same interrupt priority (when enabled by IER[0]), and it is important to serve these interrupts correctly. The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case, the SC16C852L FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should re-check LSR[0] to see if there are any additional characters. A Receive Time-Out will not occur if the receive FIFO is empty. The time-out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read. The actual time-out value is 4 character time, including data information length, start bit, parity bit, and the size of stop bit, that is, 1×, 1.5×, or 2× bit times.

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6.9 Programmable baud rate generator

The SC16C852L UART contains a programmable rational baud rate generator that takes any clock input and divides it by a divisor in the range between 1 and ($2^{16} - 1$). The SC16C852L offers the capability of dividing the input frequency by rational divisor. The fractional part of the divisor is controlled by the CLKPRES register in the 'first extra feature register set'.

$$baud\ rate = \frac{f_{XTAL1}}{MCR[7] \times \left[16 \times \left(N + \frac{M}{16}\right)\right]} \quad (1)$$

where:

N is the integer part of the divisor in DLL and DLM registers;

M is the fractional part of the divisor in CLKPRES register;

f_{XTAL1} is the clock frequency at XTAL1 pin.

Prescaler = 1 when MCR[7] is set to 0.

Prescaler = 4 when MCR[7] is set to 1.

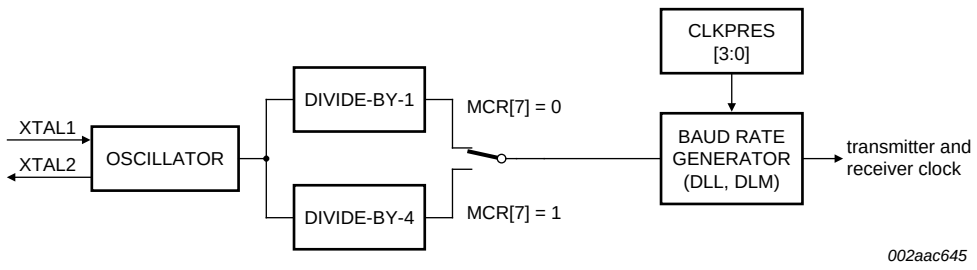

Fig 7. Prescalers and baud rate generator block diagram

A single baud rate generator is provided for the transmitter and receiver. The programmable Baud Rate Generator is capable of operating with a frequency of up to 80 MHz. To obtain maximum data rate, it is necessary to use full rail swing on the clock input. The SC16C852L can be configured for internal or external clock operation. For internal clock operation, an industry standard crystal is connected externally between the XTAL1 and XTAL2 pins (see Figure 8). Alternatively, an external clock can be connected to the XTAL1 pin (see Figure 9) to clock the internal baud rate generator for standard or custom rates (see Table 7).

The generator divides the input 16× clock by any divisor from 1 to ($2^{16} - 1$). The SC16C852L divides the basic external clock by 16. The baud rate is configured via the CLKPRES, DLL and DLM internal register functions. Customized baud rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of the baud rate generator.

Programming the baud rate generator registers CLKPRES, DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 7 shows the selectable baud rate table available when using a 1.8432 MHz external clock input when MCR[7] = 0, and CLKPRES = 0x00.

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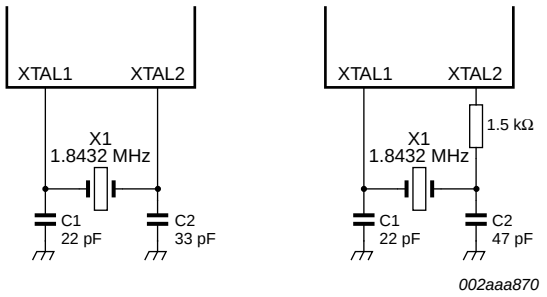
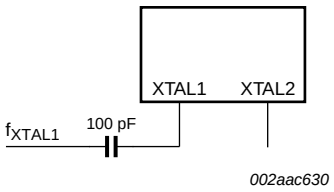


Fig 8. Crystal oscillator connection



If f_{XTAL1} frequency is greater than 50 MHz, then a DC blocking capacitor is required.

XTAL2 pin should be left unconnected when an external clock is used.

Fig 9. External clock connection

Table 7. Baud rate generator programming table using a 1.8432 MHz clock when MCR[7] = 0 and CLKPRES[3:0] = 0

Output baud rate (bit/s)	Output 16× clock divisor (decimal)	Output 16× clock divisor (hexadecimal)	DLM program value (hexadecimal)	DLL program value (hexadecimal)
50	2304	900	09	00
75	1536	600	06	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1.2 k	96	60	00	60
2.4 k	48	30	00	30
3.6 k	32	20	00	20
4.8 k	24	18	00	18
7.2 k	16	10	00	10
9.6 k	12	0C	00	0C
19.2 k	6	06	00	06
38.4 k	3	03	00	03
57.6 k	2	02	00	02
115.2 k	1	01	00	01

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6.10 DMA operation

The SC16C852L FIFO trigger level provides additional flexibility to the user for block mode operation. The user can optionally operate the transmit and receive FIFOs in the DMA mode (FCR[3]). The DMA mode affects the state of the $\overline{RXRDYA}$/$\overline{RXRDYB}$ and $\overline{TXRDYA}$/$\overline{TXRDYB}$ output pins. Table 8 and Table 9 show this.

Table 8. Effect of DMA mode on state of $\overline{RXRDYA}$/$\overline{RXRDYB}$ pin

Non-DMA mode	DMA mode
1 = FIFO empty	0-to-1 transition when FIFO empties
0 = at least 1 byte in FIFO	1-to-0 transition when FIFO reaches trigger level, or time-out occurs[1]

[1] Receive FIFO becomes full at 32 bytes when in normal mode. When TXINTLVL or RXINTLVL or FLWCNTH or FLWCNTL contains any value other than 0x00 (extended mode), then the receive FIFO becomes full at 128 bytes.

Table 9. Effect of DMA mode on state of $\overline{TXRDYA}$/$\overline{TXRDYB}$ pin

Non-DMA mode	DMA mode
1 = at least 1 byte in FIFO	0-to-1 transition when FIFO becomes full[1]
0 = FIFO empty	1-to-0 transition when FIFO has at least one empty location

[1] Transmit FIFO becomes full at 32 bytes when in normal mode. When TXINTLVL or RXINTLVL or FLWCNTH or FLWCNTL contains any value other than 0x00 (extended mode), then the transmit FIFO becomes full at 128 bytes.

6.11 Loopback mode

The internal loopback capability allows on-board diagnostics. In the Loopback mode, the normal modem interface pins are disconnected and reconfigured for loopback internally (see Figure 10). MCR[3:0] register bits are used for controlling loopback diagnostic testing. In the Loopback mode, the transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally. The $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from their normal modem control input pins, and instead are connected internally to $\overline{RTS}$, $\overline{DTR}$, MCR[3] ($\overline{OP2A}$/$\overline{OP2B}$) and MCR[2] ($\overline{OP1A}$/$\overline{OP1B}$). Loopback test data is entered into the transmit holding register via the user data bus interface, D[7:0]. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loopback connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface D[7:0]. The user optionally compares the received data to the initial transmitted data for verifying error-free operation of the UART TX/RX circuits.

In this mode, the interrupt pin is 3-stated, therefore, the software must use the polling method (see Section 7.2.2) to send and receive data.

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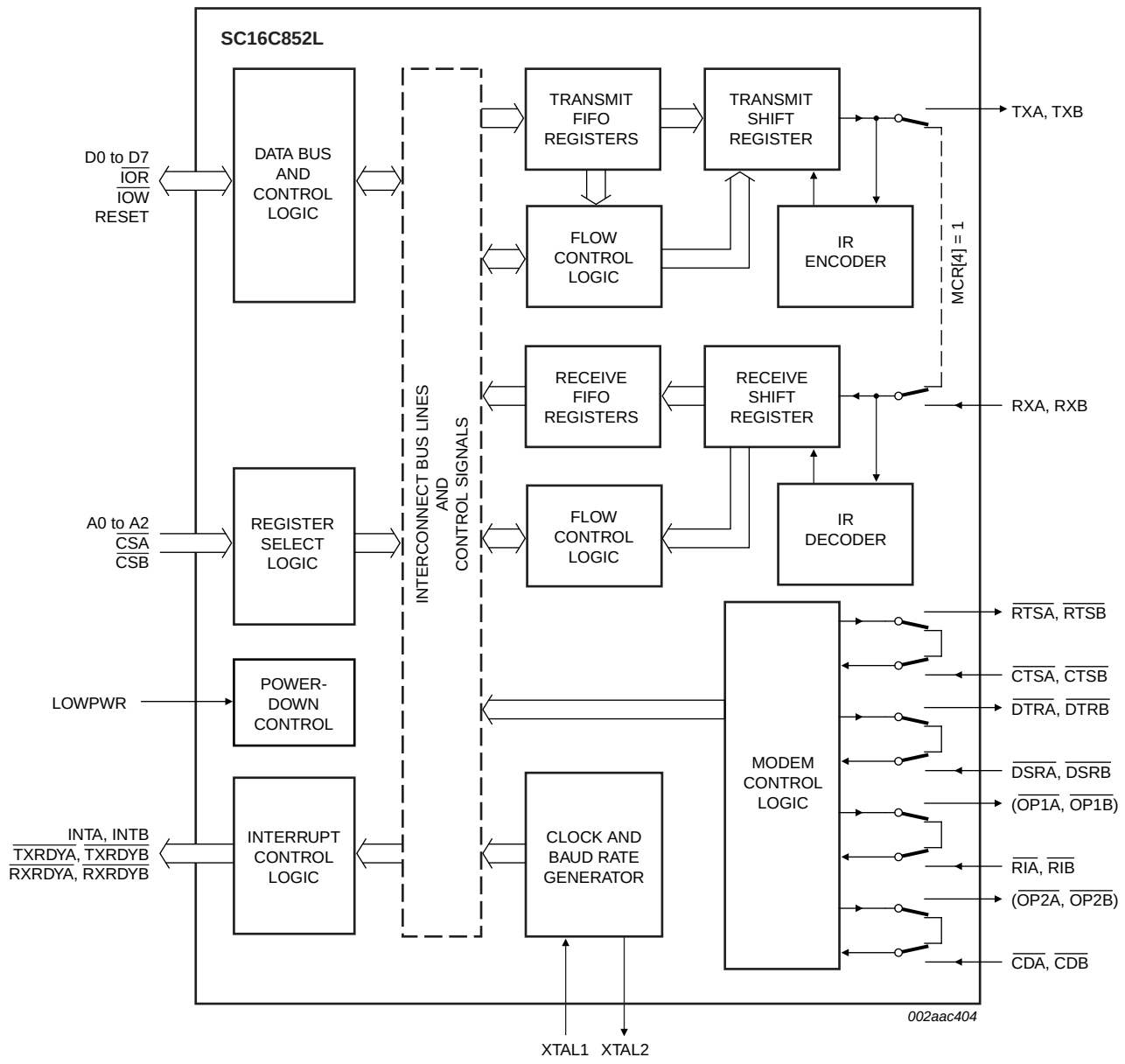

Fig 10. Internal Loopback mode diagram

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6.12 Sleep mode

Sleep mode is an enhanced feature of the SC16C852L UART. It is enabled when EFR[4], the enhanced functions bit, is set **and** when IER[4] of both channels are set.

6.12.1 Conditions to enter Sleep mode

Sleep mode is entered when:

- Modem input pins are not toggling.
- The serial data input line, RXA or RXB, is idle for 4 character time (logic HIGH) and AFCR1[4] is logic 0. When AFCR1[4] is logic 1 the device will go to sleep regardless of the state of the RXA/RXB pin (see Section 7.21 for the description of AFCR1 bit 4).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending.
- The RX FIFO is empty.

In Sleep mode, the UART clock and baud rate clock are stopped. Since most registers are clocked using these clocks, the power consumption is greatly reduced.

Remark: Writing to the divisor latches, DLL and DLM, to set the baud clock, must not be done during Sleep mode. Therefore, it is advisable to disable Sleep mode using IER[4] before writing to DLL or DLM.

6.12.2 Conditions to resume normal operation

SC16C852L resumes normal operation by any of the following:

- Receives a start bit on RXA/RXB pin.
- Data is loaded into transmit FIFO.
- A change of state on any of the modem input pins

If the device is awakened by one of the conditions described above, it will return to the Sleep mode automatically after all the conditions described in Section 6.12.1 are met. The device will stay in Sleep mode until it is disabled by setting any channel's IER bit 4 to a logic 0.

When the SC16C852L is in Sleep mode and the host data bus (D[7:0], A[2:0], $\overline{IOW}$, $\overline{IOR}$, $\overline{CSA}$, $\overline{CSB}$) remains in steady state, either HIGH or LOW, the Sleep mode supply current will be in the μA range as specified in Table 38 "Static characteristics". If any of these signals is toggling or floating then the sleep current will be higher.

6.13 Low power feature

A Low power feature is provided by the SC16C852L to prevent the switching of the host data bus from influencing the sleep current. When the pin LOWPWR is activated (logic HIGH), the device immediately and unconditionally goes into Low power mode. All clocks are stopped and most host interface pins are isolated to reduce power consumption. The device only returns to normal mode when the LOWPWR pin is de-asserted. The pin can be left unconnected because it has an internal pull-down resistor.

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6.14 RS-485 features

6.14.1 Auto RS-485 $\overline{\text{RTS}}$ control

Normally the $\overline{\text{RTSA}}$/$\overline{\text{RTSB}}$ pin is controlled by MCR bit 1, or if hardware flow control is enabled, the logic state of the $\overline{\text{RTSx}}$ pin is controlled by the hardware flow control circuitry. AFCR2 register bit 4 will take the precedence over the other two modes; once this bit is set, the transmitter will control the state of the $\overline{\text{RTSx}}$ pin. The transmitter automatically asserts the $\overline{\text{RTSx}}$ pin (logic 0) once the host writes data to the transmit FIFO, and de-asserts $\overline{\text{RTSx}}$ pin (logic 1) once the last bit of the data has been transmitted.

To use the auto RS-485 $\overline{\text{RTS}}$ mode the software would have to disable the hardware flow control function.

6.14.2 RS-485 $\overline{\text{RTS}}$ inversion

AFCR2[5] reverses the polarity of the $\overline{\text{RTSx}}$ pin if the UART is in auto RS-485 $\overline{\text{RTS}}$ mode.

When the transmitter has data to be sent it will de-asserts the $\overline{\text{RTSx}}$ pin (logic 1), and when the last bit of the data has been sent out the transmitter asserts the $\overline{\text{RTSx}}$ pin (logic 0).

6.14.3 Auto 9-bit mode (RS-485)

AFCR2[0] is used to enable the 9-bit mode (Multi-drop or RS-485 mode). In this mode of operation, a ‘master’ station transmits an address character followed by data characters for the addressed ‘slave’ stations. The slave stations examine the received data and interrupt the controller if the received character is an address character (parity bit = 1).

To use the automatic 9-bit mode, the software would have to disable the hardware and software flow control functions.

6.14.3.1 Normal Multi-drop mode

The 9-bit Mode in AFCR2[0] is enabled, but not Special Character Detect (EFR[5]). The receiver is set to Force Parity 0 (LCR[5:3] = 111) in order to detect address bytes.

With the receiver initially disabled, it ignores all the data bytes (parity bit = 0) until an address byte is received (parity bit = 1). This address byte will cause the UART to set the parity error. The UART will generate a line status interrupt (IER bit 2 must be set to ‘1’ at this time), and at the same time puts this address byte in the RX FIFO. After the controller examines the byte it must make a decision whether or not to enable the receiver; it should enable the receiver if the address byte addresses its ID address, and must not enable the receiver if the address byte does not address its ID address.

If the controller enables the receiver, the receiver will receive the subsequent data until being disabled by the controller after the controller has received a complete message from the ‘master’ station. If the controller does not disable the receiver after receiving a message from the ‘master’ station, the receiver will generate a parity error upon receiving another address byte. The controller then determines if the address byte addresses its ID address, if it is not, the controller then can disable the receiver. If the address byte addresses the ‘slave’ ID address, the controller takes no further action, and the receiver will receive the subsequent data.

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6.14.3.2 Auto address detection

If Special Character Detect is enabled (EFR[5] is set and the Xoff2 register contains the address byte) the receiver will try to detect an address byte that matches the programmed character in the Xoff2 register. If the received byte is a data byte or an address byte that does not match the programmed character in the Xoff2 register, the receiver will discard these data. Upon receiving an address byte that matches the Xoff2 character, the receiver will be automatically enabled if not already enabled, and the address character is pushed into the RX FIFO along with the parity bit (in place of the parity error bit). The receiver also generates a line status interrupt (IER[2] must be set to ‘1’ at this time). The receiver will then receive the subsequent data from the ‘master’ station until being disabled by the controller after having received a message from the ‘master’ station.

If another address byte is received and this address byte does not match the Xoff2 character, the receiver will be automatically disabled and the address byte is ignored. If the address byte matches the Xoff2 character, the receiver will put this byte in the RX FIFO along with the parity bit in the parity error bit (LSR bit 2).

7. Register descriptions

Table 10 details the assigned bit functions for the SC16C852L internal registers. The assigned bit functions are more fully defined in Section 7.1 through Section 7.23.

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Table 10. SC16C852L internal registers

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
General register set[2]													
0	0	0	RHR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
0	0	0	THR	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	W
0	0	1	IER	00	CTS interrupt[3]	RTS interrupt[3]	Xoff interrupt[3]	Sleep mode[3]	modem status interrupt	receive line status interrupt	transmit holding register interrupt	receive holding register interrupt	R/W
0	1	0	FCR	00	RCVR trigger (MSB)	RCVR trigger (LSB)	TX trigger (MSB)[3]	TX trigger (LSB)[3]	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFOs enable	W
0	1	0	ISR	01	FIFOs enabled	FIFOs enabled	INT priority bit 4	INT priority bit 3	INT priority bit 2	INT priority bit 1	INT priority bit 0	INT status	R
0	1	1	LCR	00	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit 1	word length bit 0	R/W
1	0	0	MCR	00	clock select[3]	IRDA enable	reserved	loopback	$\overline{OP2}$/INT enable	($\overline{OP1}$)	$\overline{RTS}$	$\overline{DTR}$	R/W
1	0	1	LSR	60	FIFO data error	THR and TSR empty	THR empty	break interrupt	framing error	parity error	overrun error	receive data ready	R
1	0	1	EFCR	00	reserved	reserved	reserved	reserved	reserved	Enable extra feature bit 1	Enable extra feature bit 0	Enable TXLVLCNT/ RXLVLCNT	W
1	1	0	MSR	X0	CD	RI	DSR	CTS	$\Delta\overline{CD}$	$\Delta\overline{RI}$	$\Delta\overline{DSR}$	$\Delta\overline{CTS}$	R
1	1	1	SPR	FF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
Special register set[4]													
0	0	0	DLL	XX	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
0	0	1	DLM	XX	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
Second special register set[6]													
0	1	1	TXLVLCNT	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R
1	0	0	RXLVLCNT	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R

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Table 10. SC16C852L internal registers *...continued*

A2	A1	A0	Register	Default[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W
Enhanced feature register set[5]													
0	1	0	EFR	00	Auto CTS	Auto RTS	special character select	Enable IER[7:4], ISR[5:4], FCR[5:4], MCR[7:5]	Cont-3 TX, RX Control	Cont-2 TX, RX Control	Cont-1 TX, RX Control	Cont-0 TX, RX Control	R/W
1	0	0	Xon1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	0	1	Xon2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
1	1	0	Xoff1	00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	1	Xoff2	00	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	R/W
First extra feature register set[7]													
0	1	0	TXINTLVL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	0	0	RXINTLVL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	0	FLWCNTH	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	1	FLWCNTL	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
Second extra feature register set[8]													
0	1	0	CLKPRES		reserved	reserved	reserved	reserved	bit 3	bit 2	bit 1	bit 0	R/W
1	0	0	RS485TIME	0x00	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	R/W
1	1	0	AFCR2	0x00	reserved	reserved	RS485 RTS Invert	Auto RS485 RTS	RS485 RTS/DTR	Transmitter Disable	Receiver Disable	9-bit Enable	R/W
1	1	1	AFCR1	0x00	Concurrent Write	reserved	reserved	Sleep RXLow	reserved	RTS/CTS mapped to DTR/DSR	Software Reset	TSR Interrupt	R/W

[1] The value shown represents the register's initialized hexadecimal value; X = not applicable.

[2] Accessible only when LCR[7] is logic 0, and EFCR[2:1] are logic 0.

[3] This bit is only accessible when EFR[4] is set.

[4] Baud rate registers accessible only when LCR[7] is logic 1.

[5] Enhanced feature register, Xon1/Xon2 and Xoff1/Xoff2 are accessible only when LCR is set to 0xBF, and EFCR[2:1] are logic 0.

[6] Second special registers are accessible only when EFCR[0] = 1, and EFCR[2:1] are logic 0.

[7] First extra feature register set is only accessible when EFCR[2:1] = 01b.

[8] Second extra feature register set is only accessible when EFCR[2:1] = 10b.

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7.1 Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7 to D0) to the transmit FIFO. The THR empty flag in the LSR will be set to a logic 1 when the transmit FIFO is empty or when data is transferred to the TSR.

The serial receive section also contains an 8-bit Receive Holding Register (RHR) and a Receive Serial Shift Register (RSR). Receive data is removed from the SC16C852L receive FIFO by reading the RHR. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16× clock rate. After $7\frac{1}{2}$ clocks, the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled, and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

7.2 Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INTA, INTB output pins.

Table 11. Interrupt Enable Register bits description

Bit	Symbol	Description
7	IER[7]	CTS interrupt. logic 0 = disable the CTS interrupt (normal default condition) logic 1 = enable the CTS interrupt. The SC16C852L issues an interrupt when the $\overline{CTSA}$/$\overline{CTSB}$ pin transitions from a logic 0 to a logic 1.
6	IER[6]	RTS interrupt. logic 0 = disable the RTS interrupt (normal default condition) logic 1 = enable the RTS interrupt. The SC16C852L issues an interrupt when the $\overline{RTSA}$/$\overline{RTSB}$ pin transitions from a logic 0 to a logic 1.
5	IER[5]	Xoff interrupt. logic 0 = disable the software flow control, receive Xoff interrupt (normal default condition) logic 1 = enable the receive Xoff interrupt
4	IER[4]	Sleep mode. logic 0 = disable Sleep mode (normal default condition) logic 1 = enable Sleep mode
3	IER[3]	Modem Status Interrupt. This interrupt will be issued whenever there is a modem status change as reflected in MSR[3:0]. logic 0 = disable the modem status register interrupt (normal default condition) logic 1 = enable the modem status register interrupt
2	IER[2]	Receive Line Status interrupt. This interrupt will be issued whenever a receive data error condition exists as reflected in LSR[4:1]. logic 0 = disable the receiver line status interrupt (normal default condition) logic 1 = enable the receiver line status interrupt

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Table 11. Interrupt Enable Register bits description *...continued*

Bit	Symbol	Description
1	IER[1]	Transmit Holding Register interrupt. In the non-FIFO mode, this interrupt will be issued whenever the THR is empty, and is associated with LSR[5]. In the FIFO modes, this interrupt will be issued whenever the FIFO is empty. logic 0 = disable the Transmit Holding Register Empty (TXRDY) interrupt (normal default condition) logic 1 = enable the TXRDY (ISR level 3) interrupt
0	IER[0]	Receive Holding Register interrupt. In the non-FIFO mode, this interrupt will be issued when the RHR has data, or is cleared when the RHR is empty. In the FIFO mode, this interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level. logic 0 = disable the receiver ready (ISR level 2, RXRDY) interrupt (normal default condition) logic 1 = enable the RXRDY (ISR level 2) interrupt

7.2.1 IER versus Transmit/Receive FIFO interrupt mode operation

When the receive FIFO is enabled (FCR[0] = logic 1), and receive interrupts (IER[0] = logic 1) are enabled, the receive interrupts and register status will reflect the following:

- The receive RXRDY interrupt (Level 2 ISR interrupt) is issued to the external CPU when the receive FIFO has reached the programmed trigger level. It will be cleared when the receive FIFO drops below the programmed trigger level.
- Receive FIFO status will also be reflected in the user accessible ISR register when the receive FIFO trigger level is reached. Both the ISR register receive status bit and the interrupt will be cleared when the FIFO drops below the trigger level.
- The receive data ready bit (LSR[0]) is set as soon as a character is transferred from the shift register (RSR) to the receive FIFO. It is reset when the FIFO is empty.
- When the Transmit FIFO and interrupts are enabled, an interrupt is generated when the transmit FIFO is empty due to the unloading of the data by the TSR and UART for transmission via the transmission media. The interrupt is cleared either by reading the ISR, or by loading the THR with new data characters.

7.2.2 IER versus Receive/Transmit FIFO polled mode operation

When FCR[0] = logic 1, setting IER[3:0] puts the SC16C852L in the FIFO polled mode of operation. In this mode, interrupts are not generated and the user must poll the LSR register for TX and/or RX data status. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

- LSR[0] will be a logic 1 as long as there is one byte in the receive FIFO.
- LSR[4:1] will provide the type of receive errors, or a receive break, if encountered.
- LSR[5] will indicate when the transmit FIFO is empty.
- LSR[6] will indicate when both the transmit FIFO and transmit shift register are empty.
- LSR[7] will show if any FIFO data errors occurred.

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7.3 FIFO Control Register (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receive FIFO trigger levels, and select the DMA mode.

7.3.1 DMA mode

7.3.1.1 Mode 0 (FCR bit 3 = 0)

In this mode, Transmit Ready ($\overline{TXRDY}$) will go to a logic 0 whenever the FIFO (THR, if FIFO is not enabled) is empty. Receive Ready ($\overline{RXRDY}$) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.

7.3.1.2 Mode 1 (FCR bit 3 = 1)

In this mode, the Transmit Ready ($\overline{TXRDY}$) is set when the transmit FIFO is below the programmed trigger level. The Receive Ready ($\overline{RXRDY}$) is set when the receive FIFO fills to the programmed trigger level. However, the FIFO continues to fill regardless of the programmed level until the FIFO is full. $\overline{RXRDY}$ remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

7.3.2 FIFO mode

Table 12. FIFO Control Register bits description

Bit	Symbol	Description
7:6	FCR[7:6]	Receive trigger level in 32-byte FIFO mode[1]. These bits are used to set the trigger levels for receive FIFO interrupt and flow control. The SC16C852L will issue a receive ready interrupt when the number of characters in the receive FIFO reaches the selected trigger level. Refer to Table 13.
5:4	FCR[5:4]	Transmit trigger level in 32-byte FIFO mode[2]. These bits are used to set the trigger level for the transmit FIFO interrupt and flow control. The SC16C852L will issue a transmit empty interrupt when the number of characters in FIFO drops below the selected trigger level. Refer to Table 14.
3	FCR[3]	DMA mode select. logic 0 = set DMA mode ‘0’ (normal default condition) logic 1 = set DMA mode ‘1’ **Transmit operation in mode ‘0’:** When the SC16C852L is in the non-FIFO mode (FIFOs disabled; FCR[0] = logic 0) or in the FIFO mode (FIFOs enabled; FCR[0] = logic 1; FCR[3] = logic 0), and when there are no characters in the transmit FIFO, the $\overline{TXRDYA}$/$\overline{TXRDYB}$ pin will be a logic 0. Once active, the $\overline{TXRDYA}$/$\overline{TXRDYB}$ pin will go to a logic 1 after the first character is loaded into the transmit holding register. **Receive operation in mode ‘0’:** When the SC16C852L is in non-FIFO mode, or in the FIFO mode (FCR[0] = logic 1; FCR[3] = logic 0) and there is at least one character in the receive FIFO, the $\overline{RXRDYA}$/$\overline{RXRDYB}$ pin will be a logic 0. Once active, the $\overline{RXRDYA}$/$\overline{RXRDYB}$ pin will go to a logic 1 when there are no more characters in the receiver.

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Table 12. FIFO Control Register bits description *...continued*

Bit	Symbol	Description
3 (cont.)		**Transmit operation in mode '1':** When the SC16C852L is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1), the $\overline{TXRDYA}$/$\overline{TXRDYB}$ pin will be a logic 1 when the transmit FIFO is completely full; see Section 6.10 "DMA operation". It will be a logic 0 when the trigger level has been reached. **Receive operation in mode '1':** When the SC16C852L is in FIFO mode (FCR[0] = logic 1; FCR[3] = logic 1) and the trigger level has been reached, or a Receive Time-Out has occurred, the $\overline{RXRDYA}$/$\overline{RXRDYB}$ pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.
2	FCR[2]	XMIT FIFO reset. logic 0 = no FIFO transmit reset (normal default condition) logic 1 = clears the contents of the transmit FIFO and resets the FIFO counter logic. This bit will return to a logic 0 after clearing the FIFO.
1	FCR[1]	RCVR FIFO reset. logic 0 = no FIFO receive reset (normal default condition) logic 1 = clears the contents of the receive FIFO and resets the FIFO counter logic. This bit will return to a logic 0 after clearing the FIFO.
0	FCR[0]	FIFO enable. logic 0 = disable the transmit and receive FIFO (normal default condition) logic 1 = enable the transmit and receive FIFO

[1] For 128-byte FIFO mode, refer to Section 7.16, Section 7.17, Section 7.18.

[2] For 128-byte FIFO mode, refer to Section 7.15, Section 7.17, Section 7.18.

Table 13. RCVR trigger levels

FCR[7]	FCR[6]	RX FIFO trigger level (bytes) in 32-byte FIFO mode[1]
0	0	8
0	1	16
1	0	24
1	1	28

[1] When RXINTLVL, TXINTLVL, FLWCNTL or FLWCNTH contains any value other than 0x00, receive and transmit trigger levels are set by RXINTLVL, TXINTLVL registers (see Section 6.4 "FIFO operation").

Table 14. TX FIFO trigger levels

FCR[5]	FCR[4]	TX FIFO trigger level (bytes) in 32-byte FIFO mode[1]
0	0	16
0	1	8
1	0	24
1	1	30

[1] When RXINTLVL, TXINTLVL, FLWCNTL or FLWCNTH contains any value other than 0x00, receive and transmit trigger levels are set by RXINTLVL, TXINTLVL registers (see Section 6.4 "FIFO operation").

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7.4 Interrupt Status Register (ISR)

The SC16C852L provides six levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. A lower level interrupt may be seen after servicing the higher level interrupt and re-reading the interrupt status bits. Table 15 “Interrupt source” shows the data values (bits 5:0) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

Table 15. Interrupt source

Priority level	ISR[5]	ISR[4]	ISR[3]	ISR[2]	ISR[1]	ISR[0]	Source of the interrupt
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
2	0	0	1	1	0	0	RXRDY (Receive Data time-out)
3	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	0	0	MSR (Modem Status Register)
5	0	1	0	0	0	0	RXRDY (Received Xoff signal)/ Special character
6	1	0	0	0	0	0	CTS, RTS change of state

Table 16. Interrupt Status Register bits description

Bit	Symbol	Description
7:6	ISR[7:6]	FIFOs enabled. These bits are set to a logic 0 when the FIFOs are not being used in the non-FIFO mode. They are set to a logic 1 when the FIFOs are enabled in the SC16C852L mode. logic 0 or cleared = default condition
5:4	ISR[5:4]	INT priority bits 4:3. These bits are enabled when EFR[4] is set to a logic 1. ISR[4] indicates that matching Xoff character(s) have been detected. ISR[5] indicates that CTS, RTS have been generated. Note that once set to a logic 1, the ISR[4] bit will stay a logic 1 until Xon character(s) are received. logic 0 or cleared = default condition
3:1	ISR[3:1]	INT priority bits 2:0. These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (see Table 15). logic 0 or cleared = default condition
0	ISR[0]	INT status. logic 0 = an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine logic 1 = no interrupt pending (normal default condition)

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7.5 Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

Table 17. Line Control Register bits description

Bit	Symbol	Description
7	LCR[7]	Divisor latch enable. The internal baud rate counter latch and Enhanced Feature mode enable. logic 0 = divisor latch disabled (normal default condition) logic 1 = divisor latch enabled
6	LCR[6]	Set break. When enabled, the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR[6] to a logic 0. logic 0 = no TX break condition (normal default condition) logic 1 = forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition
5:3	LCR[5:3]	Programs the parity conditions (see Table 18).
2	LCR[2]	Stop bits. The length of stop bit is specified by this bit in conjunction with the programmed word length (see Table 19). logic 0 or cleared = default condition
1:0	LCR[1:0]	Word length bits 1, 0. These two bits specify the word length to be transmitted or received (see Table 20). logic 0 or cleared = default condition

Table 18. LCR[5:3] parity selection

LCR[5]	LCR[4]	LCR[3]	Parity selection
X	X	0	no parity
X	0	1	odd parity
0	1	1	even parity
0	0	1	forced parity ‘1’
1	1	1	forced parity ‘0’

Table 19. LCR[2] stop bit length

LCR[2]	Word length (bits)	Stop bit length (bit times)
0	5, 6, 7, 8	1
1	5	1½
1	6, 7, 8	2

Table 20. LCR[1:0] word length

LCR[1]	LCR[0]	Word length (bits)
0	0	5
0	1	6
1	0	7
1	1	8

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7.6 Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

Table 21. Modem Control Register bits description

Bit	Symbol	Description
7	MCR[7]	Clock select logic 0 = divide-by-1 clock input logic 1 = divide-by-4 clock input
6	MCR[6]	IR enable (see Figure 31). logic 0 = enable the standard modem receive and transmit input/output interface (normal default condition) logic 1 = enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/inputs are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode, the infrared TX output will be a logic 0 during idle data conditions.
5	MCR[5]	Reserved; set to ‘0’.
4	MCR[4]	Loopback. Enable the local loopback mode (diagnostics). In this mode the transmitter output (TXA/TXB) and the receiver input (RXA/RXB), $\overline{CTS}$, $\overline{DSR}$, $\overline{CD}$, and $\overline{RI}$ are disconnected from the SC16C852L I/O pins. Internally the modem data and control pins are connected into a loopback data configuration (see Figure 10). In this mode, the receiver and transmitter interrupts remain fully operational. The Modem Control Interrupts are also operational, but the interrupts’ sources are switched to the lower four bits of the Modem Control. Interrupts continue to be controlled by the IER register. logic 0 = disable Loopback mode (normal default condition) logic 1 = enable local Loopback mode (diagnostics)
3	MCR[3]	$\overline{OP2A}$/$\overline{OP2B}$, INT enable logic 0 = forces INTA/INTB outputs to the 3-state mode and sets $\overline{OP2A}$/$\overline{OP2B}$ to a logic 1 (normal default condition) logic 1 = forces the INTA/INTB outputs to the active mode and sets $\overline{OP2A}$/$\overline{OP2B}$ to a logic 0 **Remark:** $\overline{OP2A}$/$\overline{OP2B}$ pins do not exist on the HVQFN32 package.
2	MCR[2]	$\overline{OP1A}$/$\overline{OP1B}$ are not available as an external signal in the SC16C852L. This bit is instead used in the Loopback mode only. In the Loopback mode, this bit is used to write the state of the modem $\overline{RI}$ interface signal.
1	MCR[1]	$\overline{RTS}$ logic 0 = force $\overline{RTSx}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{RTSx}$ output to a logic 0
0	MCR[0]	$\overline{DTR}$ logic 0 = force $\overline{DTRx}$ output to a logic 1 (normal default condition) logic 1 = force $\overline{DTRx}$ output to a logic 0

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7.7 Line Status Register (LSR)

This register provides the status of data transfers between the SC16C852L and the CPU.

Table 22. Line Status Register bits description

Bit	Symbol	Description
7	LSR[7]	FIFO data error. logic 0 = no error (normal default condition) logic 1 = at least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when there are no remaining error flags associated with the remaining data in the FIFO.
6	LSR[6]	THR and TSR empty. This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode, this bit is set to ‘1’ whenever the transmit FIFO and transmit shift register are both empty.
5	LSR[5]	THR empty. This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to a logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode, this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.
4	LSR[4]	Break interrupt. logic 0 = no break condition (normal default condition) logic 1 = the receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.
3	LSR[3]	Framing error. logic 0 = no framing error (normal default condition) logic 1 = framing error. The receive character did not have a valid stop bit(s). In the FIFO mode, this error is associated with the character at the top of the FIFO.
2	LSR[2]	Parity error. logic 0 = no parity error (normal default condition) logic 1 = parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.
1	LSR[1]	Overrun error. logic 0 = no overrun error (normal default condition) logic 1 = overrun error. A data overrun error occurred in the Receive Shift Register. This happens when additional data arrives while the FIFO is full. In this case, the previous data in the shift register is overwritten. Note that under this condition, the data byte in the Receive Shift Register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.
0	LSR[0]	Receive data ready. logic 0 = no data in Receive Holding Register or FIFO (normal default condition) logic 1 = data has been received and is saved in the Receive Holding Register or FIFO

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7.8 Modem Status Register (MSR)

This register shares the same address as EFCR register. This is a read-only register and it provides the current state of the control interface signals from the modem, or other peripheral device to which the SC16C852L is connected. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

When write, the data will be written to EFCR register.

Table 23. Modem Status Register bits description

Bit	Symbol	Description
7	MSR[7]	CD. During normal operation, this bit is the complement of the $\overline{CDx}$ input. Reading this bit in the loopback mode produces the state of MCR[3].
6	MSR[6]	RI. During normal operation, this bit is the complement of the $\overline{RIx}$ input. Reading this bit in the loopback mode produces the state of MCR[2].
5	MSR[5]	DSR. During normal operation, this bit is the complement of the $\overline{DSRx}$ input. During the loopback mode, this bit is equivalent to MCR[0].
4	MSR[4]	CTS. During normal operation, this bit is the complement of the $\overline{CTSx}$ input. During the loopback mode, this bit is equivalent to MCR[1].
3	MSR[3]	$\Delta\overline{CD}$ [1] logic 0 = no $\overline{CDx}$ change (normal default condition) logic 1 = the $\overline{CDx}$ input to the SC16C852L has changed state since the last time it was read. A modem Status Interrupt will be generated.
2	MSR[2]	$\Delta\overline{RI}$ [1] logic 0 = no $\overline{RIx}$ change (normal default condition) logic 1 = the $\overline{RIx}$ input to the SC16C852L has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.
1	MSR[1]	$\Delta\overline{DSR}$ [1] logic 0 = no $\overline{DSRx}$ change (normal default condition) logic 1 = the $\overline{DSRx}$ input to the SC16C852L has changed state since the last time it was read. A modem Status Interrupt will be generated.
0	MSR[0]	$\Delta\overline{CTS}$ [1] logic 0 = no $\overline{CTSx}$ change (normal default condition) logic 1 = the $\overline{CTSx}$ input to the SC16C852L has changed state since the last time it was read. A modem Status Interrupt will be generated.

[1] Whenever any MSR bit 3:0 is set to logic 1, a Modem Status Interrupt will be generated.

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7.9 Extra Feature Control Register (EFCR)

This is a write-only register, and it allows the software access to these registers: first extra feature register set, second extra feature register set, Transmit FIFO Level Counter (TXLVLCNT), and Receive FIFO Level Counter (RXLVLCNT).

Table 24. Extra Feature Control Register bits description

Bit	Symbol	Description
7:3	EFCR[7:3]	reserved
2:1	EFCR[2:1]	Enable Extra Feature Control bits 00 = General register set is accessible 01 = First extra feature register set is accessible 10 = Second extra feature register set is accessible 11 = reserved
0	EFCR[0]	Enable TXLVLCNT and RXLVLCNT access 0 = TXLVLCNT and RXLVLCNT are disabled 1 = TXLVLCNT and RXLVLCNT are enabled and can be read.

Remark: EFCR[2:1] has higher priority than EFCR[0]. TXLVLCNT and RXLVLCNT can only be accessed if EFCR[2:1] are zeroes.

7.10 Scratchpad Register (SPR)

The SC16C852L provides a temporary data register to store 8 bits of user information.

7.11 Division Latch (DLL and DLM)

These are two 8-bit registers which store the 16-bit divisor for generation of the baud clock in the baud rate generator. DLM, stores the most significant part of the divisor. DLL stores the least significant part of the division.

7.12 Transmit FIFO Level Count (TXLVLCNT)

This register is a read-only register. It reports the number of spaces available in the transmit FIFO.

7.13 Receive FIFO Level Count (RXLVLCNT)

This register is a read-only register. It reports the fill level of the receive FIFO (the number of characters in the RX FIFO).

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7.14 Enhanced Feature Register (EFR)

Enhanced features are enabled or disabled using this register.

Bits 0 through 4 provide single or dual character software flow control selection. When the Xon1 and Xon2 and/or Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential numbers.

Table 25. Enhanced Feature Register bits description

Bit	Symbol	Description
7	EFR[7]	Automatic CTS flow control. logic 0 = automatic CTS flow control is disabled (normal default condition) logic 1 = enable automatic CTS flow control. Transmission will stop when $\overline{CTS}$ goes to a logical 1. Transmission will resume when the $\overline{CTSA}$/$\overline{CTSB}$ pin returns to a logical 0.
6	EFR[6]	Automatic RTS flow control. Automatic RTS may be used for hardware flow control by enabling EFR[6]. When Auto-RTS is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and $\overline{RTS}$ will go to a logic 1 at the next trigger level. $\overline{RTS}$ will return to a logic 0 when data is unloaded below the next lower trigger level (programmed trigger level 1). The state of this register bit changes with the status of the hardware flow control. $\overline{RTS}$ functions normally when hardware flow control is disabled. logic 0 = automatic RTS flow control is disabled (normal default condition) logic 1 = enable automatic RTS flow control
5	EFR[5]	Special Character Detect. logic 0 = special character detect disabled (normal default condition) logic 1 = special character detect enabled. The SC16C852L compares each incoming receive character with Xoff2 data. If a match exists, the received data will be transferred to FIFO and ISR[4] will be set to indicate detection of special character. Bit-0 in the X-registers corresponds with the LSB bit for the receive character. When this feature is enabled, the normal software flow control must be disabled (EFR[3:0] must be set to a logic 0).
4	EFR[4]	Enhanced function control bit. The content of IER[7:4], ISR[5:4], FCR[5:4], and MCR[7:5] can be modified and latched. After modifying any bits in the enhanced registers, EFR[4] can be set to a logic 0 to latch the new values. This feature prevents existing software from altering or overwriting the SC16C852L enhanced functions. logic 0 = disable/latch enhanced features[1]. (Normal default condition.) logic 1 = enables the enhanced functions[1].
3:0	EFR[3:0]	Cont-3:0 TX, RX control. Logic 0 or cleared is the default condition. Combinations of software flow control can be selected by programming these bits. See Table 26.

[1] Enhanced function control bits IER[7:4], ISR[5:4], FCR[5:4] and MCR[7:5].

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Table 26. Software flow control functions[1]

Cont-3	Cont-2	Cont-1	Cont-0	TX, RX software flow controls
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1/Xoff1
0	1	X	X	Transmit Xon2/Xoff2
1	1	X	X	Transmit Xon1 and Xon2/Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1/Xoff1
X	X	0	1	Receiver compares Xon2/Xoff2
1	0	1	1	Transmit Xon1/Xoff1
				Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2/Xoff2
				Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2
				Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

[1] When using a software flow control the Xon/Xoff characters cannot be used for data transfer.

7.15 Transmit Interrupt Level register (TXINTLVL)

This 8-bit register is used to store the transmit FIFO trigger levels used for DMA and interrupt generation. Trigger levels from 1 to 128 can be programmed with a granularity of 1. Table 27 shows TXINTLVL register bit settings.

Table 27. TXINTLVL register bits description

Bit	Symbol	Description
7:0	TXINTLVL[7:0]	This register stores the programmable transmit interrupt trigger levels for 128-byte FIFO mode[1]. 0x00 = trigger level is set to 1 0x01 = trigger level is set to 1 ... 0x80 = trigger level is set to 128

[1] For 32-byte FIFO mode, refer to Section 7.3.

7.16 Receive Interrupt Level register (RXINTLVL)

This 8-bit register is used to store the receive FIFO trigger levels used for DMA and interrupt generation. Trigger levels from 1 to 128 can be programmed with a granularity of 1. Table 28 shows RXINTLVL register bit settings.

Table 28. RXINTLVL register bits description

Bit	Symbol	Description
7:0	RXINTLVL[7:0]	This register stores the programmable receive interrupt trigger levels for 128-byte FIFO mode[1]. 0x00 = trigger level is set to 1 0x01 = trigger level is set to 1 ... 0x80 = trigger level is set to 128

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[1] For 32-byte FIFO mode, refer to Section 7.3.

7.17 Flow Control Trigger Level High (FLWCNTH)

This 8-bit register is used to store the receive FIFO high threshold levels to start/stop transmission during hardware/software flow control. Table 29 shows FLWCNTH register bit settings; see Section 6.5.

Table 29. FLWCNTH register bits description

Bit	Symbol	Description
7:0	FLWCNTH[7:0]	This register stores the programmable HIGH threshold level for hardware and software flow control for 128-byte FIFO mode[1]. 0x00 = trigger level is set to 1 0x01 = trigger level is set to 1 ... 0x80 = trigger level is set to 128

[1] For 32-byte FIFO mode, refer to Section 7.3.

7.18 Flow Control Trigger Level Low (FLWCNTL)

This 8-bit register is used to store the receive FIFO low threshold levels to start/stop transmission during hardware/software flow control. Table 30 shows FLWCNTL register bit settings; see Section 6.5.

Table 30. FLWCNTL register bits description

Bit	Symbol	Description
7:0	FLWCNTL[7:0]	This register stores the programmable LOW threshold level for hardware and software flow control for 128-byte FIFO mode[1]. 0x00 = trigger level is set to 1 0x01 = trigger level is set to 1 ... 0x80 = trigger level is set to 128

[1] For 32-byte FIFO mode, refer to Section 7.3.

7.19 Clock Prescaler (CLKPRES)

This register hold values for the clock prescaler.

Table 31. Clock Prescaler register bits description

Bit	Symbol	Description
7:4	CLKPRES[7:4]	reserved
3:0	CLKPRES[3:0]	Clock Prescaler value. Reset to 0.

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7.20 RS-485 turn-around time delay (RS485TIME)

The value in this register controls the turn-around time of the external line transceiver in bit time. In automatic 9-bit mode $\overline{RTSA}$/$\overline{RTSB}$ or $\overline{DTRA}$/$\overline{DTRB}$ pin is used to control the direction of the line driver, after the last bit of data has been shifted out of the transmit shift register the UART will count down the value in this register. When the count value reaches zero, the UART will assert $\overline{RTSA}$/$\overline{RTSB}$ or $\overline{DTRA}$/$\overline{DTRB}$ pin (logic 0) to turn the external RS-485 transceiver around for receiving.

Table 32. RS-485 programmable turn-around time register bits description

Bit	Symbol	Description
7:0	RS485TIME[7:0]	External RS-485 transceiver turn-around time delay. The value represents the bit time at the programmed baud rate.

7.21 Advanced Feature Control Register 2 (AFCR2)

Table 33. Advanced Feature Control Register 2 register bits description

Bit	Symbol	Description
7:6	AFCR2[7:6]	reserved
5	AFCR2[5]	RTSInvert. Invert RTS or DTR signal in automatic 9-bit mode. logic logic 0 = RTS or DTR is set to 0 by the UART during transmission, and to 1 during reception logic 1 = RTS or DTR is set to 1 by the UART during transmission, and to 0 during reception
4	AFCR2[4]	RTSCon. Enable the transmitter to control $\overline{RTSx}$ or $\overline{DTRx}$ pin in automatic 9-bit mode. logic logic 0 = transmitter does not control $\overline{RTSx}$ or $\overline{DTRx}$ pin logic 1 = transmitter controls $\overline{RTSx}$ or $\overline{DTRx}$ pin
3	AFCR2[3]	RS485 RTS/DTR. Select $\overline{RTSx}$ or $\overline{DTRx}$ pin to control the external transceiver. logic logic 0 = $\overline{RTSx}$ pin is used to control the external transceiver logic 1 = $\overline{DTRx}$ pin is used to control the external transceiver
2	AFCR2[2]	TXDisable. Disable transmitter logic 0 = transmitter is enabled logic 1 = transmitter is disable
1	AFCR2[1]	RXDisable. Disable receiver logic 0 = receiver is enabled logic 1 = receiver is disable
0	AFCR2[0]	9-bitMode. Enable 9-bit mode or Multidrop (RS-485) mode logic logic 0 = normal RS-232 mode logic 1 = enable 9-bit mode

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7.22 Advanced Feature Control Register 1 (AFCR1)

Table 34. Advanced Feature Control Register 1 register bits description

Bit	Symbol	Description
7	AFCR1[7]	Concurrent write. When this bit is set the host can write concurrently to the same register of all channel. logic logic 0 = Normal operation logic 1 = Concurrent Write operation
6:5	AFCR1[6:5]	reserved
4	AFCR1[4]	Sleep RXLow. Program RX input to be edge-sensitive or level-sensitive. logic 0 = RX input is level-sensitive. If RXA/RXB pin is LOW, the UART will not go to sleep. Once the UART is in Sleep mode, it will wake up if RXA/RXB pin goes LOW. logic 1 = RX input is edge-sensitive. UART will go to sleep even if RXA/RXB pin is LOW, and will wake up when RXA/RXB pin toggles.
3	AFCR1[3]	reserved
2	AFCR1[2]	RTS/CTS mapped to DTR/DSR. Switch the function of RTS/CTS to DTR/DSR. logic 0 = RTS and CTS signals are used for hardware flow control. logic 1 = DTR and DSR signals are used for hardware flow control. RTS and CTS retain their functionality.
1	AFCR1[1]	SReset. Software Reset A write to this bit will reset the UART. Once the UART is reset this bit is automatically set to 0.[1]
0	AFCR1[0]	TSR Interrupt. Select TSR interrupt mode logic 0 = transmit empty interrupt occurs when transmit FIFO falls below the trigger level or becomes empty. logic 1 = transmit empty interrupt occurs when transmit FIFO falls below the trigger level, or becomes empty and the last stop bit has been shifted out of the Transmit Shift Register.

[1] It takes 4 XTAL1 clocks to reset the device.

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7.23 SC16C852L external reset condition and software reset

These two reset methods are identical and will reset the internal registers as indicated in Table 35.

Table 35. Reset state for registers

Register	Reset state
IER	IER[7:0] = 0
FCR	FCR[7:0] = 0
ISR	ISR[7:1] = 0; ISR[0] = 1
LCR	LCR[7:0] = 0
MCR	MCR[7:0] = 0
LSR	LSR[7] = 0; LSR[6:5] = 1; LSR[4:0] = 0
MSR	MSR[7:4] = input signals; MSR[3:0] = 0
EFCR	EFCR[7:0] = 0
SPR	SPR[7:0] = 1
DLL	undefined
DLM	undefined
TXLVLCNT	TXLVLCNT[7:0] = 0
RXLVLCNT	RXLVLCNT[7:0] = 0
EFR	EFR[7:0] = 0
Xon1	undefined
Xon2	undefined
Xoff1	undefined
Xoff2	undefined
TXINTLVL	TXINTLVL[7:0] = 0
RXINTLVL	RXINTLVL[7:0] = 0
FLWCNTH	FLWCNTH[7:0] = 0
FLWCNTL	FLWCNTL[7:0] = 0
CLKPRES	CLKPRES[7:0] = 0
RS485TIME	RS485TIME[7:0] = 0
AFCR2	AFCR2[7:0] = 0
AFCR1	AFCR1[7:0] = 0

Table 36. Reset state for outputs

Output	Reset state
TXA, TXB	logic 1
$\overline{OP2A}$, $\overline{OP2B}$	logic 1
$\overline{RTSA}$, $\overline{RTSB}$	logic 1
$\overline{DTRA}$, $\overline{DTRB}$	logic 1
INTA, INTB	3-state condition

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8. Limiting values

Table 37. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-	2.5	V
V_n	voltage on any other pin		[1]	V_{SS} – 0.3	V_{DD} + 0.3	V
T_{amb}	ambient temperature	operating in free air		–40	+85	°C
T_{stg}	storage temperature			–65	+150	°C
P_{tot}/pack	total power dissipation per package			-	500	mW

[1] V_n should not exceed 2.5 V.

9. Static characteristics

Table 38. Static characteristics

T_{amb} = –40 °C to +85 °C; V_{DD} = 1.65 V to 1.95 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{IL(clk)}$	LOW-level clock input voltage	XTAL1 pin		-	-	0.25	V
$V_{IH(clk)}$	HIGH-level clock input voltage	XTAL1 pin		1.35	-	-	V
V_{IL}	LOW-level input voltage	except XTAL1 clock, LOWPWR pin		-	-	0.45	V
		LOWPWR pin	[1]	-	-	0.45	V
V_{IH}	HIGH-level input voltage	except XTAL1 clock, LOWPWR pin		1.35	-	-	V
		LOWPWR pin	[1]	1.35	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	[2]	-	-	0.35	V
V_{OH}	HIGH-level output voltage	I_{OH} = –800 μA	[2]	1.45	-	-	V
I_{LIL}	LOW-level input leakage current			-	-	1	μA
I_{LIH}	HIGH-level input leakage current			-	-	1	μA
$I_{L(clk)}$	clock leakage current	LOW-level		-	-	30	μA
		HIGH-level		-	-	30	μA
I_{DD}	supply current	f = 5 MHz		-	-	2	mA
$I_{DD(sleep)}$	sleep mode supply current		[3]	-	-	5	μA
$I_{DD(lp)}$	low-power mode supply current		[4]	-	-	5	μA
C_i	input capacitance			-	-	5	pF

[1] Hysteresis input.

[2] Except XTAL2.

[3] Sleep current might be higher if there is any activity on the UART data bus during Sleep mode.

[4] Activate by LOWPWR pin.

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10. Dynamic characteristics

Table 39. Dynamic characteristics - Intel or 16 mode

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 1.95 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WH}	pulse width HIGH			6	-	-	ns
t_{WL}	pulse width LOW			6	-	-	ns
$t_{w(clk)}$	clock pulse width			12.5	-	-	ns
f_{XTAL1}	frequency on pin XTAL1		[1][2]	-	-	80	MHz
$t_{su(A)}$	address setup time			0	-	-	ns
$t_{h(A)}$	address hold time			10	-	-	ns
$t_{d(CS-IOR)}$	delay time from $\overline{CS}$ to $\overline{IOR}$			5	-	-	ns
$t_{d(IOW-TXRDYH)}$	delay time from $\overline{IOW}$ to $\overline{TXRDY}$ HIGH			-	-	50	ns
$t_{d(IOR-RXRDYH)}$	delay time from $\overline{IOR}$ to $\overline{RXRDY}$ HIGH			-	-	50	ns
$t_{d(stop-RXRDY)}$	delay time from stop to $\overline{RXRDY}$		[4]	-	-	$1T_{RCLK}$	s
$t_{d(start-TXRDY)}$	delay time from start to $\overline{TXRDY}$		[4]	-	-	$8T_{RCLK}$	s
$t_{w(IOR)}$	$\overline{IOR}$ pulse width time			20	-	-	ns
$t_{h(IOR-CS)}$	hold time from $\overline{IOR}$ to chip select			0	-	-	ns
$t_{d(IOR)}$	$\overline{IOR}$ delay time			10	-	-	ns
$t_{d(IOR-Q)}$	delay time from $\overline{IOR}$ to data output	25 pF load		-	-	40	ns
$t_{dis(IOR-QZ)}$	disable time from $\overline{IOR}$ to high-impedance data output[3]	25 pF load		-	-	20	ns
$t_{d(CSL-IOWL)}$	delay time from $\overline{CS}$ LOW to $\overline{IOW}$ LOW			5	-	-	ns
$t_{w(IOW)}$	$\overline{IOW}$ pulse width time			10	-	-	ns
$t_{h(IOW-CS)}$	hold time from $\overline{IOW}$ to $\overline{CS}$			0	-	-	ns
$t_{d(IOW)}$	$\overline{IOW}$ delay time			10	-	-	ns
$t_{su(D-IOWH)}$	setup time from data input to $\overline{IOW}$ HIGH			5	-	-	ns
$t_{h(IOWH-D)}$	data input hold time after $\overline{IOW}$ HIGH			5	-	-	ns
$t_{d(IOW-Q)}$	delay time from $\overline{IOW}$ to data output	25 pF load		-	-	50	ns
$t_{d(modem-INT)}$	delay time from modem to INT	25 pF load		-	-	50	ns
$t_{d(IOR-INTL)}$	delay time from $\overline{IOR}$ to INT LOW	25 pF load		-	-	50	ns
$t_{d(stop-INT)}$	delay time from stop to INT	25 pF load	[4]	-	-	$1T_{RCLK}$	s
$t_{d(start-INT)}$	delay time from start to INT	25 pF load		-	-	$1T_{RCLK}$	s
$t_{d(IOW-TX)}$	delay time from $\overline{IOW}$ to TX	25 pF load	[4]	$8T_{RCLK}$	-	$24T_{RCLK}$	s
$t_{d(IOW-INTL)}$	delay time from $\overline{IOW}$ to INT LOW	25 pF load		-	-	50	ns
$t_{w(RESET)}$	pulse width on pin RESET			10	-	-	ns
N	baud rate divisor			1	-	$(2^{16} - 1)$	

[1] Applies to external clock, crystal oscillator max 24 MHz.

[2] Maximum frequency = $\frac{1}{t_{w(clk)}}$

[3] 10 % of the data bus output voltage level.

[4] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

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Table 40. Dynamic characteristics - Motorola or 68 mode

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.65 V to 1.95 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WH}	pulse width HIGH			6	-	-	ns
t_{WL}	pulse width LOW			6	-	-	ns
$t_{w(clk)}$	clock pulse width			12.5	-	-	ns
f_{XTAL1}	frequency on pin XTAL1		[1][2]	-	-	80	MHz
$t_{su(A)}$	address setup time			5	-	-	ns
$t_{h(A)}$	address hold time			10	-	-	ns
$t_{su(RWL-CSL)}$	set-up time from R/$\overline{W}$ LOW to $\overline{CS}$ LOW			10	-	-	ns
$t_{su(RWH-CSL)}$	set-up time from R/$\overline{W}$ HIGH to $\overline{CS}$ LOW			10	-	-	ns
$t_{d(stop-RXRDY)}$	delay time from stop to $\overline{RXRDY}$		[3]	-	-	$1T_{RCLK}$	s
$t_{d(start-TXRDY)}$	delay time from start to $\overline{TXRDY}$		[3]	-	-	$8T_{RCLK}$	s
$t_{w(CS)}$	$\overline{CS}$ pulse width	25 pF load		20	-	-	ns
$t_{d(CS)}$	$\overline{CS}$ delay time	25 pF load		10	-	-	ns
$t_{d(CS-Q)}$	delay time from $\overline{CS}$ to data output	25 pF load		-	-	40	ns
$t_{dis(CS-QZ)}$	disable time from $\overline{CS}$ to high-impedance data output	25 pF load		-	-	20	ns
$t_{h(CS-RWH)}$	hold time from $\overline{CS}$ to R/$\overline{W}$ HIGH			5	-	-	ns
$t_{d(RW)}$	R/$\overline{W}$ delay time			10	-	-	ns
$t_{su(D-CSH)}$	set-up time from data input to $\overline{CS}$ HIGH			5	-	-	ns
$t_{h(CSH-D)}$	data input hold time after $\overline{CS}$ HIGH			5	-	-	ns
$t_{d(modem-IRQL)}$	delay time from modem to $\overline{IRQ}$ LOW			-	-	50	ns
$t_{d(CS-IRQH)R}$	read delay time from $\overline{CS}$ to $\overline{IRQ}$ HIGH			-	-	50	ns
$t_{d(stop-IRQL)}$	delay time from stop to $\overline{IRQ}$ LOW		[3]	-	-	$1T_{RCLK}$	s
$t_{d(CS-RXRDYH)R}$	read delay time from $\overline{CS}$ to $\overline{RXRDY}$ HIGH			-	-	50	ns
$t_{d(CS-TX)W}$	write delay time from $\overline{CS}$ to TX		[3]	$8T_{RCLK}$	-	$24T_{RCLK}$	s
$t_{d(start-IRQL)}$	delay time from start to $\overline{IRQ}$ LOW		[3]	-	-	$1T_{RCLK}$	s
$t_{d(CS-IRQH)W}$	write delay time from $\overline{CS}$ to $\overline{IRQ}$ HIGH			-	-	50	ns
$t_{d(CS-TXRDYH)W}$	write delay time from $\overline{CS}$ to $\overline{TXRDY}$ HIGH			-	-	50	ns
$t_{d(CS-Q)W}$	write delay time from $\overline{CS}$ to data output			-	-	50	ns
$t_{w(RESET_N)}$	pulse width on pin $\overline{RESET}$			10	-	-	ns
N	baud rate divisor			1	-	$(2^{16} - 1)$	

[1] Applies to external clock, crystal oscillator max 24 MHz.

[2] Maximum frequency = $\frac{1}{t_{w(clk)}}$

[3] RCLK is an internal signal derived from Divisor Latch LSB (DLL) and Divisor Latch MSB (DLM) divisor latches.

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10.1 Timing diagrams

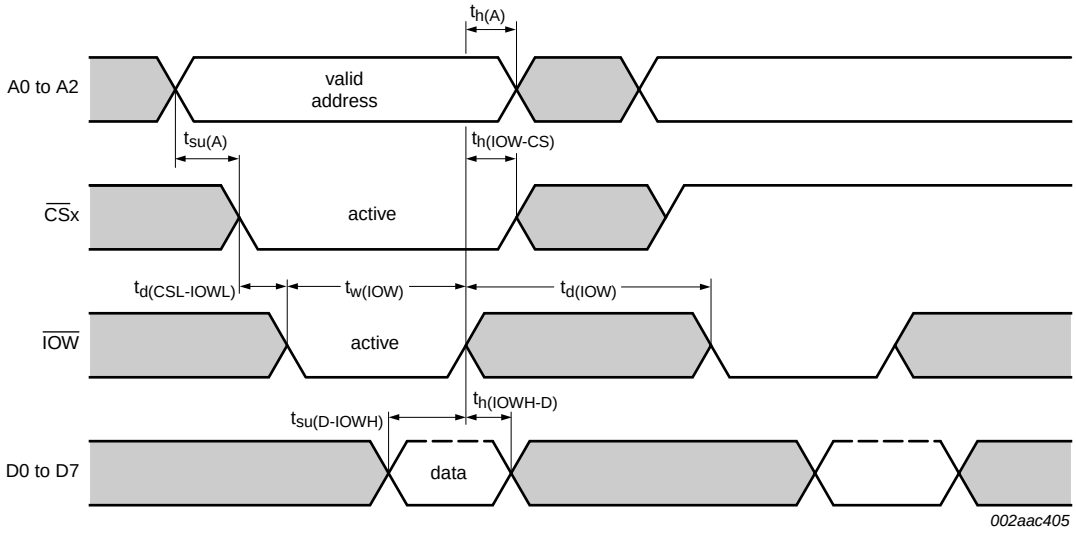

Fig 11. General write timing in 16 mode

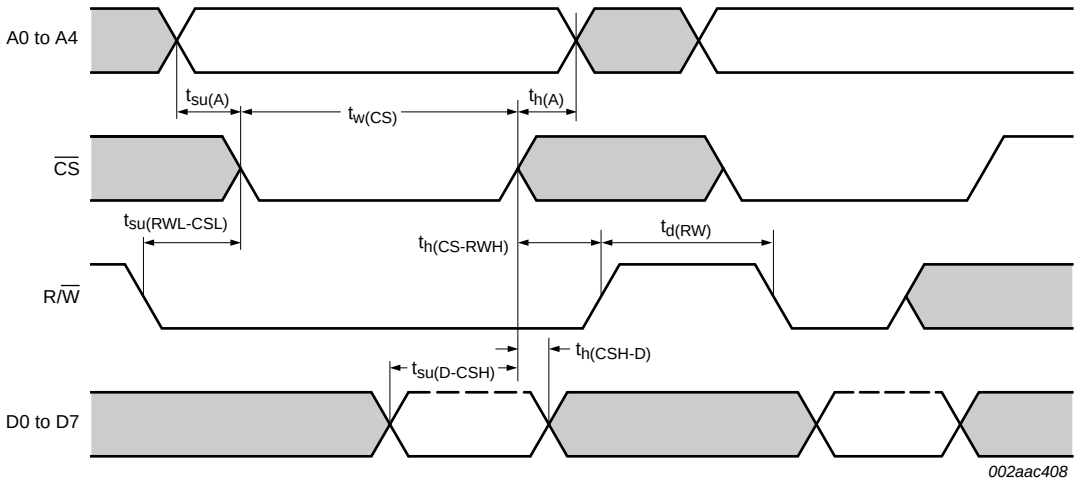

Fig 12. General write timing in 68 mode

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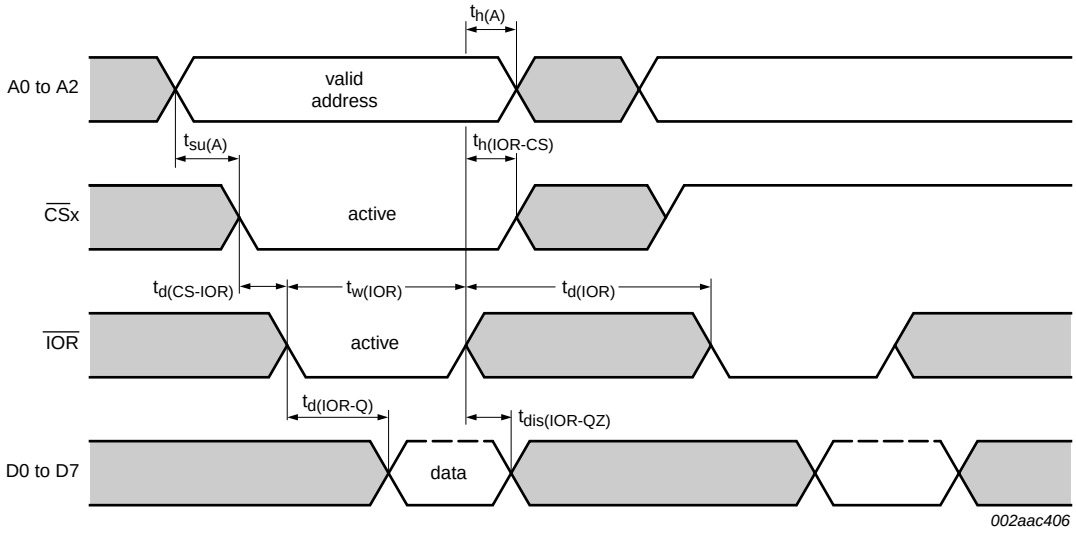


Fig 13. General read timing in 16 mode

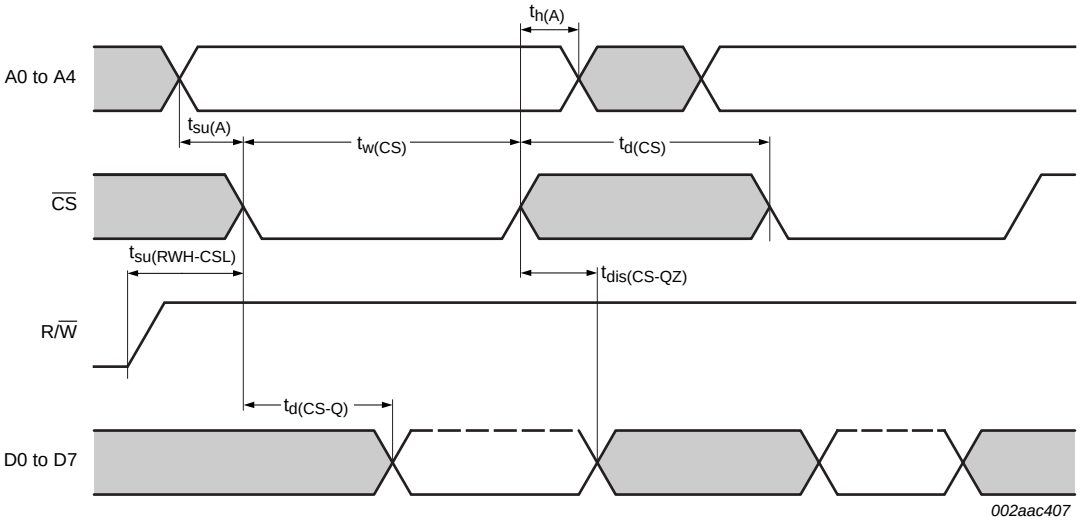
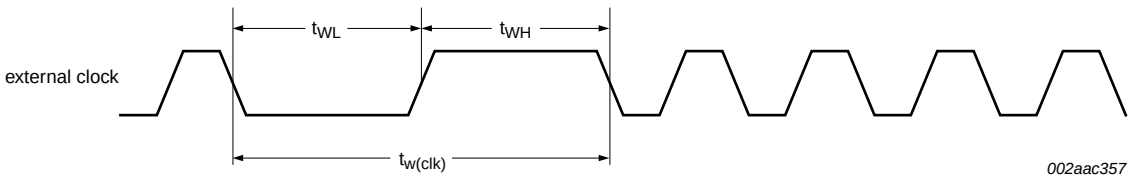


Fig 14. General read timing in 68 mode



$$f_{XTAL1} = \frac{1}{t_{w(clk)}}$$

Fig 15. External clock timing

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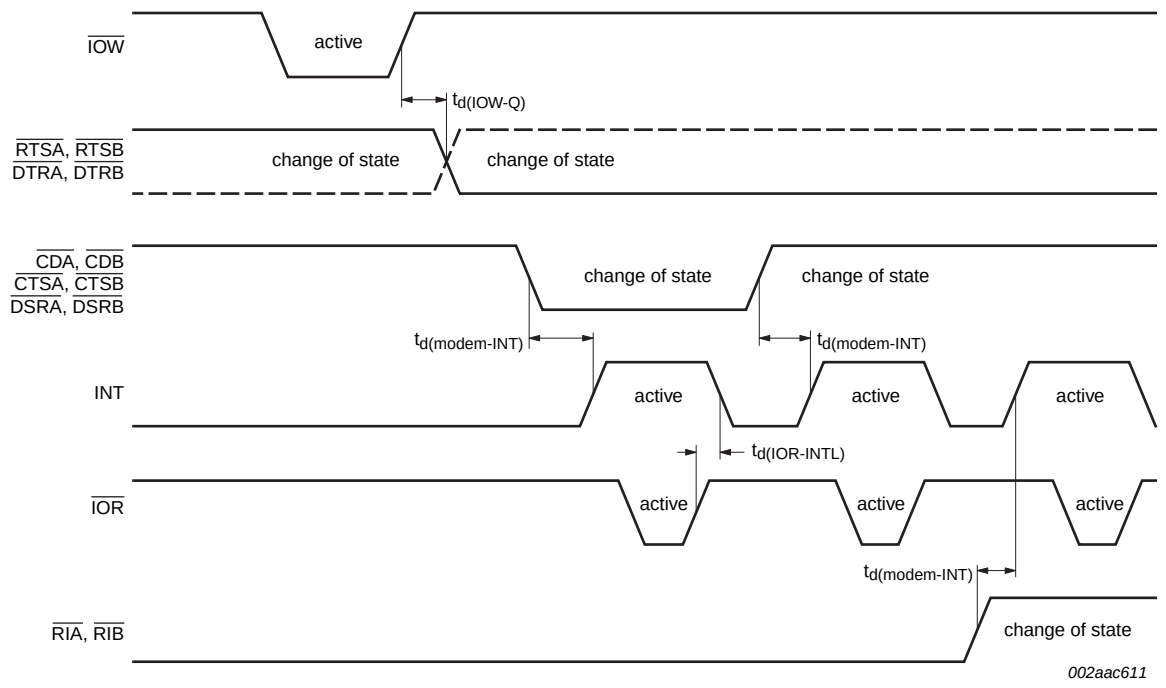
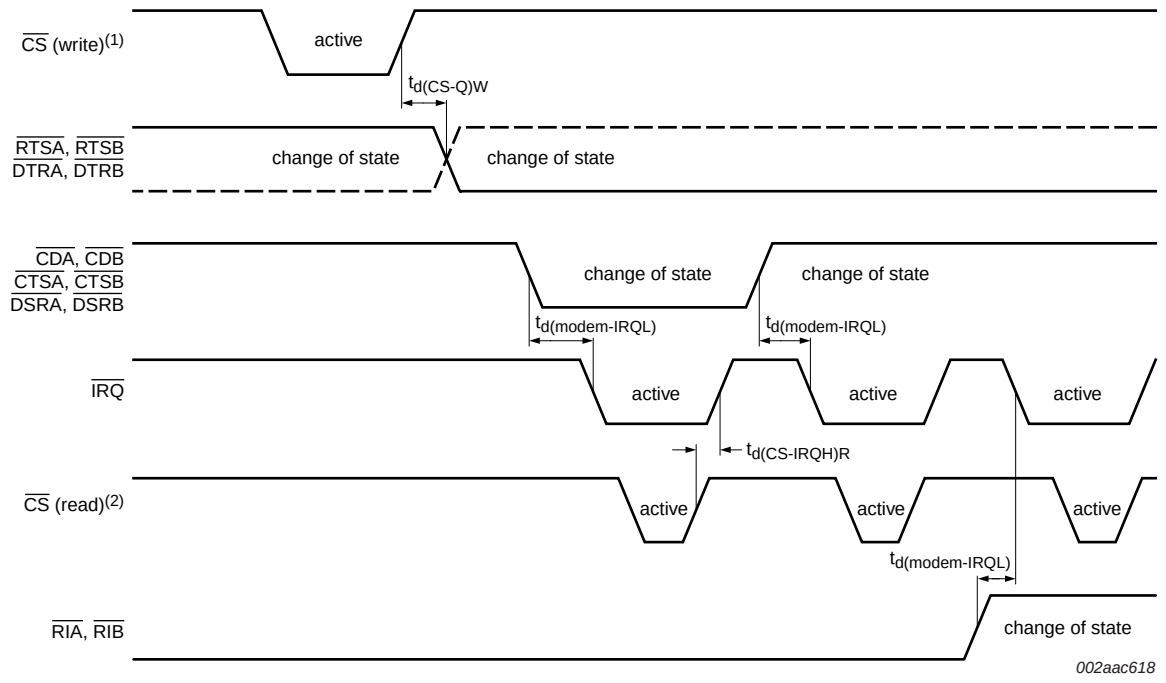


Fig 16. Modem input/output timing in 16 mode



(1) $\overline{CS}$ timing during a write cycle. See Figure 12.

(2) $\overline{CS}$ timing during a read cycle. See Figure 14.

Fig 17. Modem input/output timing in 68 mode

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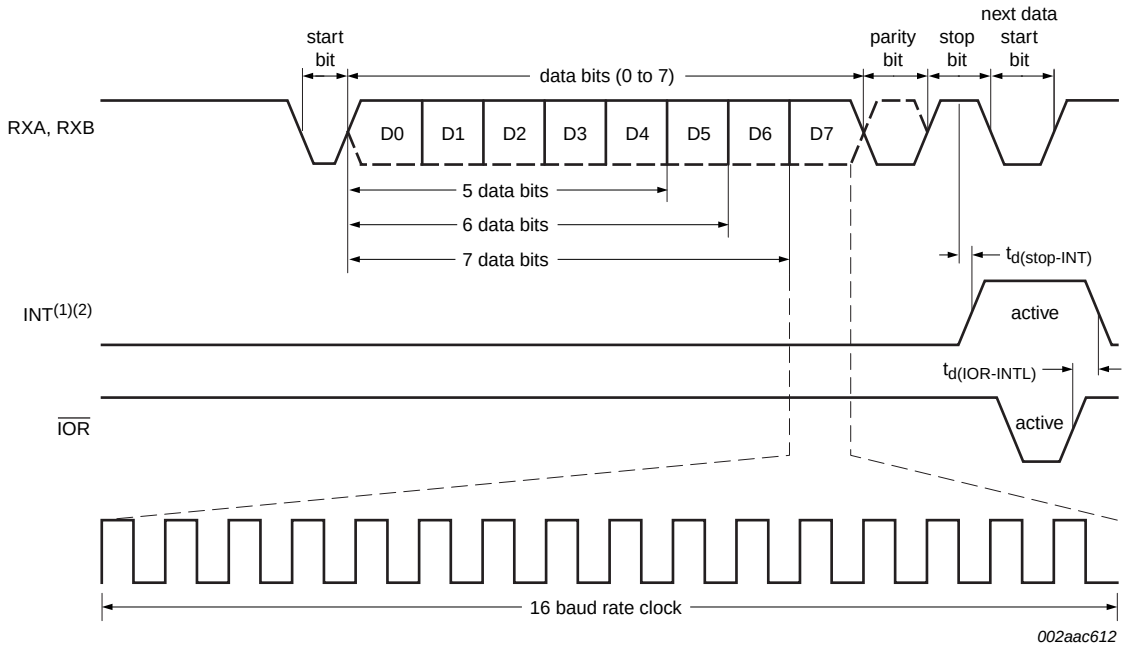
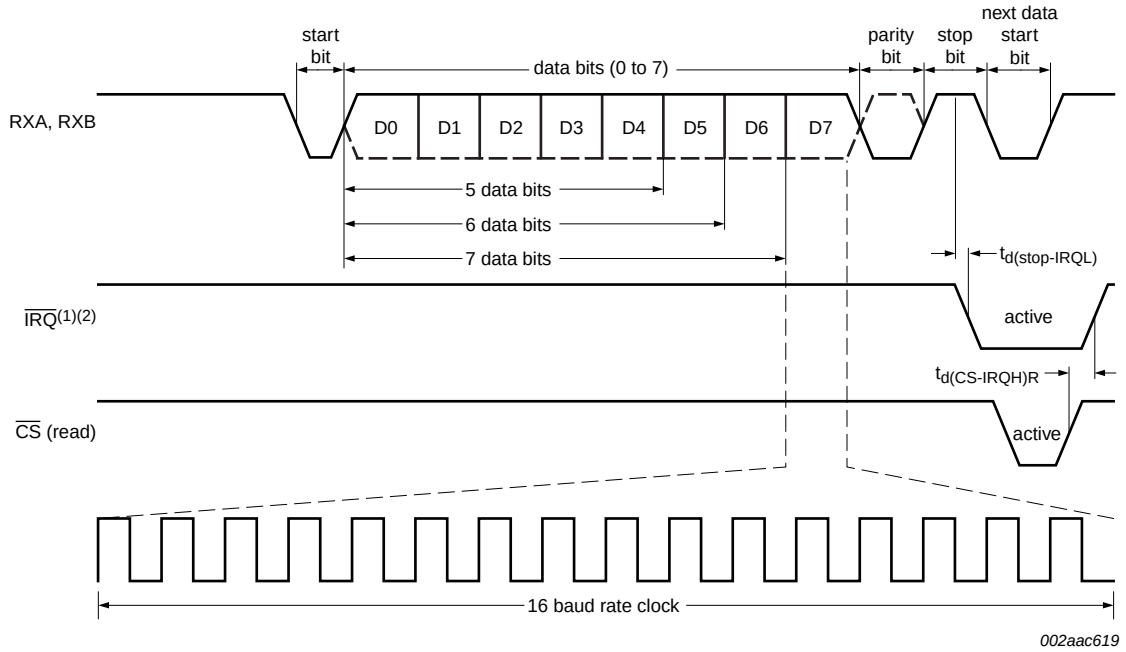


(1) INT is active when RX FIFO fills up to trigger level or a time-out condition happens (see Section 6.8).

(2) INT is cleared when RX FIFO drops below trigger level.

Fig 18. Receive timing in 16 mode



(1) $\overline{IRQ}$ is active when RX FIFO fills up to trigger level or time-out condition happens (see Section 6.8).

(2) $\overline{IRQ}$ is cleared when RX FIFO drops below trigger level.

Fig 19. Receive timing in 68 mode

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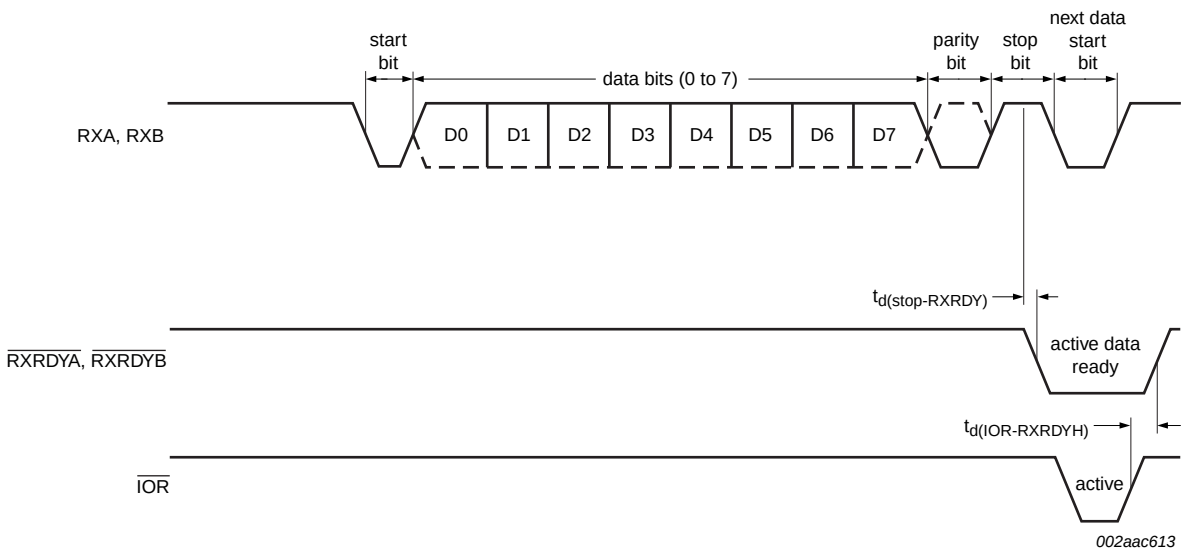

Fig 20. Receive ready timing in non-FIFO mode (16 mode)

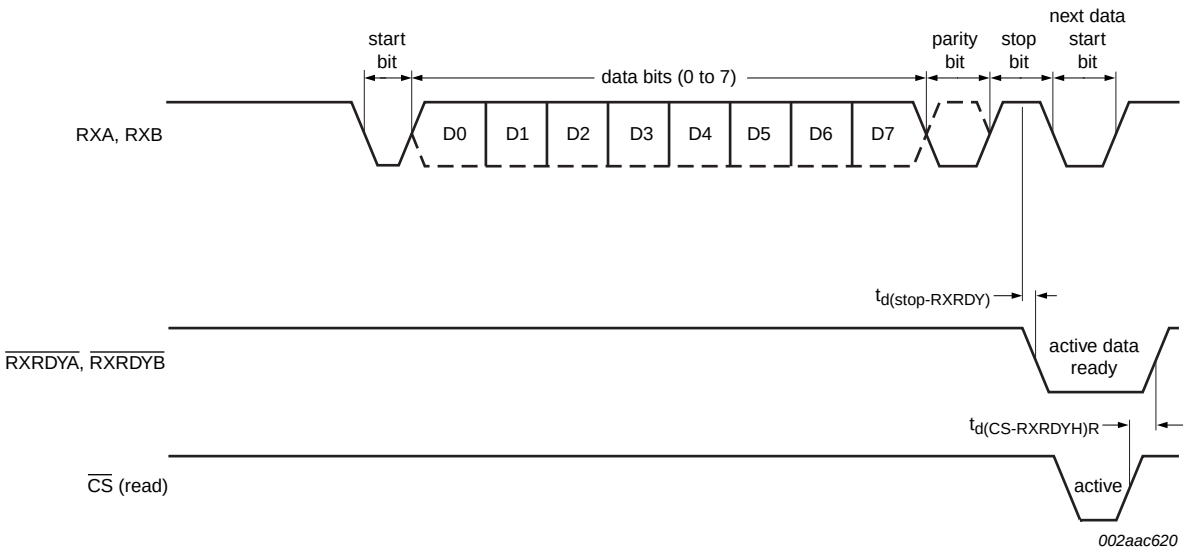

Fig 21. Receive ready timing in non-FIFO mode (68 mode)

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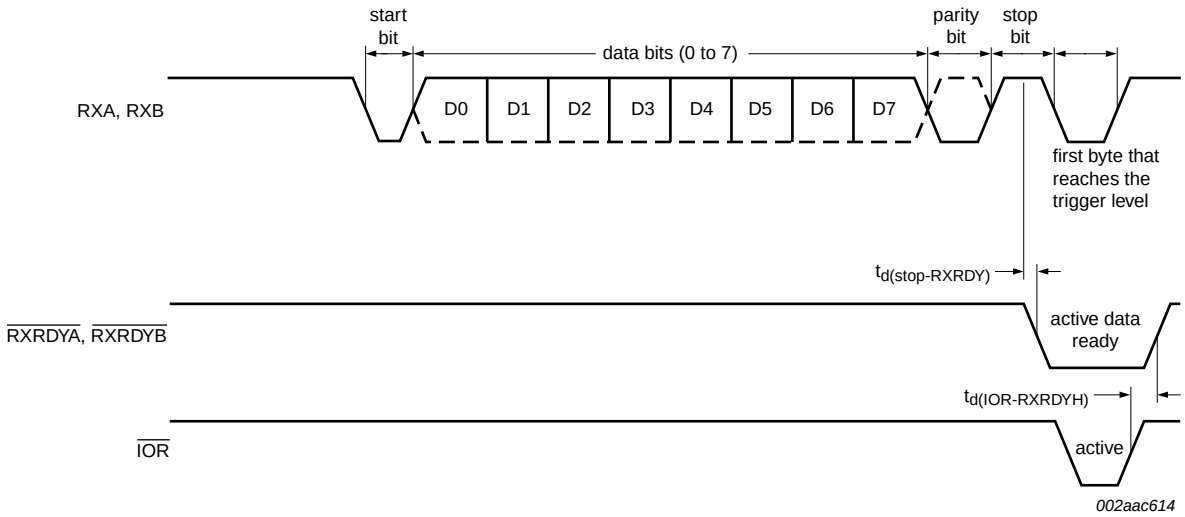

Fig 22. Receive ready timing in FIFO mode (16 mode)

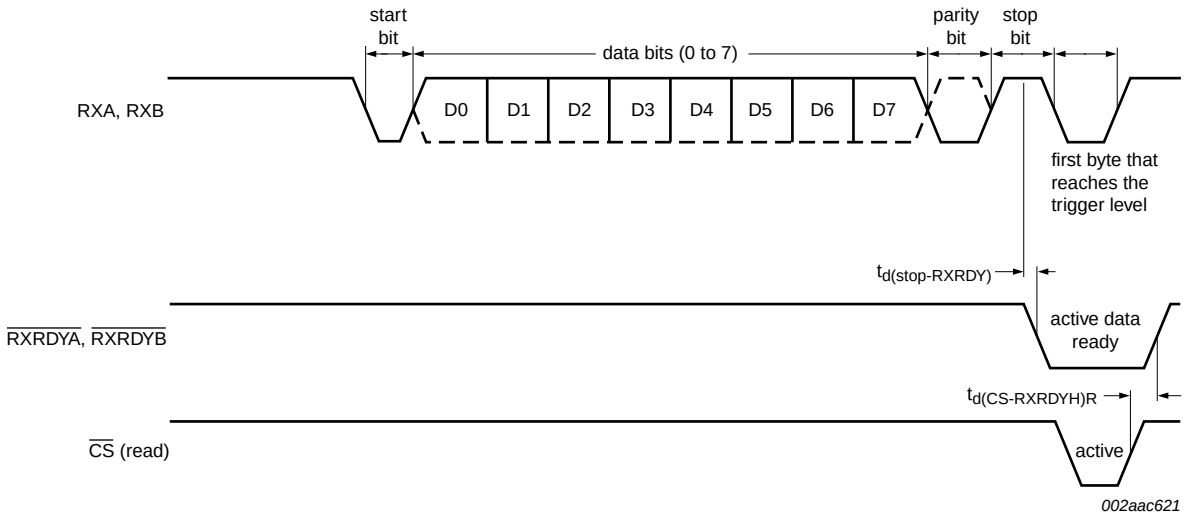

Fig 23. Receive ready timing in FIFO mode (68 mode)

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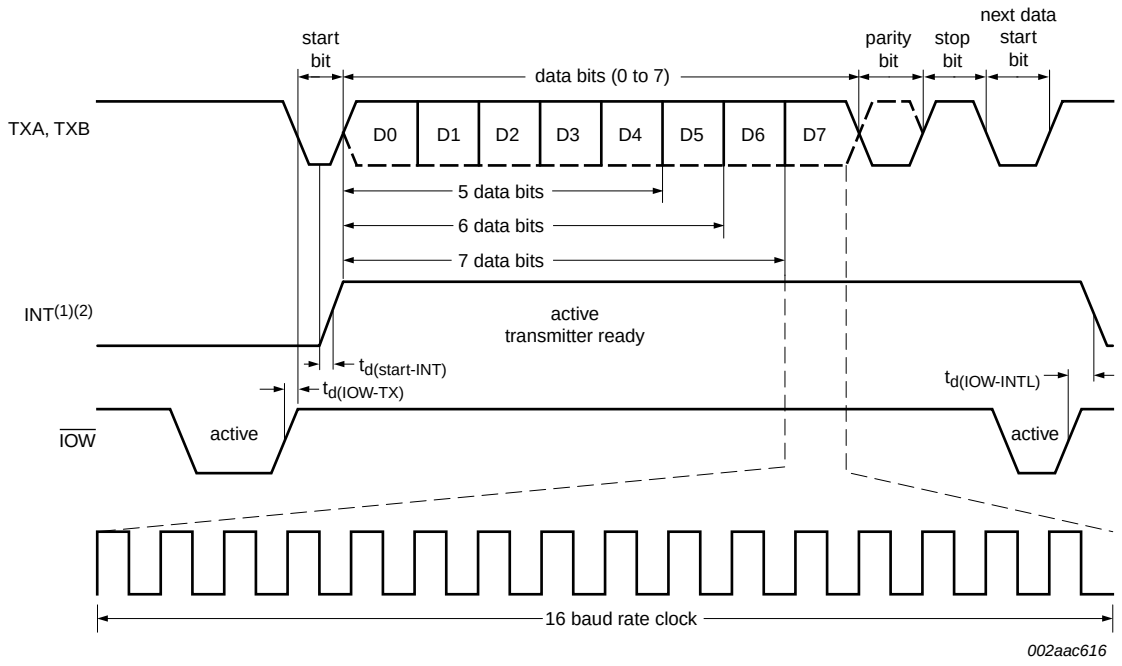
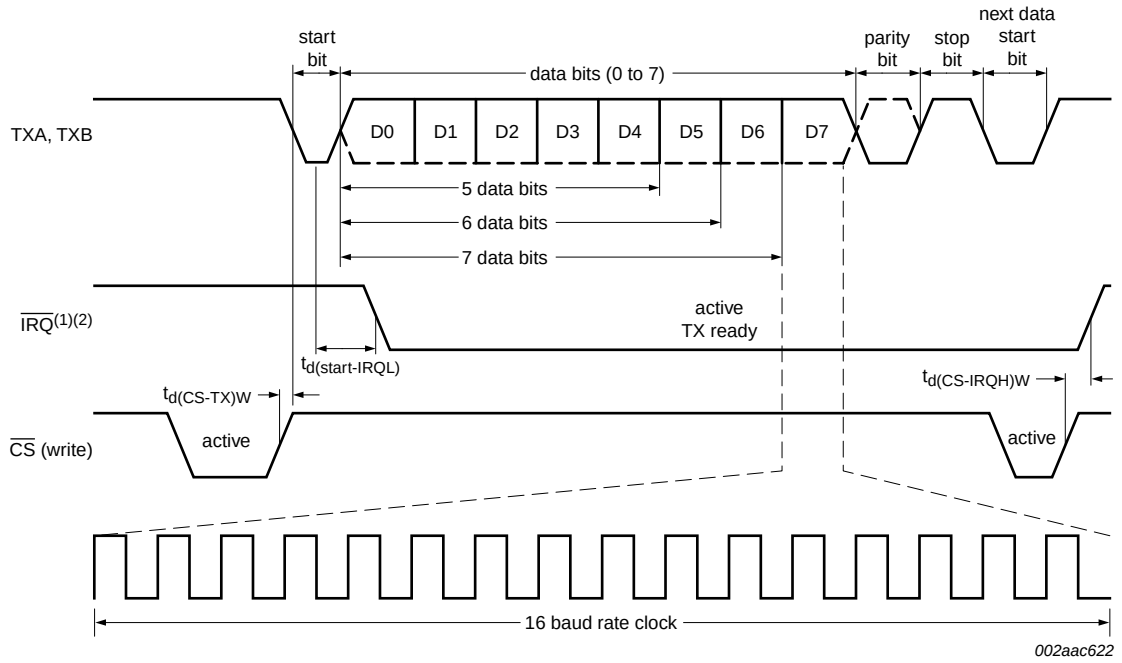


(1) INT is active when TX FIFO is empty or TX FIFO drops below trigger level.

(2) INT is cleared when ISR is read or TX FIFO fills up to trigger level.

Fig 24. Transmit timing in 16 mode



(1) $\overline{IRQ}$ is active when TX FIFO is empty or TX FIFO drops below trigger level.

(2) $\overline{IRQ}$ is cleared when ISR is read or TX FIFO fills up to trigger level.

Fig 25. Transmit timing in 68 mode

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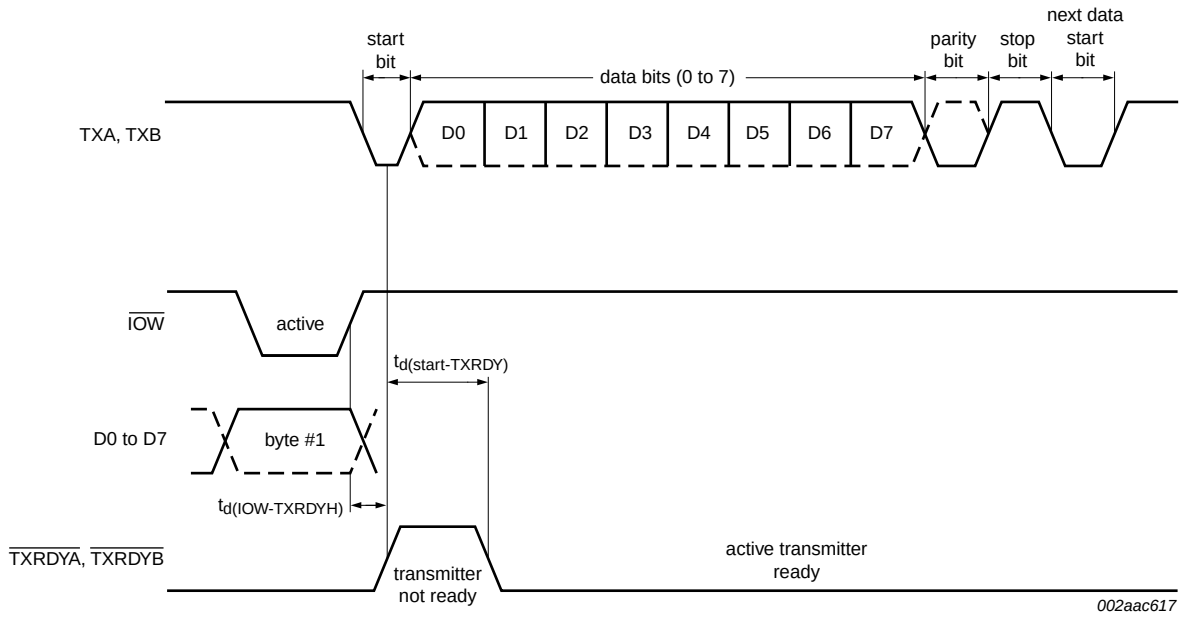

Fig 26. Transmit ready timing in non-FIFO mode (16 mode)

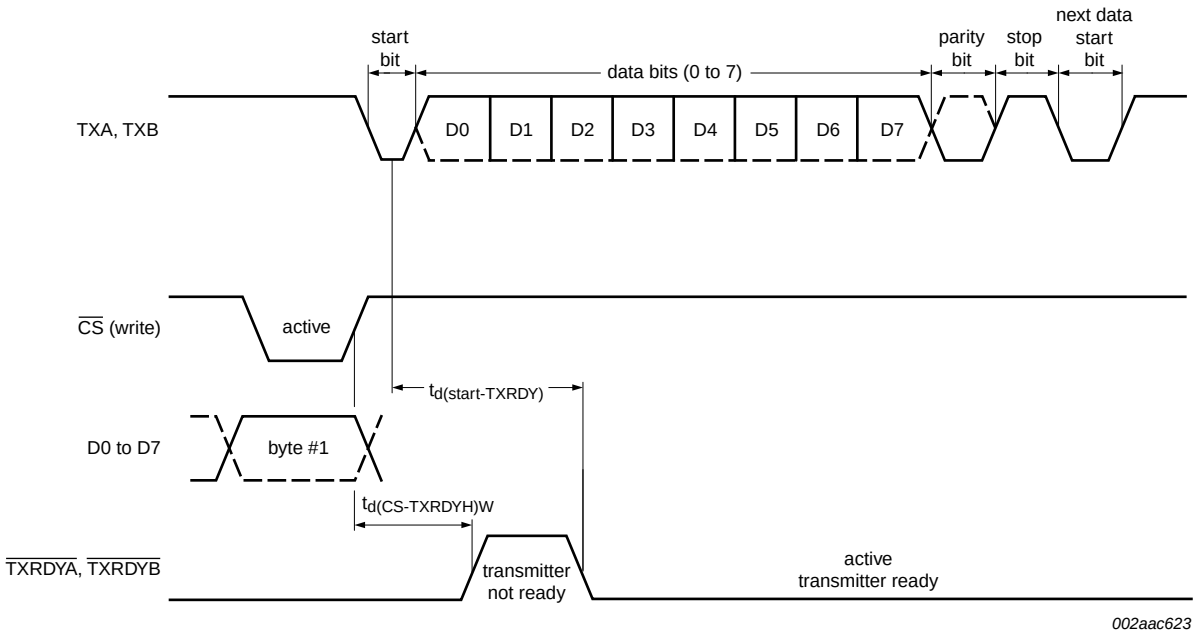

Fig 27. Transmit ready timing in non-FIFO mode (68 mode)

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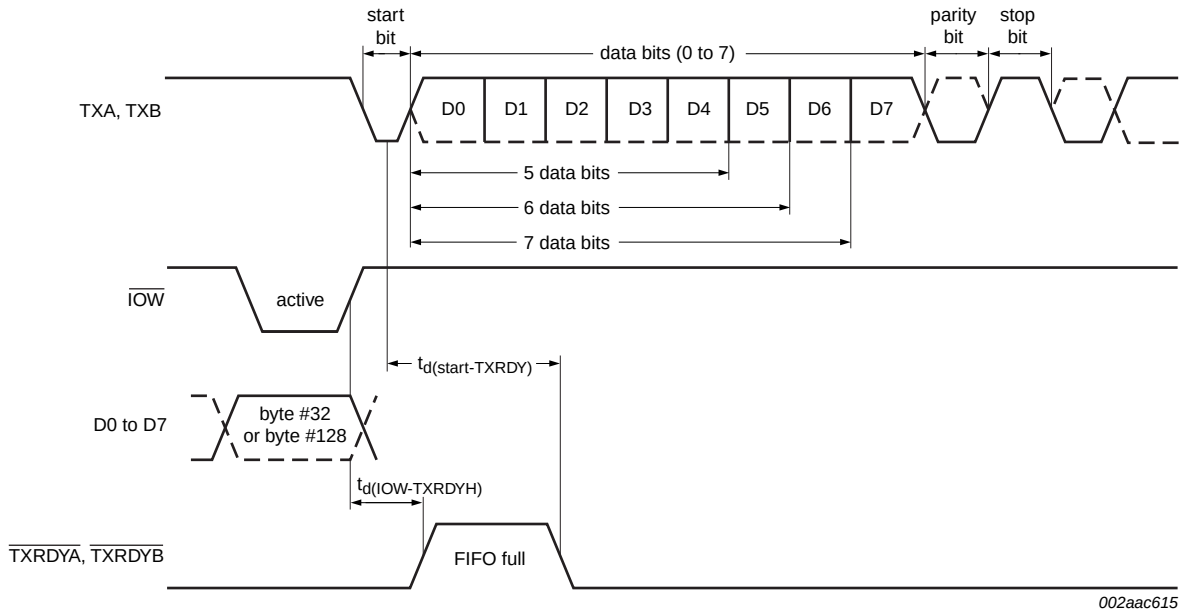

Fig 28. Transmit ready timing in FIFO mode (DMA mode '1') in 16 mode

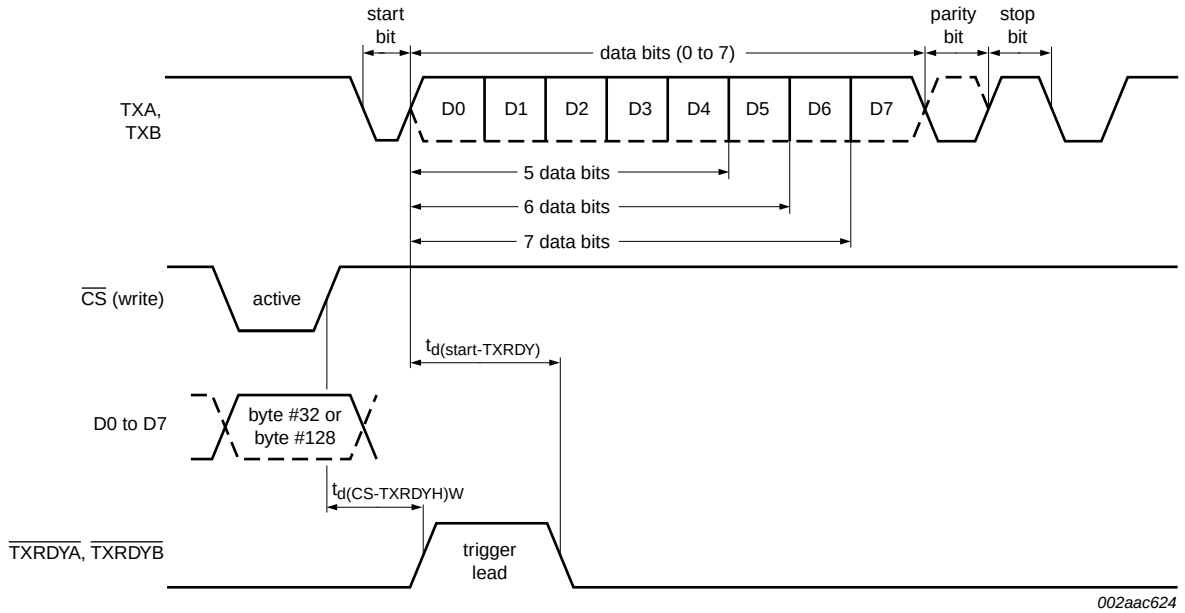

Fig 29. Transmit ready timing in FIFO mode (DMA mode '1') in 68 mode

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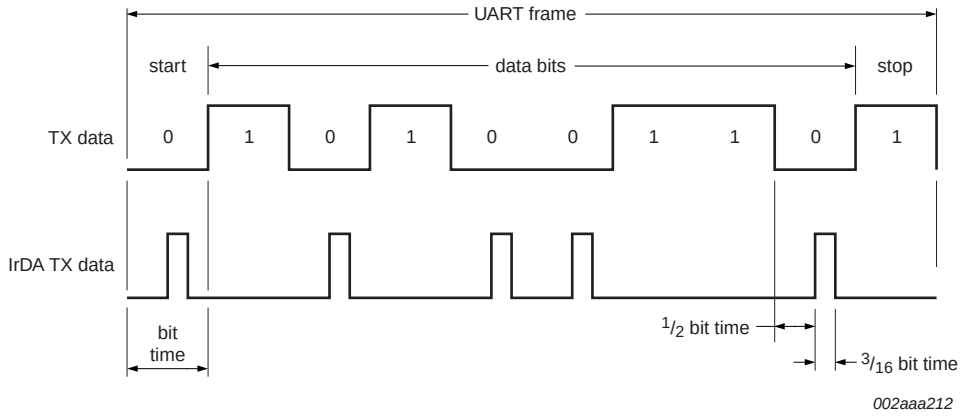

Fig 30. Infrared transmit timing

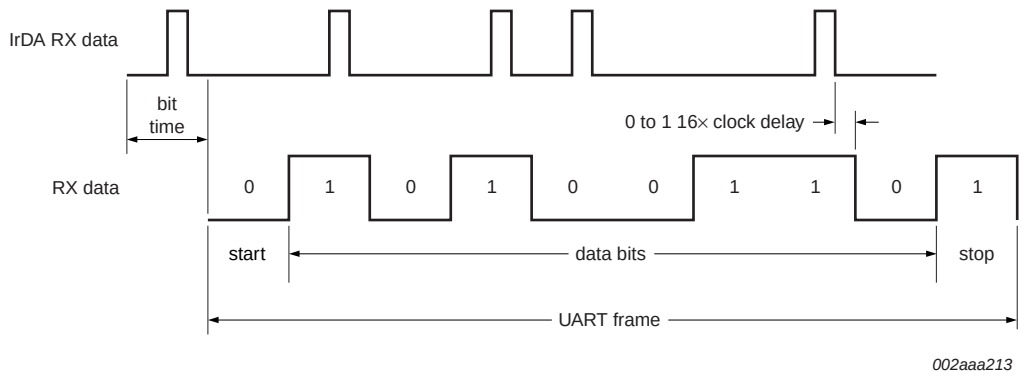

Fig 31. Infrared receive timing

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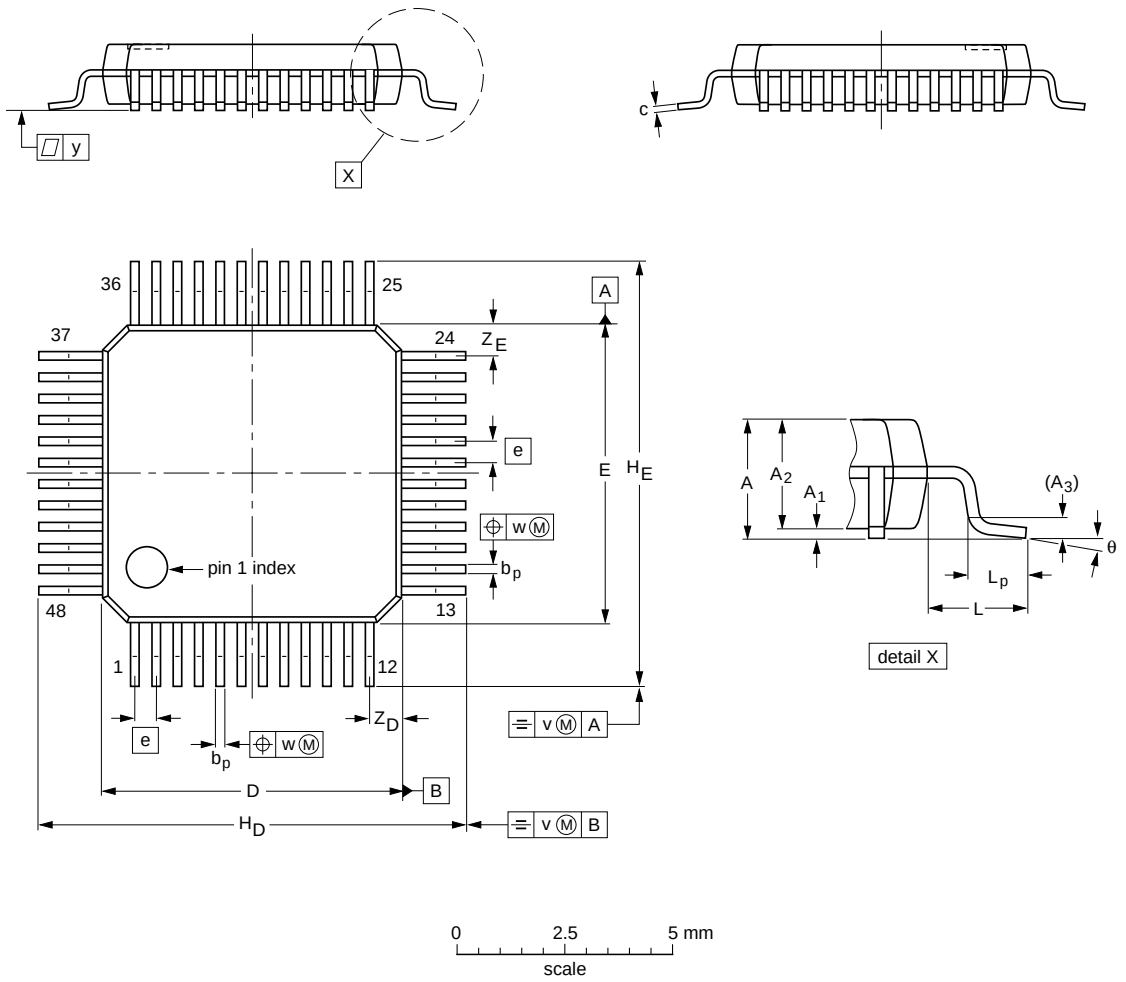
11. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 32. Package outline SOT313-2 (LQFP48)

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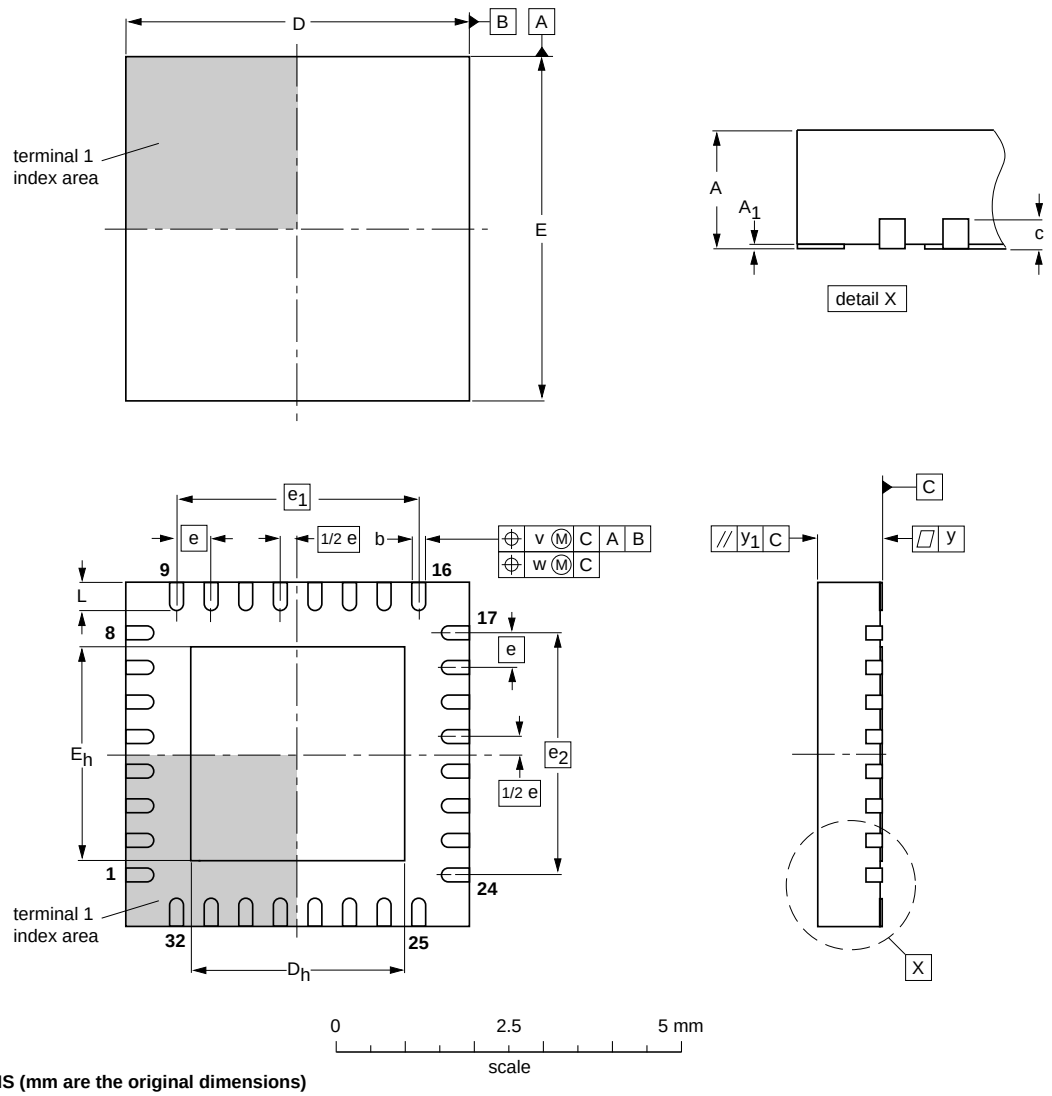
HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 33. Package outline SOT617-1 (HVQFN32)

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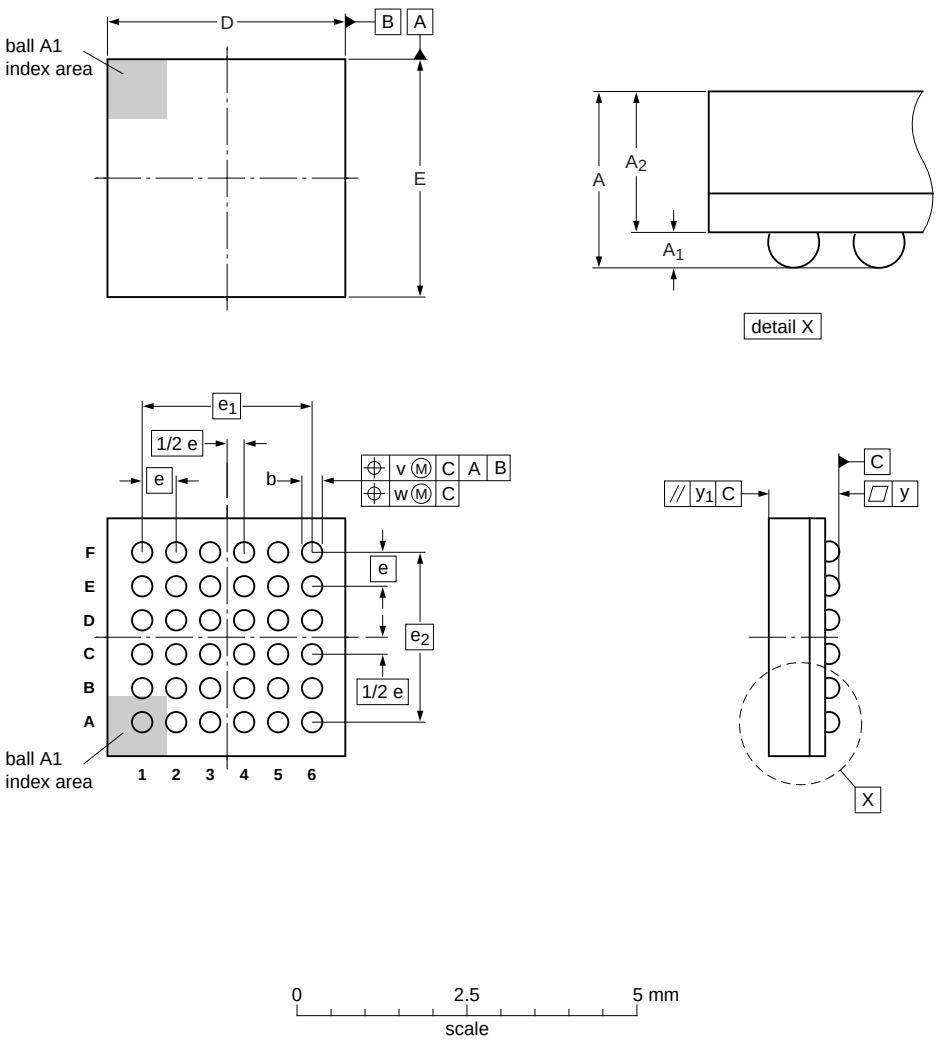
TFBGA36: plastic thin fine-pitch ball grid array package; 36 balls; body 3.5 x 3.5 x 0.8 mm **SOT912-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	3.6 3.4	3.6 3.4	0.5	2.5	2.5	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT912-1	- - -	- - -	- - -			~~05-08-09~~ 05-09-01

Fig 34. Package outline SOT912-1 (TFBGA36)

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12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 35) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 41 and 42

Table 41. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 42. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 35.

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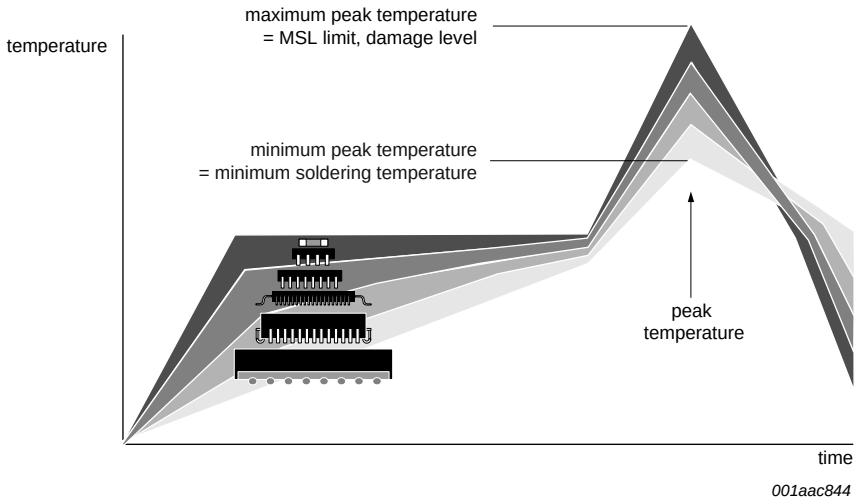

MSL: Moisture Sensitivity Level

Fig 35. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 43. Abbreviations

Acronym	Description
CPU	Central Processing Unit
DLL	Divisor Latch LSB
DLM	Divisor Latch MSB
DMA	Direct Memory Access
FIFO	First In, First Out
IrDA	Infrared Data Association
ISDN	Integrated Service Digital Network
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
RoHS	Restriction of Hazardous Substances directive
UART	Universal Asynchronous Receiver/Transmitter

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14. Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC16C852L v.4	20110201	Product data sheet	-	SC16C852L v.3
Modifications:	• Table 38 “Static characteristics”: – $V_{IL(clk)}$ specification: added condition “XTAL1 pin” – $V_{IH(clk)}$ specification: added condition “XTAL1 pin” – V_{IL} specification split for condition “LOWPWR pin”. – V_{IH} specification split for condition “LOWPWR pin”. – Added (new) Table note [1].			
SC16C852L v.3	20080118	Product data sheet	-	SC16C852L v.2
SC16C852L v.2	20070125	Product data sheet	-	SC16C852L v.1
SC16C852L v.1	20061109	Objective data sheet	-	-

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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