NXP demo board for configurable logic device 74AXP1G57

Demonstrate seven different logic functions

This compact board makes it easy to evaluate all seven functions of the 74AXP1G57

Key features and benefits

- Wide supply voltage range: 0.7 to 2.75 V
- High noise immunity
- Excellent ESD Protection
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption: I_{cc} (max) = 0.6 µA (max)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 2.75 V
- Low noise overshoot and undershoot: <10% of V_{cc}
- I_{OFF} circuitry operates in partial power-down mode
- Multiple package options
- Specified from -40 to +85 °C

The NXP 74AXP1G57 is a low-power, low-voltage device for configurable logic gate functions. The output state is determined by eight patterns of 3-bit input. The device can be configured as a two-input AND, NAND, NOR, XNOR, inverter, or buffer. All inputs can be connected to Vcc or GND. The device ensures a very low static and dynamic power consumption across the entire V_{cc} range from 0.7 to 2.75 V.

The 74AXP1G57 is designed for low-voltage, power-sensitive applications with critical power budget. Inputs can withstand voltages up to 2.75 V, with a supply voltage ranging from 0.7 to 2.75 V. The input pins tolerate over-supply voltages, supporting translation between high- and low-level voltages using AXP logic.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current from going through the device when it is powered down. Schmitt trigger inputs make the circuit tolerant to slower input rise and fall times across the entire V_{cc} range.

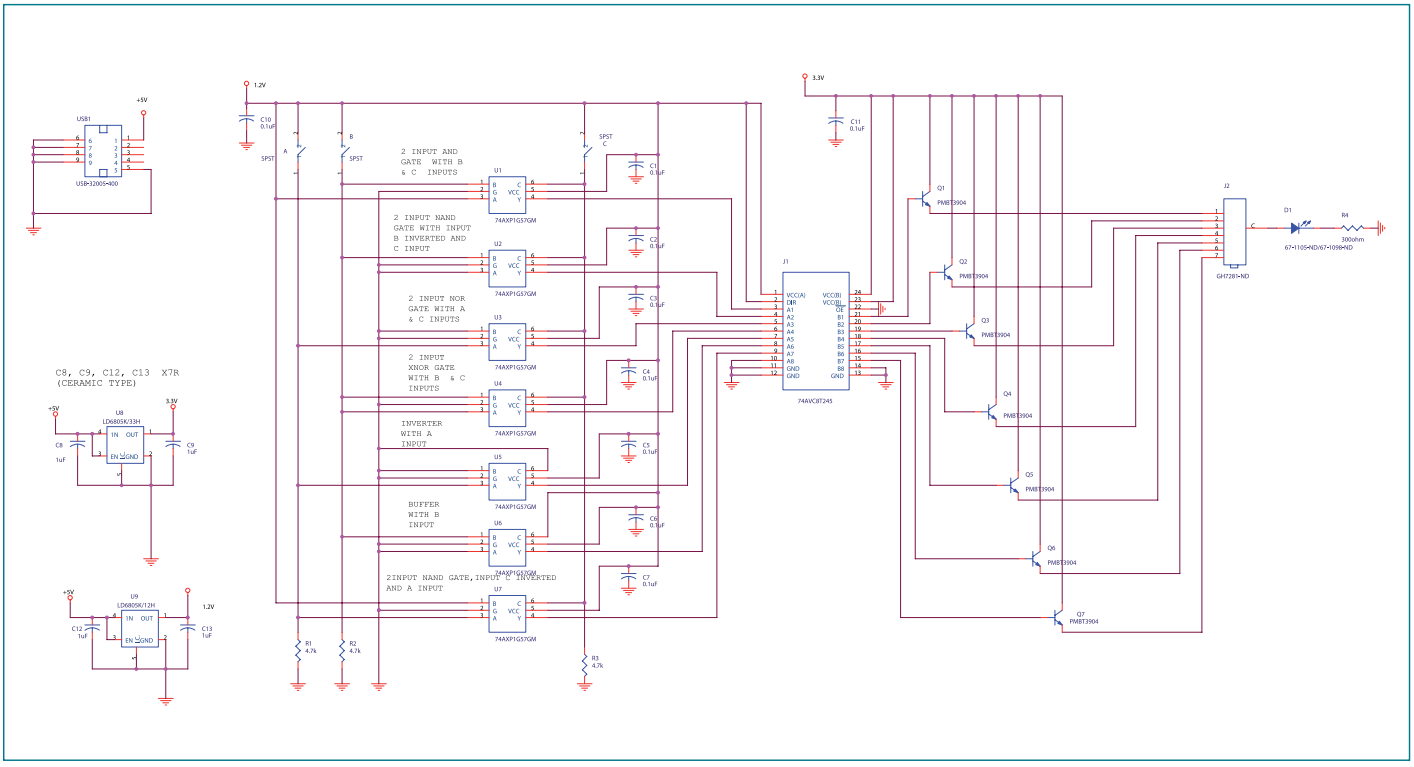
Schematics for the demo board are shown below. Each of the seven AXP1G57 devices is configured for a different logic function. Each 74AXP1G57 has an identical Y output which is connected to NXP's 8-bit level shifter 74AVC8T245 for translation between 1.2 and 3.3 V.
The 3.3 V output of the AVC8T245 is used to drive NXP's seven PMBT3904 devices i.e. NPN BJT transistors which turn on or off a green or red 2.2 V, 20 mA LED.

Three push-button switches are provided to toggle the input pins A, B, and C as marked on the configuration diagrams.

A rotary switch is used to select one of the seven outputs of the AVC8T245 and to drive the on-board LED. The user can select the desired function type on the board and verify it with the corresponding truth table for the function.

A Mini-USB socket is provided to supply power to the AXP1G57 devices via an NXP 1.2 V fixed output regulator LD6805K/12H. The NXP 3.3 V fixed output regulator LD6805K/33H is used to supply power from the USB socket to the on-board NXP NPN drive transistors for LEDs.
Note: The USB data lines are not connected and there is no USB control available for this board.

Circuit schematic of 74AXP1G57 demo board



Other configurable logic devices

NXP offers configurable logic devices for many of the most common logic functions. This table makes it easy to find the device with the right mix of logic functions.

Part	Translator	True Schmitt trigger inputs	AND	AND with two inverted inputs	AND with one inverted input	Buffer	Inverter	MUX	MUX with inverted output	NAND	NAND with two inverted inputs	NAND with one inverted input	NOR	NOR with two inverted inputs	NOR with one inverted input	OR
74AXP1G57		•	•	•		•	•					•	•	•		
74AXP1G58		•			•	•	•			•	•				•	•
74AXP1G97		•	•		•	•	•	•				•			•	•
74AXP1G98		•			•	•	•		•	•		•	•		•	
74AUP1G57		•	•	•		•	•					•	•	•		
74AUP1T57*	•	•	•	•		•	•					•	•	•		
74LVC1G57		•	•	•		•	•					•	•	•		
74AUP1G58		•			•	•	•			•	•				•	•
74AUP1T58*	•	•			•	•	•			•	•				•	•
74LVC1G58		•			•	•	•			•	•				•	•
74AUP1G97		•	•		•	•	•	•				•			•	•
74AUP1T97*	•	•	•		•	•	•	•				•			•	•
74LVC1G97		•	•		•	•	•	•				•			•	•
74AUP1G98		•			•	•	•		•	•		•	•		•	
74AUP1T98*	•	•			•	•	•		•	•		•	•		•	
74LVC1G98		•			•	•	•		•	•		•	•		•	
74LVC1G99		•	•	•	•	•	•	•	•	•	•	•				

Package options for other configurable logic devices

The table below lists the SOT number and the corresponding NXP package suffix for each configurable logic device.

Part	363 GW	457 GV	833 GT	886 GM	891 GF	902 GM	996 GD	1089 GF	1115 GN	1116 GN	1202 GS	1203 GS
74AXP1G57				•					•		•	
74AXP1G58				•					•		•	
74AXP1G97				•					•		•	
74AXP1G98				•					•		•	
74AUP1G57	•			•	•				•		•	
74AUP1T57*	•			•	•				•		•	
74LVC1G57	•	•		•	•				•		•	
74AUP1G58	•			•	•				•		•	
74AUP1T58*	•			•	•				•		•	
74LVC1G58	•	•		•	•				•		•	
74AUP1G97	•			•	•				•		•	
74AUP1T97*	•			•	•				•		•	
74LVC1G97	•	•		•	•				•		•	
74AUP1G98	•			•	•				•		•	
74AUP1T98*	•			•	•				•		•	
74LVC1G98	•	•		•	•				•		•	
74LVC1G99			•			•	•	•		•		•

* 74AUP1GXX functions have lower input switching thresholds than 74AUP1GXX devices. Also, 74AUP1TXX devices can be used in logic-level translation applications with input switching levels that accept 1.8 V low-voltage CMOS signals, while operating from either a single 2.5 or 3.3 V supply voltage.

Operating guide

To operate the demo, connect a standard type A USB-to-Mini-USB cable (not included) between the USB power source (power supply or PC USB socket) and the Mini-USB socket on the demo board.

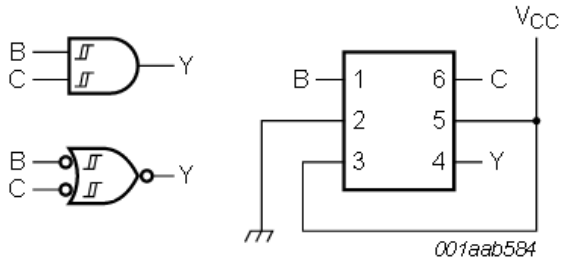
Devices U1 through U6 i.e. 74AXP1g57GM are located on the back side of the board. The NXP LD6805K/33H, LD6805K/12H, AVC8T245PW, and PMBT3904 are also located on the back side of the board. Changing the positions of the rotary switch demonstrates device configuration into a unique function.

U1 operation (1 on rotary-switch output circle)

Device U1 is configured as a two-input AND gate. Switches B and C select input levels for the gate and the signal is transferred to output Y. The LED lights up when the inputs are held at logic 1, with the rotary switch at position 1 and both B and C switches pushed down.

Truth table

A	B	C	Y	D
0	0	0	0	Off
1	0	0	0	Off
1	1	0	0	Off
0	1	0	0	Off
1	0	1	0	Off
1	1	1	1	On
0	1	1	1	On

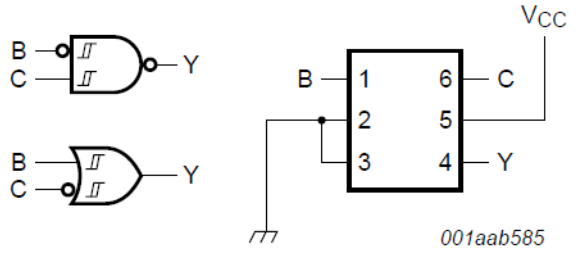


U2 operation (2 on rotary-switch output circle)

Device U2 is configured as a two-input NAND gate with an inverted B input. Toggle switches B and C to demonstrate the function.

Truth table

A	B	C	Y	D
0	0	0	1	On
1	0	0	1	On
1	1	0	1	On
0	1	0	1	On
1	0	1	0	Off
1	1	1	1	On
0	1	1	1	On



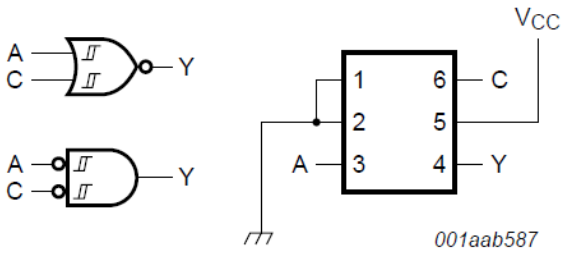
* Note: Since the A input is hard-wired to GND, toggling the A switch does not impact gate function.

U3 operation (3 on rotary-switch output circle)

Device U3 is configured as a two-input NOR gate with A and C inputs. Push the switches A and C to demonstrate the function.

Truth table

A	B	C	Y	D
0	0	0	1	On
1	0	0	0	Off
1	1	0	0	Off
0	1	0	1	On
1	0	1	0	Off
1	1	1	0	Off
0	1	1	0	Off



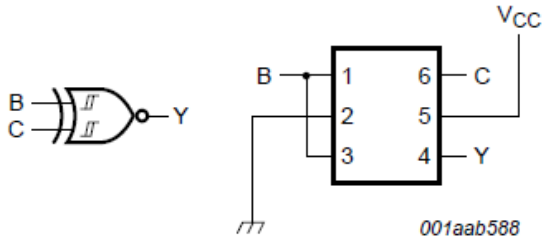
* Note: Since the B input is hard-wired to Vcc, toggling the B switch does not impact gate function.

U4 operation (4 on rotary-switch output circle)

Device U4 is configured as a two-input XNOR gate with B and C inputs. Toggle switches B and C to demonstrate the function. LED D4 stays ON at all times except when either the B or C input is held low.

Truth table

A	B	C	Y	D
0	0	0	1	On
1	0	0	1	On
1	1	0	0	Off
0	1	0	0	Off
1	0	1	0	Off
1	1	1	1	On
0	1	1	1	On



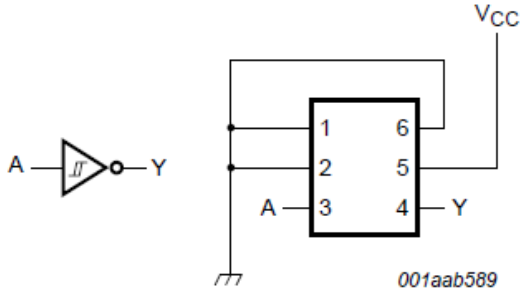
* Note: since the A input is hard-wired to GND, toggling the A switch does not impact gate function.

U5 operation (5 on rotary-switch output circle)

Device U5 is configured as a single inverter. Toggle switch A to demonstrate the function. LED D stays ON as long as the A input is 0.

Truth table

A	B	C	Y	D5
0	0	0	1	On
1	0	0	0	Off
1	1	0	0	Off
0	1	0	1	On
1	0	1	0	Off
1	1	1	0	Off
0	1	1	1	On



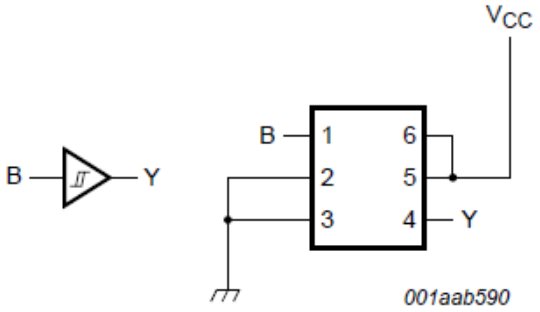
* Note: Since the B and C inputs are hard-wired to GND, toggling the B and C switches does not impact gate function.

U6 operation (6 on rotary-switch output circle)

Device U6 is configured as a single-channel buffer. Toggle switch B to demonstrate the function. LED D stays ON as long as the B input/switch is held high at 1.

Truth table

A	B	C	Y	D
0	0	0	0	Off
1	0	0	0	Off
1	1	0	1	On
0	1	0	1	On
1	0	1	0	Off
1	1	1	1	On
0	1	1	1	On



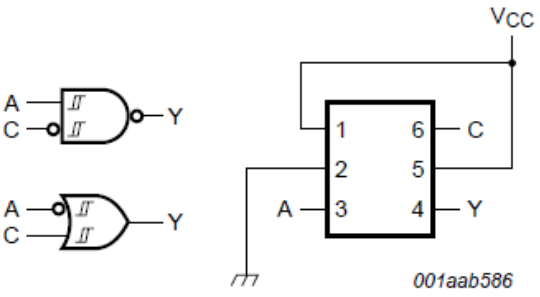
* Note: Since the A input is hard-wired to GND and the C input is hard-wired to Vcc, toggling the A and C switches does not impact buffer function.

U7 operation (7 on rotary-switch output circle)

Device U7 is configured as a two-input NAND gate with inverted C and A inputs. Toggle switches A and C to demonstrate the function. LED D7 stays ON as long as the B input/switch is held high at 1.

Truth table

A	B	C	Y	D
0	0	0	1	On
1	0	0	0	Off
1	1	0	0	Off
0	1	0	1	On
1	0	1	1	On
1	1	1	1	On
0	1	1	1	On



* Note: since the B input is hard-wired to Vcc, toggling the B switch does not impact gate function.

Packages

The 74AXP1G57 is available in the following 6-pin packages: SOT886, SOT1115, SOT1202.

Package suffix	-GM	-GN	-GS
			
Width (mm)	1.45	0.9	1.0
Length (mm)	1.0	1.0	1.0
Height (mm)	0.5	0.35	0.35
Pitch (mm)	0.5	0.35	0.35
SOT	SOT886	SOT1115	SOT1202

Ordering Information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
74AXP1G57GM	-40 to 125 °C	XSON6	Surface-mounted package	RC	Plastic
74AXP1G57GN	-40 to 125 °C	XSON6	Extremely thin small outline package; no leads	RC	Plastic
74AXP1G57GS	-40 to 125 °C	XSON6	Extremely thin small outline package; no leads	RC	Plastic

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