TFA9815

Stereo full-bridge audio amplifier 2 x 17 W

Rev. 01 — 16 December 2008 Preliminary data sheet

1. General description

The TFA9815 is a 2-channel power comparator for high-efficiency class D audio amplifier systems. It contains two full-bridge Bridge-Tied Load (BTL) power stages, drive logic, protection control logic and full differential input comparators. By using this power comparator a compact closed-loop self-oscillating digital audio amplifier system or open-loop system can be built. The continuous output power is 2 ×17 W in a full-bridge BTL application. The TFA9815 does not require a heat sink and operates using an asymmetrical supply voltage.

2. Features

- Stereo full-bridge audio amplifier for class D applications
- No external heat sink required
- Operating voltage range: asymmetrical from 8 V to 20 V
- Thermally protected
- Zero dead-time switching
- Current-limiting (no audible interruptions)

3. Applications

- Self-oscillating or open-loop class D audio amplifier applications
- Flat-panel television sets
- Flat-panel monitors
- Multimedia systems
- Wireless speakers
- High-end CRT television sets

4. Quick reference data

Table 1. Quick reference data

V_P = 12 V; f_{osc} = 550 kHz; T_{amb} = 25 °C; typical application diagram Figure 12, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
V_P	supply voltage	single, asymmetrical supply (V_{DD} - V_{SS})	8	12	20	V
I_P	supply current	Sleep mode	-	110	200	µA

founded by Philips

Table 1. Quick reference data *...continued*

V_P = 12 V; f_{osc} = 550 kHz; T_{amb} = 25 °C; typical application diagram Figure 12, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no snubbers; no filter connected	-	40	50	mA
η_{po}	output power efficiency	output power; 2 × 10 W into 8 Ω	89	91	-	%
$P_{o(RMS)}$	RMS output power	V_P = 15 V; R_L = 8 Ω; THD = 10 %	15	16	-	W
		V_P = 12 V; R_L = 8 Ω; THD = 10 %	9	10	-	W
		V_P = 12 V; R_L = 6 Ω; THD = 10 %	12	13	-	W
		V_P = 12 V; R_L = 4 Ω; THD = 10 %	17	18	-	W

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9815T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

6. Block diagram

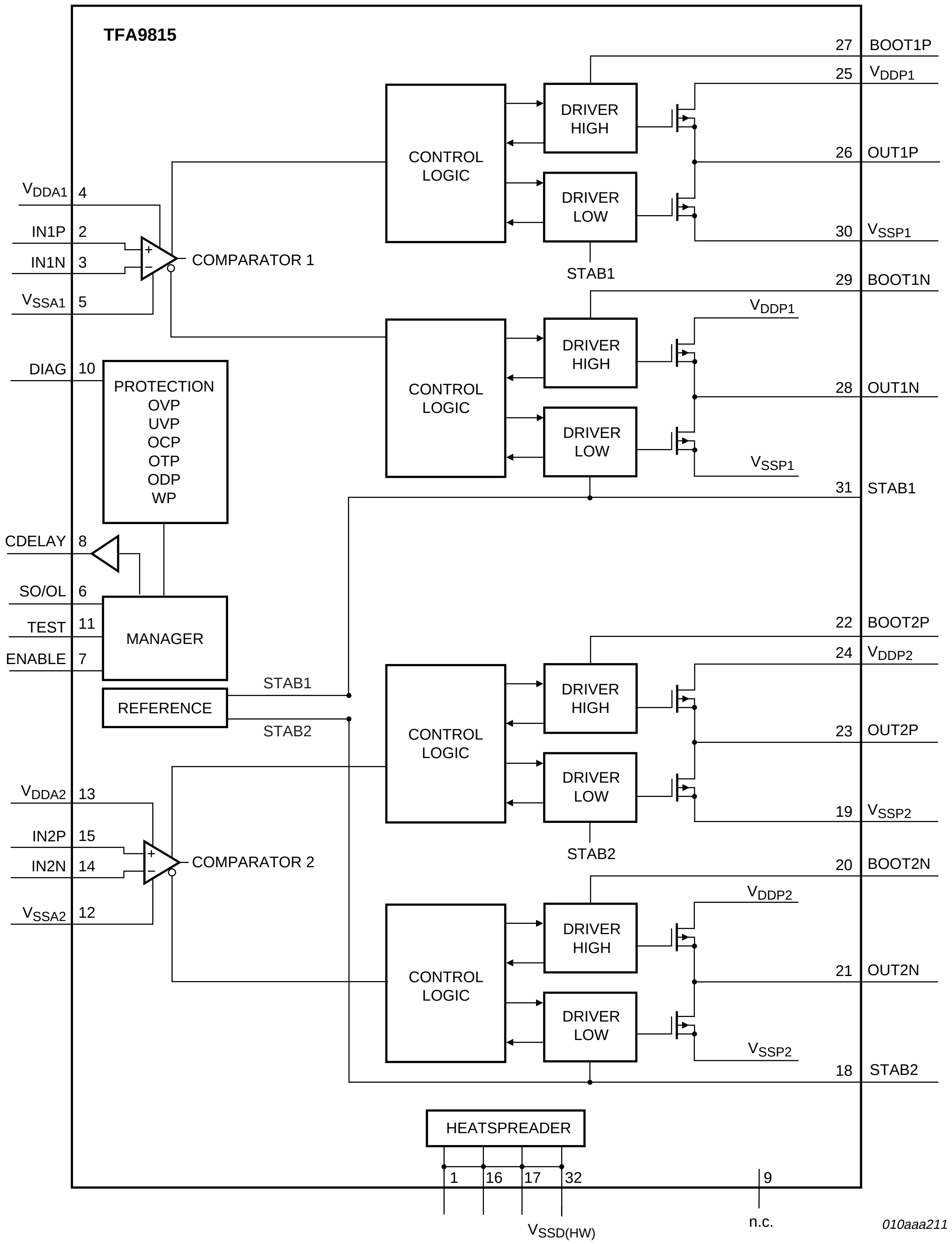


Fig 1. TFA9815 block diagram

7. Pinning information

7.1 Pinning

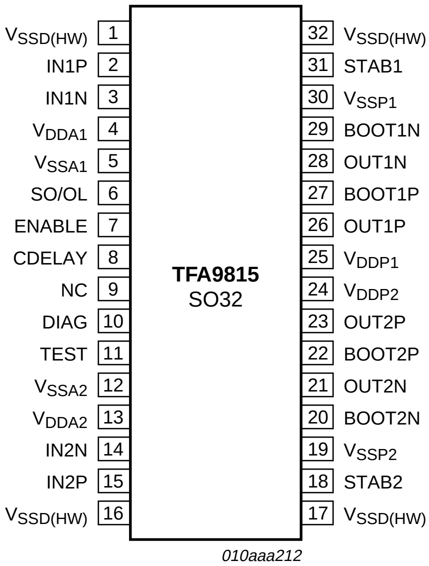


Fig 2. Pin configuration

The SO32 package has four corner leads. These leads (1, 16, 17 and 32) are internally connected to the die pad and must be connected to V_{SSA}. Together with the applied copper area on the PCB these leads determine the ambient temperature, which affects the thermal resistance of the junction.

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{SSD(HW)}$	1	negative digital supply voltage and handle-wafer connection
IN1P	2	positive input comparator channel 1
IN1N	3	negative input comparator channel 1
V_{DDA1}	4	positive analog supply voltage channel 1
V_{SSA1}	5	negative analog supply voltage channel 1
SO/OL	6	self-oscillating / open-loop configuration enable
ENABLE	7	enable input to switch between Sleep and Operating mode
CDELAY	8	switch on/off timing control
n.c.	9	not connected
DIAG	10	diagnostic output; open-drain
TEST	11	test signal input; for testing purposes only
V_{SSA2}	12	negative analog supply voltage channel 2
V_{DDA2}	13	positive analog supply voltage channel 2
IN2N	14	negative input comparator channel 2

Table 3. Pin description *...continued*

Symbol	Pin	Description
IN2P	15	positive input comparator channel 2
$V_{SSD(HW)}$	16	negative digital supply voltage and handle-wafer connection
$V_{SSD(HW)}$	17	negative digital supply voltage and handle-wafer connection
STAB2	18	decoupling of internal 11 V regulator for channel 2 drivers
V_{SSP2}	19	negative power supply voltage channel 2
BOOT2N	20	bootstrap high-side driver negative output channel 2
OUT2N	21	negative output channel 2
BOOT2P	22	bootstrap high-side driver positive output channel 2
OUT2P	23	positive output channel 2
V_{DDP2}	24	positive power supply voltage channel 2
V_{DDP1}	25	positive power supply voltage channel 1
OUT1P	26	positive output channel 1
BOOT1P	27	bootstrap high-side driver positive output channel 1
OUT1N	28	negative output channel 1
BOOT1N	29	bootstrap high-side driver negative output channel 1
V_{SSP1}	30	negative power supply voltage channel 1
STAB1	31	decoupling of internal 11 V regulator for channel 1 drivers
$V_{SSD(HW)}$	32	negative digital supply voltage and handle-wafer connection

8. Functional description

8.1 General

The TFA9815 is a dual-switching power comparator. It is the main building block for a stereo high-efficiency Class D audio power amplifier system. It contains two full-bridge BTL power stages, drive logic, protection control logic and full differential input comparators and references (see Figure 1). By using this power comparator a compact closed-loop self-oscillating digital amplifier system or open-loop system can be built. A second-order low-pass filter converts the PWM output signal into an analog audio signal across the speaker.

8.2 Interfacing

The pins ENABLE and SO/OL control the Operating mode of the TFA9815. Both the ENABLE and the SO/OL pins are referenced to $V_{SSD(HW)}$.

When the SO/OL pin is connected to $V_{SSD(HW)}$ the TFA9815 is in self-oscillating configuration: when the SO/OL pin is floating the TFA9815 is in open-loop configuration. Under this latter condition the open-pin voltage is typically 4 V applied internally. The TEST pin needs to be connected to ground in both situations.

Table 4. SO/OL connections

Interfacing	
SO/OL connected to:	Configuration
$V_{SSD(HW)}$	Self-oscillating
Open	Open-loop

The device has two modes: Sleep and Operating.

In Sleep mode the TFA9815 is not biased and has a very low supply current. Sleep mode can also be used to quickly mute the device.

When the TFA9815 is set into Operating mode the device is started via the start-up sequence, which provides a pop-free start-up behavior. After start-up the STABn reference voltages are present and the outputs start switching.

Table 5. Start-up

Interfacing	
ENABLE (V)	Mode
ENABLE < 0.8 V	Sleep mode
ENABLE > 3 V	Operating mode

8.3 Input comparators

The input stages have a differential input and are optimized for low noise and offset. This results in maximum flexibility in the application.

Operating in self-oscillating configuration the inputs (IN1P, IN1N, IN2P, IN2N) of the comparators are internally set to a voltage level of $\frac{1}{2}V_P$, but only during the start-up sequence. In Operating mode the inputs are high-ohmic.

Operating in open-loop configuration, no internal voltages are applied to the inputs. The input pins (IN1P, IN1N, IN2P, IN2N) are pulled down to V_{SSA1} and V_{SSA2} level by internal resistors.

8.4 Diagnostic

The DIAG output is an open-drain output. The maximum current is 2 mA. When one of the protections is activated the DIAG output is set LOW. The DIAG output refers to V_{SSD}.

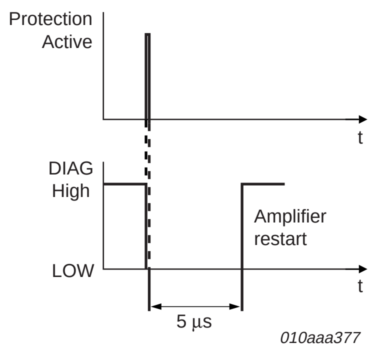


Fig 3. Timing diagram

8.5 Protections

The TFA9815 has the following protections:

- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- OverVoltage Protection (OVP)
- UnderVoltage Protection (UVP)
- OverDissipation Protection (ODP)
- Window Protection (WP)

When either the OTP or the OCP are activated the output power stage is switched off and all the outputs (OUT1N, OUT1P, OUT2N and OUT2P) become floating. The power stage will switch back on after 5 µs or as soon as the fault condition is removed.

When any other protection is activated (OVP, UVP, ODP, or WP) all the outputs become floating and the device shuts down. The TFA9815 will resume operating after the fault condition has been removed, going through the restart sequence shown in Figure 3. Restarting will typically take 500 ms, depending on the power-supply voltage level.

- **Overtemperature protection**

  If the junction temperature (T_j) exceeds a threshold level of about 150 °C the outputs become floating. The device will start switching again after 5 ms and when the temperature is below 150 °C. This thermal limitation is without audible interruptions.

- **Overcurrent protection**

  If the output current exceeds the maximum output-current threshold level the outputs become floating. The device will start switching again after 5 µs. This current limitation is without audible interruptions.

- **Overvoltage protection**

  If the supply voltage applied to the TFA9815 exceeds the maximum supply-voltage threshold level the device shuts down. The device will resume operating when the supply is within the operating range, going through the restart sequence.

- **Undervoltage protection**

  If the supply voltage applied to the TFA9815 falls below the minimum supply-voltage threshold level the device shuts down. The device will resume operating when the supply is within the operating range, going through the restart sequence.

- **Overdissipation protection**

  If the junction temperature (T_j) exceeds 135 °C an internal OverTemperature Warning (OTW) signal is generated. If the overcurrent protection is generated while the OTW is active the device will shut down and resume operating automatically, going through the restart sequence.

- **Window protection**

  During start-up, if one of the outputs is shorted to V_{SS} or V_{DD} the device will interrupt the start-up sequence and wait until the short is removed. This is an effective measure to protect the device against shorts between the outputs (before the filter) and the ground or supply lines. The WP protects the device against errors made during board assembly.

Table 6. Overview protections

Protections				
Symbol	**Condition**	**Diag.**	**Outputs**	**Recovering**
OTP	$T_j > 150$ °C	LOW	Floating	Automatic, after 5 µs and $T_j < 150$ °C
OCP	$I_O > I_{ORM}$	LOW	Floating	Automatic, after 5 µs
OVP	$V_P > 20$ V	LOW	Floating	Switch-off to restart when $V_P < 20$ V
UVP	$V_P < 8$ V	LOW	Floating	Switch-off to restart when $V_P > 8$ V
ODP	$T_j > 135$ °C and $I_O > I_{ORM}$	LOW	Floating	Switch-off to restart
WP	OUTX > V_{DDA} – 1 V or OUTX < V_{SSA} + 1 V	LOW		Start-up after removing fault condition

8.6 Timing diagram

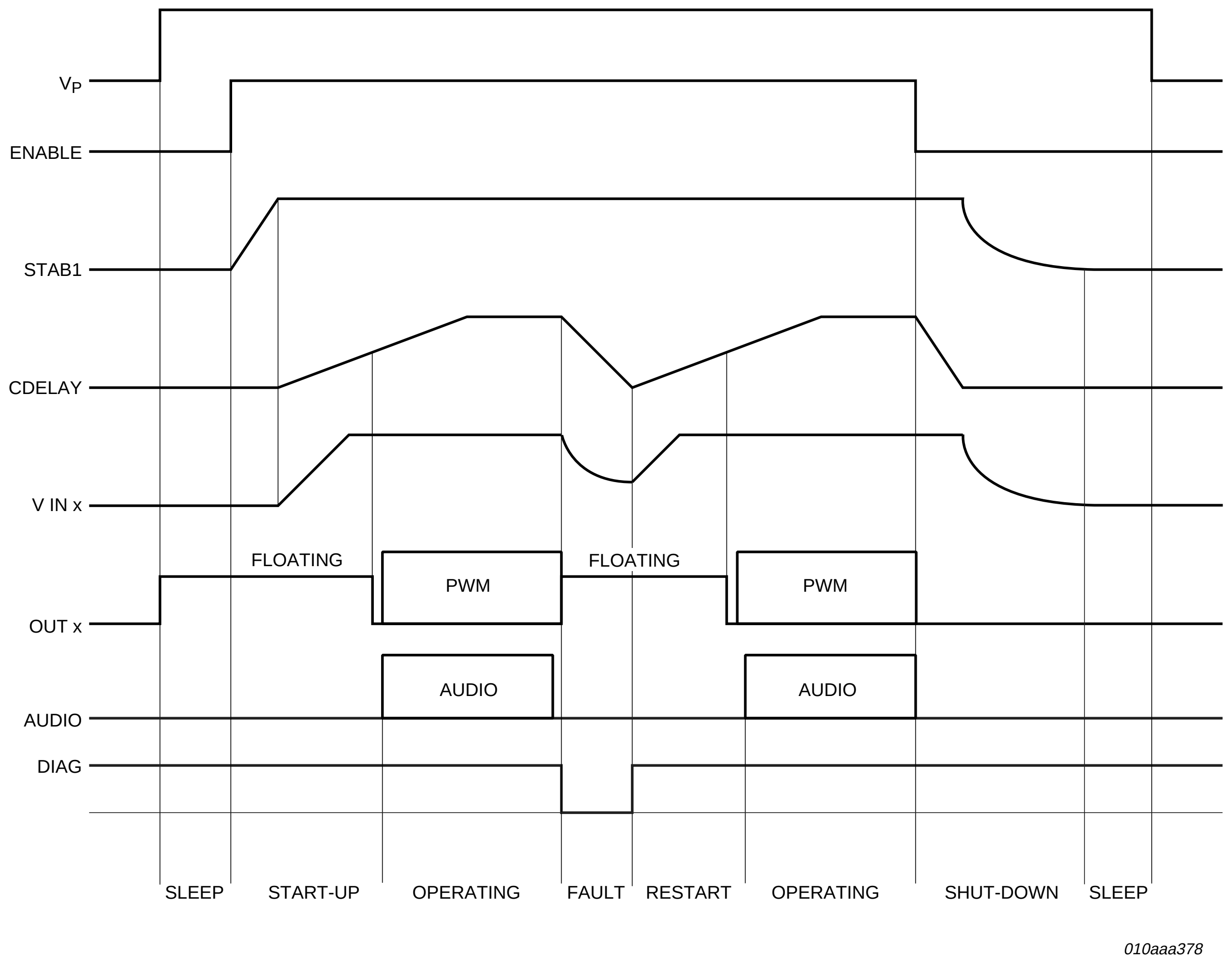


Fig 4. Start-up sequence

9. Internal circuitry

Table 7. Internal circuitry

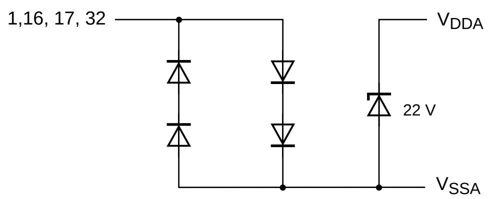
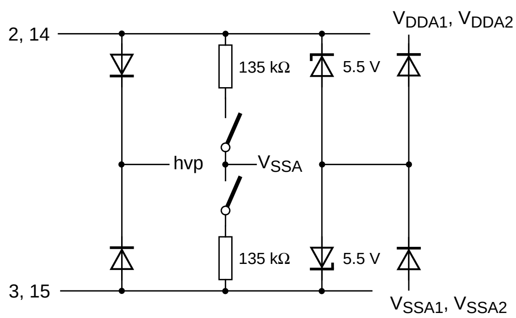
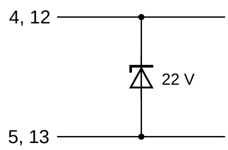
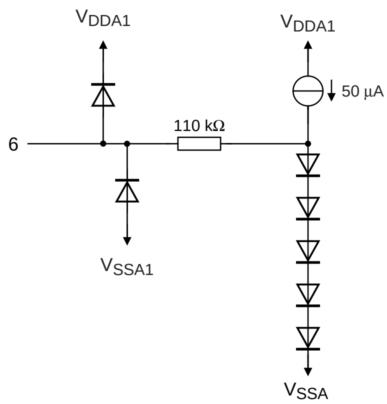
Pin	Symbol	Equivalent circuit
1	$V_{SSD(HW)}$	 *010aaa384*
16	$V_{SSD(HW)}$	
17	$V_{SSD(HW)}$	
32	$V_{SSD(HW)}$	
2	IN1P	 *010aaa385*
3	IN1N	
14	IN2N	
15	IN2P	
4	V_{DDA1}	 *010aaa386*
5	V_{SSA1}	
12	V_{SSA2}	
13	V_{DDA2}	
6	SO/OL	 *010aaa381*

Table 7. Internal circuitry *…continued*

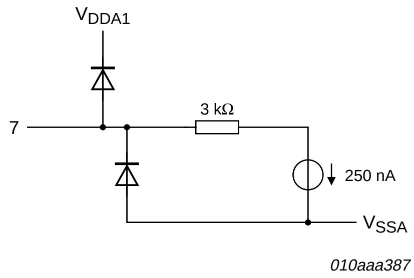
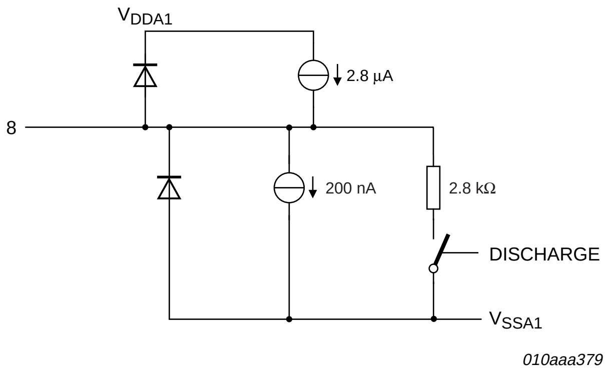
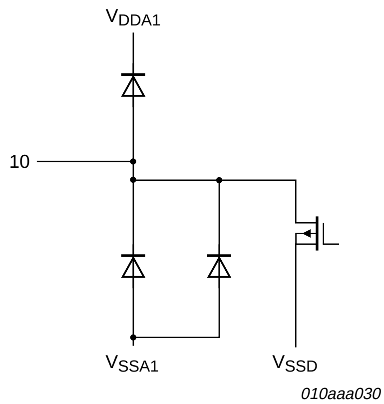
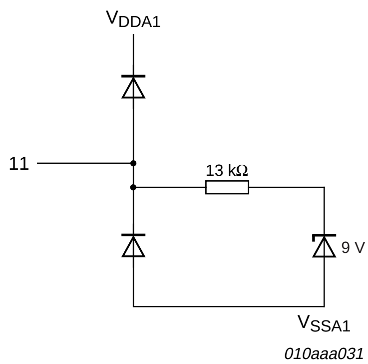
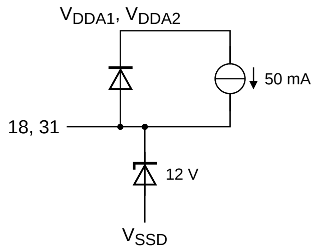
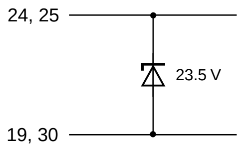
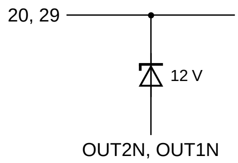
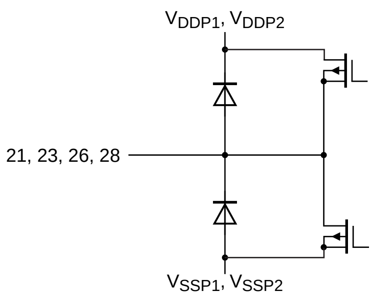
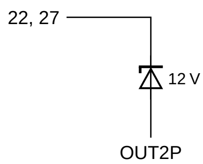
Pin	Symbol	Equivalent circuit
7	ENABLE	
8	CDELAY	
10	DIAG	
11	TEST	

Table 7. Internal circuitry *...continued*

Pin	Symbol	Equivalent circuit
18	STAB2	 010aaa445
31	STAB1	
19	V_{SSP2}	 010aaa446
24	V_{DDP2}	
25	V_{DDP1}	
30	V_{SSP1}	
20	BOOT2N	 010aaa447
29	BOOT1N	
21	OUT2N	 010aaa380
23	OUT2P	
26	OUT1P	
28	OUT1N	
22	BOOT2P	 010aaa448
27	BOOT1P	

10. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	Asymmetrical		–0.3	+23.1	V
I_{ORM}	repetitive peak output current	-		3	-	A
T_j	junction temperature	-		-	180	°C
T_{stg}	storage temperature	-		–55	+150	°C
T_{amb}	ambient temperature	-		–40	+85	°C
P_{max}	maximum power dissipation	-		-	5	W
V_x	voltage on pin x	DIAG		V_{SS} – 0.3	12	V
		IN1P - IN1N		–6	+6	V
		IN2P - IN2N		–6	+6	V
		all other pins		V_{SS} – 0.3	V_{DD} + 0.3	V
V_{esd}	electrostatic discharge voltage	HBM	[1]	–2000	+2000	V
		MM	[2]	–200	+200	V

[1] Human-body model (HBM): R_S = 1500 Ω; C = 100 pF; for pins 2, 3, 14, and 15: V_{esd} = ±1500 V.

[2] Machine model (MM): R_S = 0 Ω; C = 200 pF; L = 0.75 µH.

11. Thermal characteristics

Table 9. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	[1]	-	39	42	K/W
		Two-layer application board	[2]	-	42	-	K/W
Ψ_{j-lead}	thermal characterization parameter from junction to lead	-		-	-	30	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	-	[3]	-	-	8	K/W

[1] Measured in a JEDEC high K-factor test board (standard EIA/JESD 51-7) in free air with natural convection.

[2] Two-layer application board (70 mm x 57 mm), 35 µm copper, FR4 base material in free air with natural convection.

[3] Strongly depends on where the measurement is taken on the package.

12. Characteristics

12.1 Static characteristics

Table 10. Characteristics

V_P= 12 V;T_{amb} = 25 ˚C; f_{osc} = 550 kHz; typical application diagram Figure 12, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_P	supply voltage	single asymmetrical supply ($V_{DD} - V_{SS}$)	8	12	20	V
I_P	supply current	Sleep mode	-	110	200	µA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, no snubbers and no filter connected	-	40	50	mA
Series resistance output power switches						
R_{DSon}	drain-source on-state resistance	T_j = 25 °C	-	150	220	mΩ
Enable input: pin ENABLE[1]						
V_{IL}	LOW-level input voltage	Sleep mode	-	-	0.8	V
V_{IH}	HIGH-level input voltage	Operating mode	3	-	V_P	V
I_I	input current	V_I = 5 V	-	1	20	µA
SO/OL input: pin SO/OL[1]						
V_{IL}	LOW-level input voltage	self-oscillating configuration	0	-	0.4	V
V_{IH}	HIGH-level input voltage	open-loop configuration	3	4	5	V
Stabilizer output pins STAB1 and STAB2						
V_O	output voltage	Operating mode [1]	10.2	11	11.7	V
Comparator full-differential input stage						
$V_{offset(i)(eq)}$	equivalent input offset voltage	-	-	-	1	mV
$V_{n(i)(eq)}$	equivalent input noise voltage	20 Hz < f < 20 kHz	-	-	15	µV
$V_{i(cm)}$	common-mode input voltage	-	V_{SSA} + 3	-	V_{DDA} − 1	V
I_{IB}	input bias current	-	-	-	1	µA
Overtemperature protection						
$T_{act(th\_prot)}$	thermal protection activation temperature	-	150	-	180	°C
Overvoltage protection						
$V_{th(ovp)}$	overvoltage protection threshold voltage	level internal fixed	20.1	21.5	23	V
Undervoltage protection						
$V_{P(uvp)}$	undervoltage protection supply voltage	level internal fixed	7	7.5	7.9	V
Overcurrent protection						
$I_{O(ocp)}$	overcurrent protection output current	- [2]	3	3.5	-	A

Table 10. Characteristics *...continued*

V_P= 12 V;T_{amb} = 25 °C; f_{osc} = 550 kHz; typical application diagram Figure 12, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Window Protection (WP)						
V_O	output voltage	HIGH-level	-	$V_{DDA} - 1$	-	V
		LOW-level	-	$V_{SSA} + 1$	-	V

[1] Measured with respect to V_{SSD}.

[2] Current limiting concept: in overcurrent condition no interruption of the audio signal in case of impedance drop.

12.2 Dynamic characteristics

Table 11. Switching characteristics

V_P= 12 V;T_{amb} = 25 °C; f_{osc} = 550 kHz unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing PWM output: pins OUT1 and OUT2						
t_r	rise time	I_O = 0 A	-	10	-	ns
t_f	fall time	I_O = 0 A	-	10	-	ns
$t_{w(min)}$	minimum pulse width	I_O = 0 A	-	60	-	ns

12.3 AC characteristics measured in typical application

Table 12. AC characteristics measured in typical application

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(RMS)}$	RMS output power	V_P = 15 V; R_L = 8 Ω; THD = 10 %		15	16	-	W
		V_P = 12 V; R_L = 8 Ω; THD = 10 %		9	10	-	W
		V_P = 12 V; R_L = 6 Ω; THD = 10 %		12	13	-	W
		V_P = 12 V; R_L = 4 Ω; THD = 10 %		17	18	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 1 W; f_i = 1 kHz	[1]	-	0.05	0.1	%
η_{po}	output power efficiency	$P_o = 2 \times 10$ W at 8 Ω		89	91	-	%
		$P_o = 2 \times 18$ W at 4 Ω		88	90	-	%
$G_{v(cl)}$	closed-loop voltage gain	V_i = 100 mV (RMS); f_i = 1 kHz		18.6	19.3	21	dB
$V_{n(o)}$	output noise voltage	inputs shorted; AES17 brick-wall		-	150	-	μV
S/N	signal-to-noise ratio	V_o = 10 V (RMS); $G_{v(cl)}$ = 20 dB		94	96	-	dB
SVRR	supply voltage ripple rejection	Operating mode; f_i = 1 kHz	[2]	34	45	-	dB
α_{cs}	channel separation	P_o = 1 W; f_i = 1 kHz		55	70	-	dB

[1] THD+N is measured in a bandwidth of 20 Hz to 20 kHz, AES17, brick-wall.

[2] Minimum value determined by R5, R10, R17, R22 equalling +1 % and R7, R14, R18, R20 equalling –1 %.

13. Application information

13.1 Output power estimation

For BTL configuration the output power can be estimated using Equation 1:

$$P_{o1\%} = \frac{\left[\left[\frac{R_L}{R_L + 2 \times (R_{DSon} + R_S)}\right] \times V_P\right]^2}{2 \times R_L} \qquad (1)$$

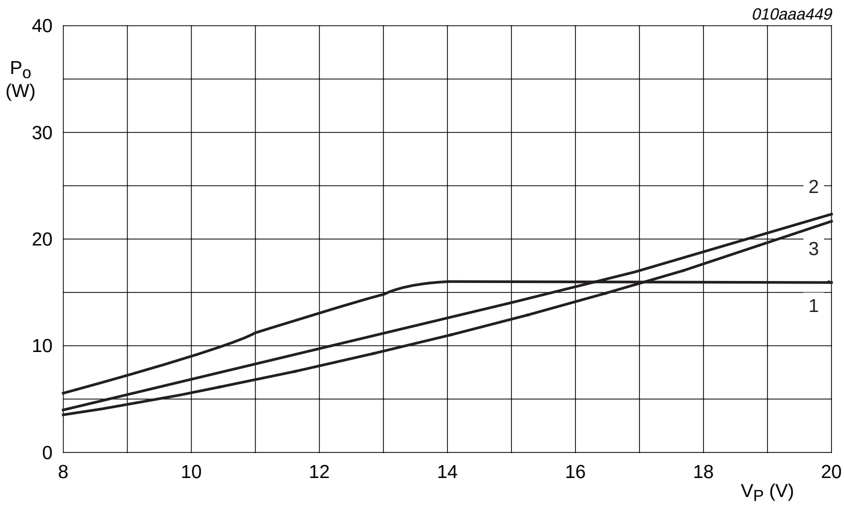
Where,

- V_P = supply voltage [V]
- R_L = load impedance [Ω]
- R_{DSon} = on resistance power switch [Ω]
- R_S = series resistance output inductor [Ω]

The output power at 10% THD can be estimated by using Equation 2

$$P_{o10\%} = 1.25 \times P_{o0.5\%} \qquad (2)$$

Figure 5 and Figure 6 below show the estimated output power at THD = 0.5 % and THD = 10 % as a function of the BLT supply voltage for different load impedances.



THD+N = 0.5 %

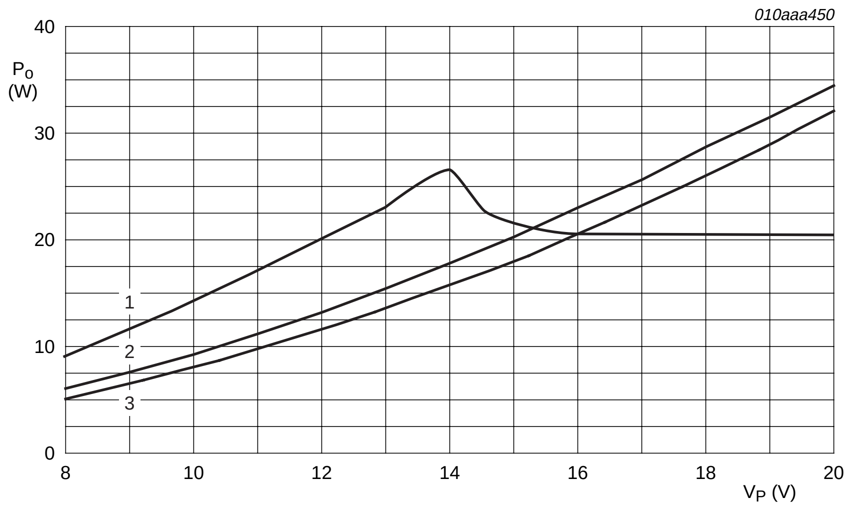
f = 1 kHz

(1) 4 Ω

(2) 6 Ω

(3) 8 Ω

Fig 5. BTL output power as function of supply voltage: THD = 1 %



THD+N = 10 %

f = 1 kHz

(1) R_L = 4 Ω

(2) R_L = 6 Ω

(3) R_L = 8 Ω

Fig 6. BTL output power as function of supply voltage: THD = 10 %

13.2 Output current limiting

The maximum peak output current is limited by the level of the overcurrent protection threshold. During normal operation the output current should not exceed this threshold level of 3 A otherwise the OCP will be triggered and the device will stop switching for 5 µs. The peak output current in BTL can be estimated using the following equation:

$$I_O max \le \frac{V_P}{R_L + 2 \times (R_{DSon} + R_S)} \le 3A$$

Where:

- V_P = supply voltage [V]
- R_L = load impedance [Ω]
- R_{DSon} = on resistance power switch [Ω]
- R_S = series resistance output inductor [Ω]

13.3 Speaker configuration and impedance

For a flat-frequency response (second-order Butterworth filter) it is necessary to change the low-pass filter components LLC and CLC according to the speaker configuration and impedance. Table 13 shows the practical required values:

Table 13. Filter component values

Configuration	Impedance (Ω)	LLC (μH)	CLC (nF)
BTL	4	10	1500
	6	15	1000
	8	22	680

13.4 Differential input

For a high common-mode rejection ratio and a maximum of flexibility in the application, the audio inputs of the application are fully differential.

The input configuration for a differential-input application is illustrated in Figure 7.

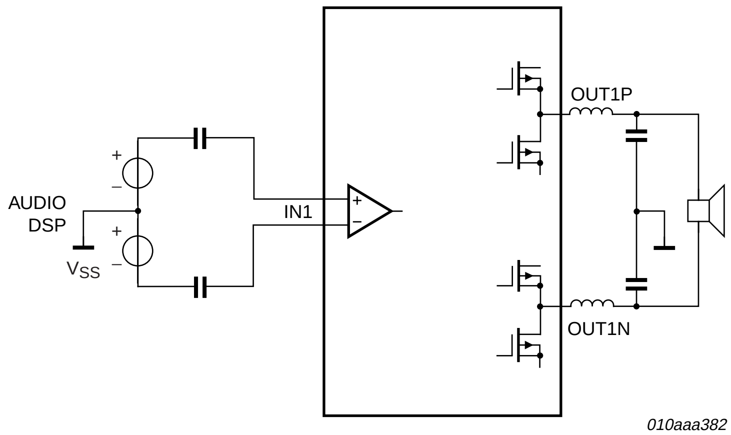


Fig 7. Input configuration for a differential input

13.5 Single-ended input

When using an audio source with a single-ended ‘out’, it is important to connect the IN1N from the application board to the V_{SS} of the audio source (e.g. Audio Digital Signal Processing (Audio DSP)).

The input configuration for a single-ended ‘in’ application is illustrated in Figure 8.

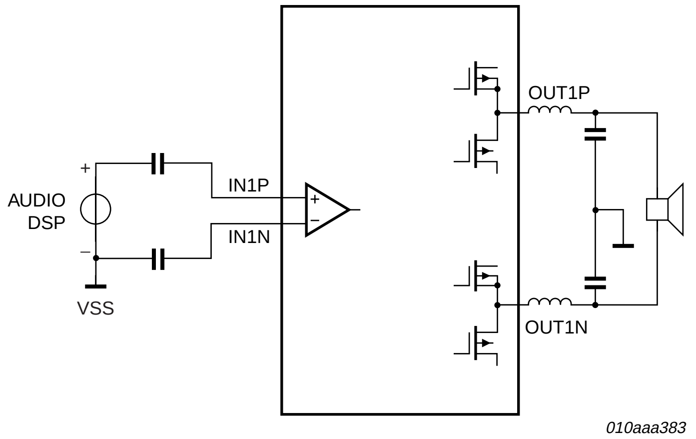
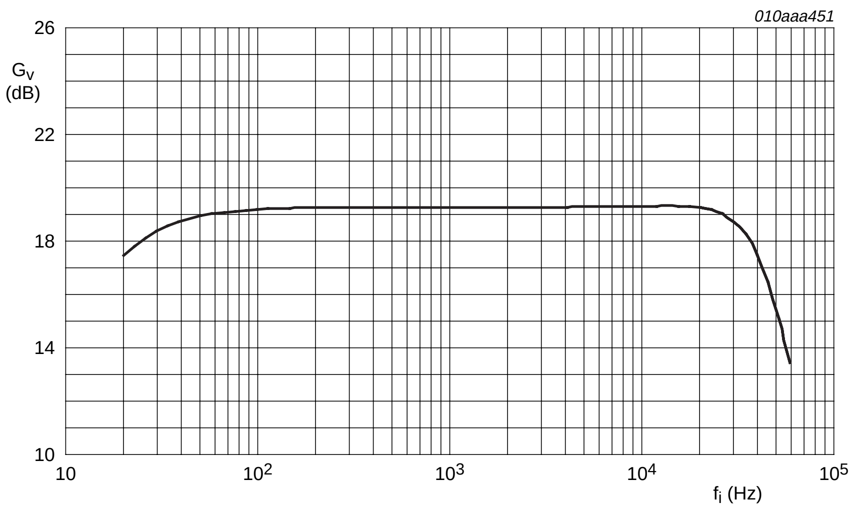


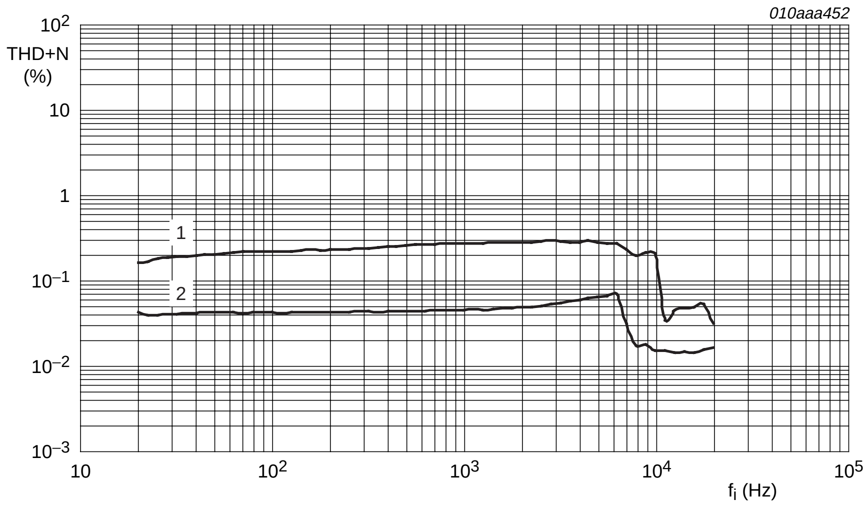
Fig 8. Input configuration for a single-ended input

13.6 Curves measured in a typical application



V_P = 12 V; R_L = 4 Ω; V_I = 300 mV (RMS)

Fig 9. Gain as a function of frequency

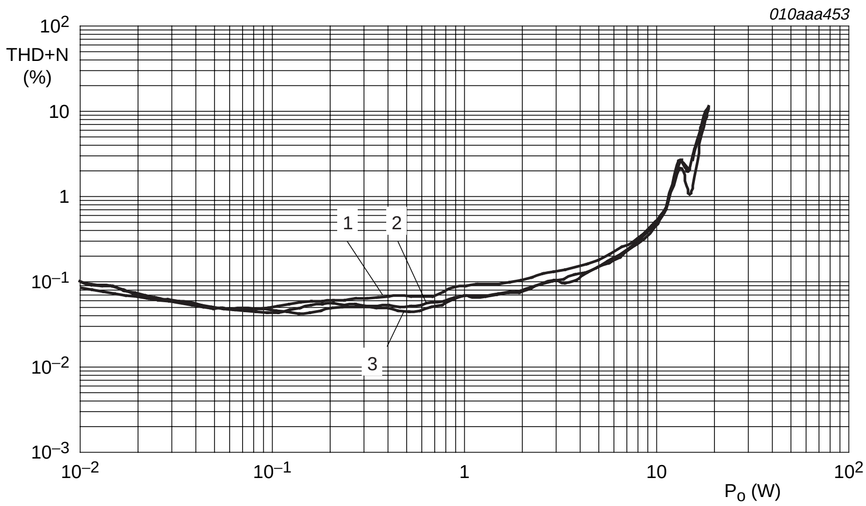


V_P = 12 V; R_L = 4 Ω

(1) P_o = 1 W

(2) P_o = 10 W

Fig 10. Total harmonic distortion + noise as a function of frequency



V_P = 12 V; R_L = 4 Ω; f = 1 kHz

(1) 6 kHz

(2) 1 kHz

(3) 100 Hz

Fig 11. Total harmonic distortion as a function of output power

13.7 Typical application diagram TFA9815

A typical application diagram with the TFA9815 supplied from an asymmetrical supply is shown in Figure 12.

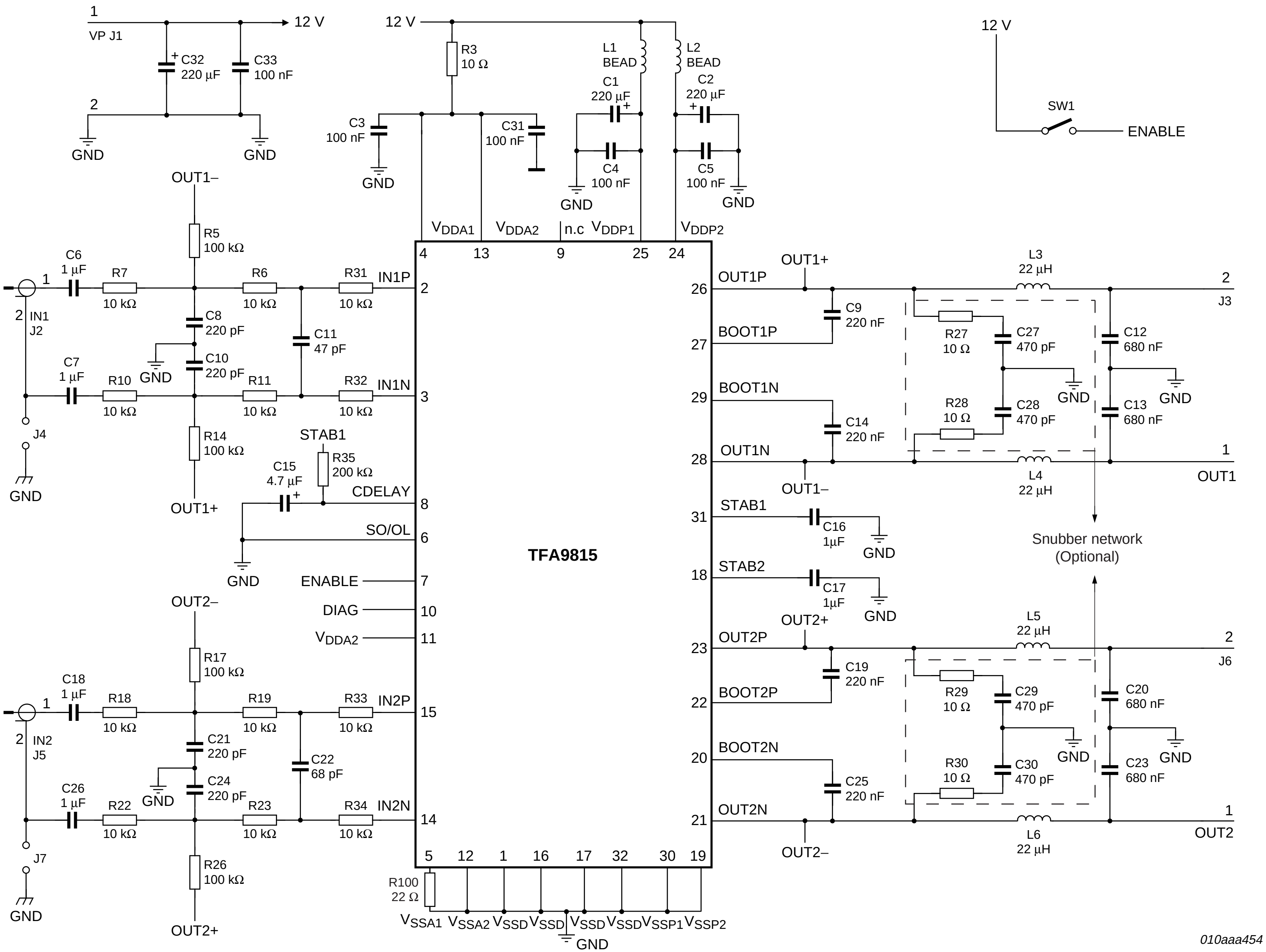


Fig 12. Typical application diagram TFA9815

13.8 Typical application: bill of materials

Table 14. Typical application: bill of materials

Item	Quantity	Reference	Part	Footprint
1	2	C1, C2.	220 mF/35 V	CE09-02R
2	5	C3, C4, C5, C31, C33.	100 nF/50 V	SMD 0805 X7R
3	2	C16, C17.	1 mF/50 V	SMD 1206 X7R
4	4	C6, C7, C18, C26	1 mF/25 V	MKT
5	4	C8, C10, C21, C24.	220 pF/25 V	SMD 0402 NP0
6	4	C9, C14, C19, C25.	220 nF/25 V	SMD 0805 X7R
7	1	C11	47 pF/25 V	SMD 0402 NP0
8	4	C12, C13, C20, C23.	680 nF/25 V	MKT
9	1	C22.	68 pF/25 V	SMD 0402 NP0
10	3	J1, J3, J6.	CON2	2 pins terminal
11	2	J2, J5.	CINCH	CINCH
12	2	J4, J7	Jumper	Closed on demo board only
13	2	L1, L2	BEAD	SMD 1206 Würth Elektronik DC < 0.5 Ω 10 MHz > 80 Ω
14	1	R35	200 kΩ / 0.1 W / 5 %	SMD 0603
15	1	C15	4.7 μF / 16 V	
16	4	L3, L4, L5, L6.	22 μH	8RDY TOKO A7040HN-220M, 11RHBP TOKO A7503CY-220M or Sagami 7311NA-220M
17	5	R3	10 / 0.25 W / 5 %	SMD 1206
18	4	R5, R14, R17, R26.	100 kΩ / 0.1 W / 1 % for 20 dB 200 k / 0.1 W / 1 % for 26 dB	SMD 0603
19	12	R6, R7, R10, R11, R18, R19, R22, R23, R31, R32, R33, R34.	10 kΩ / 0.1 W / 1 %	SMD 0603
20	1	R100	22 Ω / 5 % / 0.1 W	SMD 0603
21	1	SW1	SC 1X1	Secme 090320901
22	1	U1	TFA9815T	SOT287-1 (SO32) NXP Semiconductors

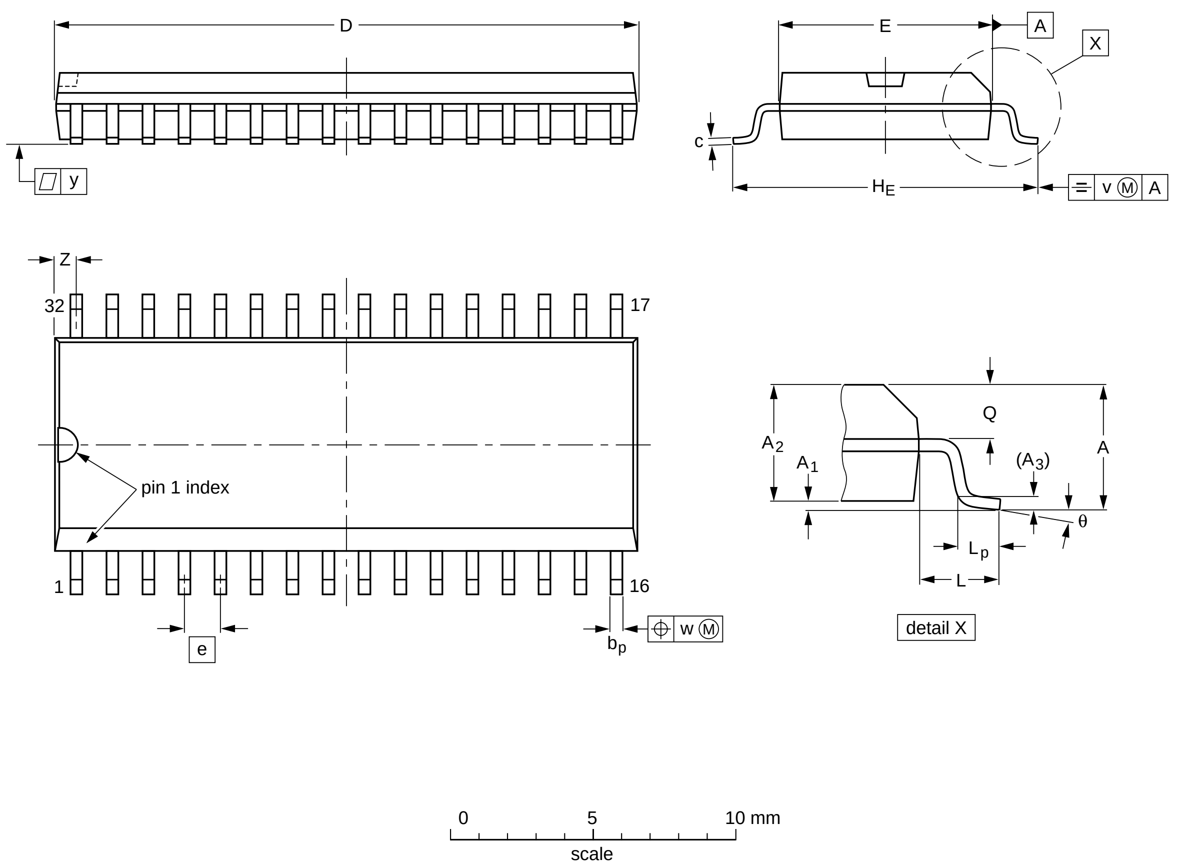
Remark: The power supply requires at least a 1000 μF capacitor.

Table 15. Snubber network: bill of materials

Item	Quantity	Reference	Part	Footprint
1	4	C27, C28, C29, C30	470 pF, 25 V	SMD 0805 X7R
2	4	R27, R28, R29, R30	10 / 0.25 W / 5 %	SMD 1206

14. Package outline

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT287-1		MO-119				~~00-08-17~~ 03-02-19

Fig 13. Package outline SOT287-1 (SO32)

15. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9815_1	20081216	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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