UBA2080; UBA2080A; UBA2081

Half-bridge driver IC

Rev. 3 — 18 June 2012 Product data sheet

1. General description

The UBA2080(A) and UBA2081 are high voltage monolithic integrated circuits made using the latch-up free Silicon-On-Insulator (SOI) process. The circuit is designed for driving MOSFETs in a half-bridge configuration.

2. Features and benefits

- Latch-up free and robust half bridge driver
- Output driver capability: $I_{O(sink)}$ = 400 mA and $I_{O(source)}$ = 200 mA
- Maximum frequency 800 kHz
- UBA2080:
  - Outputs in phase with HIN and LIN inputs
  - Overlap protection
- UBA2081:
  - Outputs in phase with CLK input
  - Adjustable dead-time
  - Low active shutdown input

3. Applications

- Driver (via external MOSFETs) for any kind of load in a half-bridge configuration
- UBA2080A:
  - Selectable between UBA2080 and UBA2081 functionality
  - Thermally enhanced package for high frequency operation.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UBA2080P	DIP8	plastic dual in-line package; 8 leads	SOT97-1
UBA2081P			
UBA2080T	SO8	plastic small outline package; 8 leads	SOT96-1
UBA2081T			
UBA2080AT	SO14	plastic small outline package; 14 leads	SOT108-1

5. Block diagram

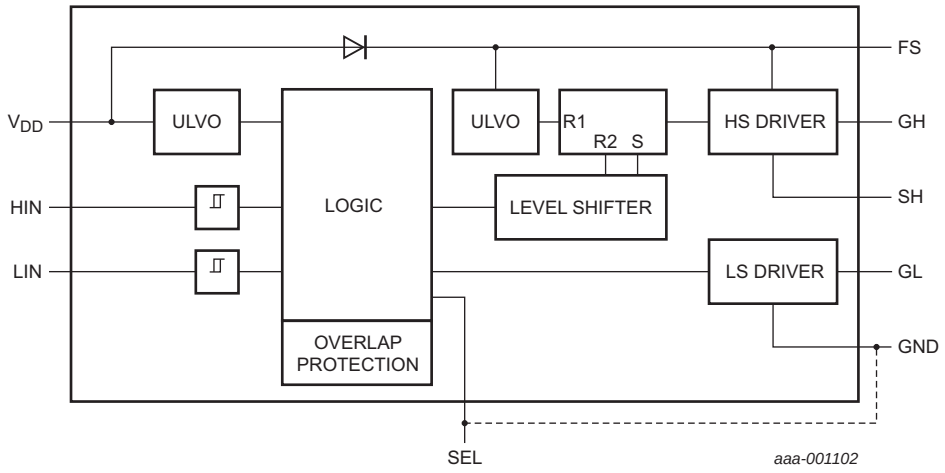


Fig 1. Block diagram (UBA2080 and UBA2080A with select = GND)

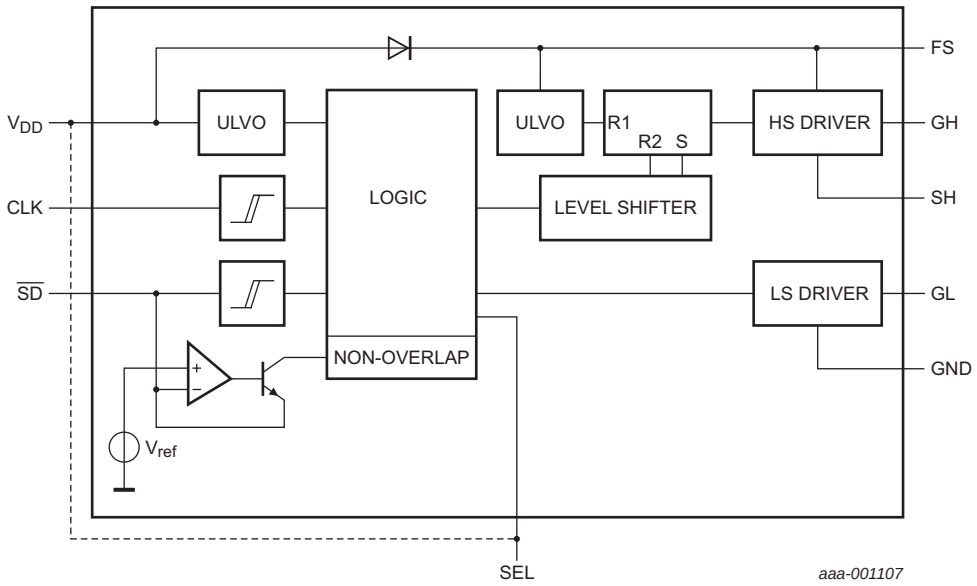


Fig 2. Block diagram (UBA2080A and UBA2081 with select = V_{DD})

Refer to Figure 7 and Figure 8 for detailed information on the required application components.

6. Pinning information

6.1 Pinning

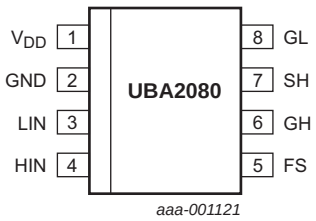


Fig 3. UBA2080: Pin configuration DIP8 and SO8 package

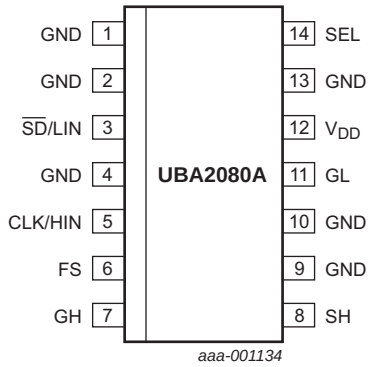


Fig 4. UBA2080A: Pin configuration SO14 package

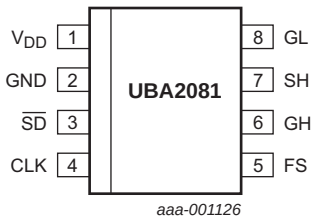


Fig 5. UBA2081: Pin configuration DIP8 and SO8 package

6.2 Pin description

Table 2. Pin description UBA2080/UBA2081 DIP8 and SO8

Symbol	Pin		Description
	UBA2080 (DIP8/SO8)	UBA2081 (DIP8/SO8)	
V_{DD}	1		IC supply
GND	2		IC ground and low-side driver return
LIN	3	-	low-side driver logic input
$\overline{SD}$	-	3	low active analog shutdown input and non-overlap time setting
HIN	4	-	high-side driver logic input
CLK	-	4	clock logic input
FS	5		floating supply voltage
GH	6		high-side MOSFET gate
SH	7		high-side MOSFET source
GL	8		low-side MOSFET gate

Table 3. Pin description UBA2080AT (SO14)

Symbol	Pin	Description
GND	1, 2, 4, 9, 10, 13	IC ground and low side driver return
$\overline{SD}$/LIN	3	low-side driver logic input or low active shutdown and non-overlap time setting
CLK/HIN	5	high-side driver logic input or clock logic input
FS	6	floating supply voltage
SH	8	high-side MOSFET source

Table 3. Pin description UBA2080AT (SO14) *...continued*

Symbol	Pin	Description
GH	7	high-side MOSFET gate
GL	11	low-side MOSFET gate
V_{DD}	12	IC supply
SEL	14	select UBA2080 or UBA2081 functionality; only connect to GND or V_{DD}

7. Functional description

7.1 Start-up state

The IC enters the start-up state when the supply voltage on pin V_{DD} increases. In the start-up state, the high-side power transistor is non-conducting and the low-side power transistor is switched on. The internal circuit is reset and the capacitor on the bootstrap pin FS is charged. The start-up state is defined until the value of V_{DD} = the $V_{DD(start)}$ value. After which the IC switches to the oscillation state.

The circuit enters the start-up state again when the voltage on pin $V_{DD} < V_{DD(stop)}$.

7.2 UBA2080 oscillation state

In the oscillation state, the output voltage of the GL and GH drivers depend on the logical signals HIN and LIN (see Table 4).

To prevent cross conduction in the half-bridge MOSFETs, the combination HIN = LIN = 1 is not allowed. Both GL and GH are LOW under this condition.

Table 4. UBA2080 Logic table

State	HIN	LIN	GH	GL
Start-up	-	-	LOW	HIGH
Oscillation	0	0	LOW	LOW
Oscillation	0	1	LOW	HIGH
Oscillation	1	0	HIGH	LOW
Oscillation	1	1	LOW	LOW

7.3 UBA2081 oscillation state

In the oscillation state, the output voltage of the GL and GH drivers depend on the logical signals CLK and SD (see Table 5).

Table 5. UBA2081 Logic table

State	CLK	SD	GH	GL
Start-up	-	-	LOW	HIGH
Oscillation	0	0	LOW	HIGH
Oscillation	1	0	HIGH	LOW
Oscillation	0	1	LOW	LOW
Oscillation	1	1	LOW	LOW

7.4 UBA2081 non-overlap time

The external resistor (R_{SD}) on pin SD sets the non-overlap time of the UBA2081. The relationship between this resistor value and actual dead-time is listed in Figure 6.

It is essential to add a 10 nF to 100 nF decoupling capacitor across R_{SD} to ensure a noise immune dead-time system.

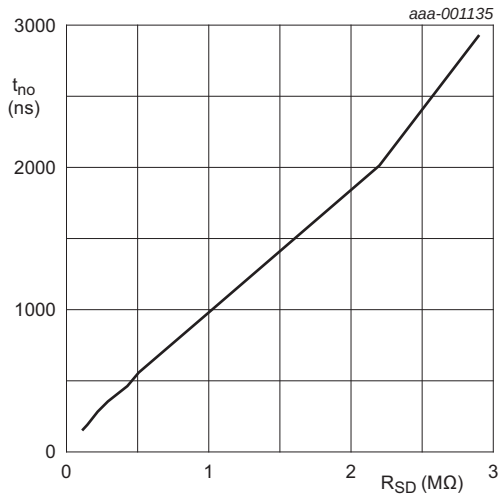


Fig 6. Non-overlap time versus SD resistor (R_{SD})

7.5 UBA2081 shutdown protection

When the voltage at pin $\overline{SD}$ is pulled below V_{IH}, the internal sink drivers of the pins GL and GH are immediately enabled to switch off the external power MOSFETs.

The shutdown comparator has a hysteresis of $V_{hys(\overline{SD})}$ to avoid multiple switching.

Preferably, pin $\overline{SD}$ is pulled low via a collector of a transistor (see application schematic) to avoid loading of this pin (Influences the non-overlap time settings) at normal operation.

7.6 UBA2080 overlap protection

The internal logic takes care that the GL driver and GH driver are both set to LOW in this situation to avoid that HIN = LIN = 1 causes a cross current in the external half-bridge.

7.7 UBA2080A select function

Pin SEL enables the selection of either the UBA2080 or the UBA2081 functionality. SEL = 0 gives the UBA2080 functionality. SEL = V_{DD} gives the UBA2081 functionality.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage	nominal		0	15.5	V
V_{FS}	voltage on pin FS			V_{SH}	V_{SH} + 15.5	V
V_{SH}	voltage on pin SH	source high-side MOSFET		–3	+600	V
		t < 1 µs		–14	+600	V
$V_{i(HIN)}$	input voltage on pin HIN	logic input for high-side driver		0	15.5	V
$V_{i(LIN)}$	input voltage on pin LIN	logic input for low-side driver		0	15.5	V
$V_{i(SEL)}$	input voltage on pin SEL			0	15.5	V
V_{CLK}	voltage on pin CLK	logic input for output drivers		0	15.5	V
$V_{i(SD)}$	input voltage on pin SD	logic input for output drivers and analog input for non-overlap setting		0	15.5	V
SR	slew rate	on pin SH; repetitive		–6	+6	V/ns
T_j	junction temperature			–40	+150	°C
T_{amb}	ambient temperature			–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C
V_{ESD}	electrostatic discharge voltage	human body model:	[1]			
		pins FS, GH and SH		-	1	kV
		pins V_{DD}, HIN, LIN, SD, CLK, SEL		-	2	kV
		machine model:	[2]			
		all pins		-	250	V

[1] In accordance with the Human Body Model (HBM): equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] In accordance with the Machine Model (MM): equivalent to discharging a 200 pF capacitor through a 1.5 kΩ series resistor and a 0.75 µH inductor.

9. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
SO8					
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	160	K/W
SO14 and DIP8					
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	100	K/W

[1] In accordance with IEC 60747-1.

10. Characteristics

Table 8. Characteristics

T_j = 25 °C; all voltages are measured with respect to SGND; V_{DD} = 12.8 V; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-voltage supply						
I_{leak}	leakage current	FS = GH = SH = 600 V	-	-	10	µA
Start-up state						
I_{VDD}	current on pin V_{DD}		420	520	620	µA
$V_{DD(start)}$	start supply voltage		11	12	13	V
$V_{DD(stop)}$	stop supply voltage		8	8.5	9	V
$V_{DD(hys)}$	hysteresis of supply voltage	start-to-stop	3	3.5	4	V
Pin LIN input						
V_{IH}	HIGH-level input voltage		1.6	2.2	2.8	V
$V_{hys(LIN)}$	hysteresis voltage on pin LIN		-	400	-	mV
$I_{I(LIN)}$	input current on pin LIN		-	0	1	µA
Pin HIN input						
V_{IH}	HIGH-level input voltage		1.6	2.2	2.8	V
$V_{hys(HIN)}$	hysteresis voltage on pin HIN		-	400	-	mV
$I_{I(HIN)}$	input current on pin HIN		-	0	1	µA
Pin CLK input						
V_{IH}	HIGH-level input voltage		2.7	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
$I_{I(CLK)}$	input current on pin CLK		-	0	1	µA
Pin SD input						
V_{IH}	HIGH-level input voltage	to activate shutdown	1.6	2.2	2.8	V
$V_{hys(SD)}$	hysteresis voltage on pin SD		-	400	-	mV
t_{no}	non-overlap time	R_{SD} = 100 kΩ; typical minimum	-	140	-	ns
		R_{SD} = 3 MΩ; typical maximum	-	2.4	-	µs
Pin SEL input						
$I_{I(SEL)}$	input current on pin SEL		-	0	1	µA
gate drivers						
$I_{O(source)}$	output source current	$V_{FS} = V_{VDD}$ = 12 V; V_{SH} = 0 V; $V_{GH} = V_{GL}$ = 8 V	-	200	-	mA
$I_{O(sink)}$	output sink current	$V_{FS} = V_{VDD}$ = 12 V; V_{SH} = 0 V; $V_{GH} = V_{GL}$ = 4 V	-	400	-	mA
$V_{d(bs)}$	bootstrap diode voltage	$I_{d(bs)}$ = 20 mA	-	2.3	-	V
V_{UVLO}	undervoltage lockout voltage	reset	3.6	4.2	4.8	V
I_{FS}	current on pin FS	$V_{FS} = V_{VDD}$ = 12 V; V_{SH} = 0 V	27	32	37	µA
Timing						
t_{PD}	propagation delay	UBA2080; matching; $C_{(GL)} = C_{(GH)}$ = 0, propagation time difference between GL and GH.	-	50	-	ns

Table 8. Characteristics *…continued*

T_j = 25 °C; all voltages are measured with respect to SGND; V_{DD} = 12.8 V; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PD(LIN-GL)}$	propagation delay from LIN to GL	UBA2080; $C_{(GL)}$ = 0 pF	-	240	-	ns
$t_{PD(HIN-GH)}$	propagation delay from HIN to GH	UBA2080; $C_{(GH)}$ = 0 pF	-	180	-	ns
f_{max}	maximum frequency		800	-	-	kHz

11. Application information

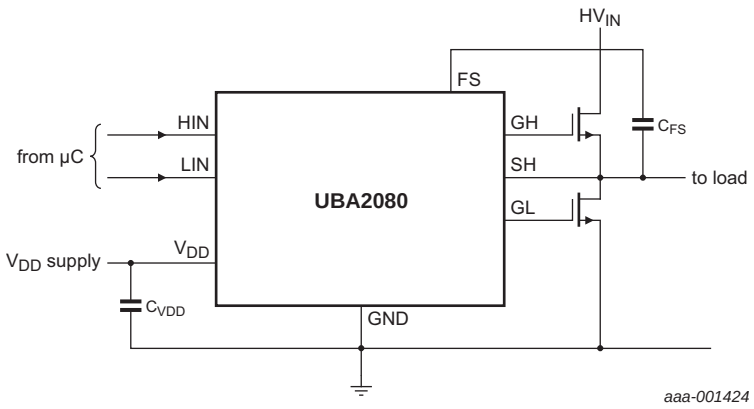
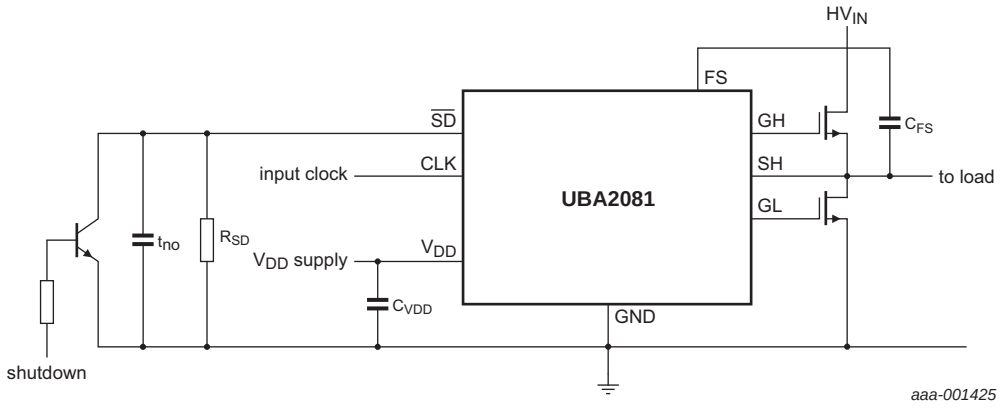


Fig 7. Typical UBA2080 application

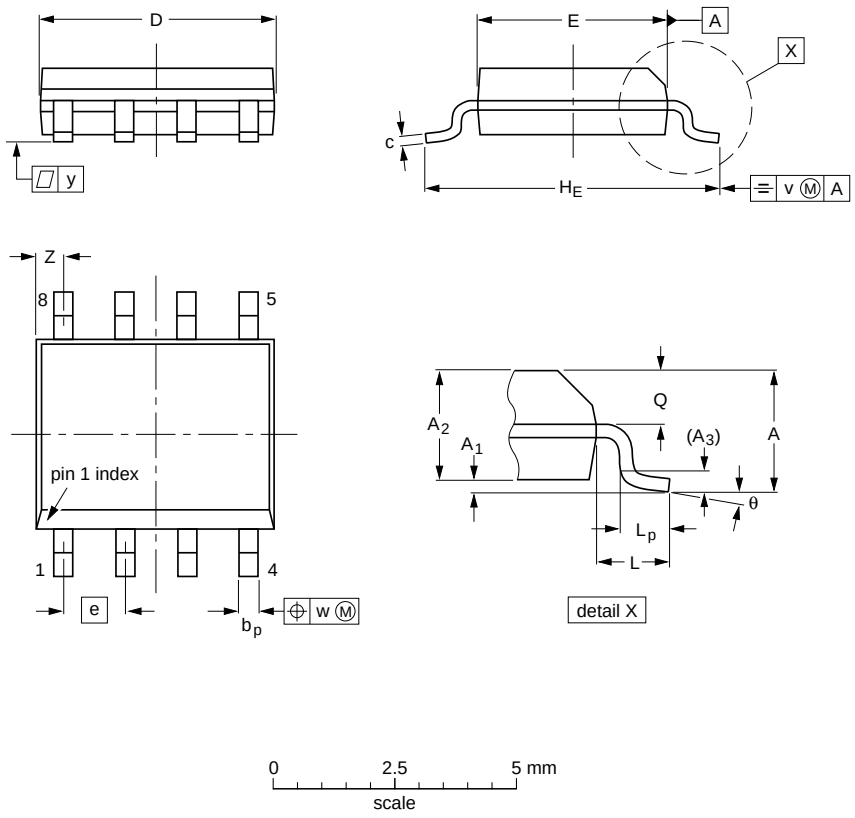


Remark: The capacitor connected to the $\overline{SD}$ pin ensures a noise immune dead-time.

Fig 8. Typical UBA2081 application

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

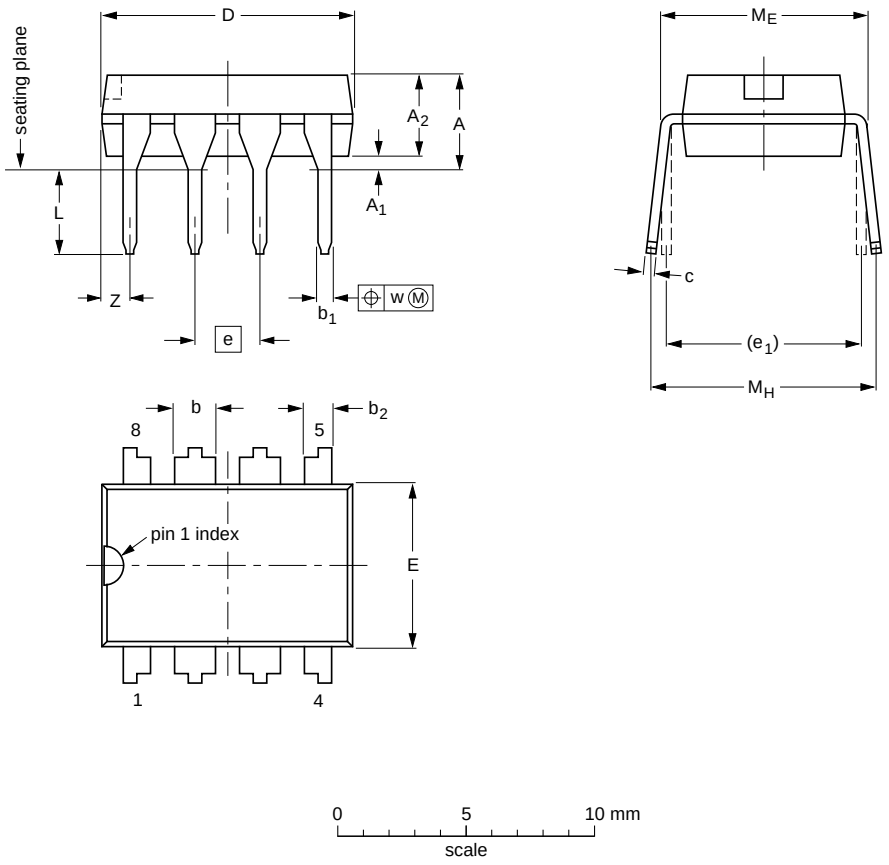
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 9. Package outline SOT96-1 (SO8)

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

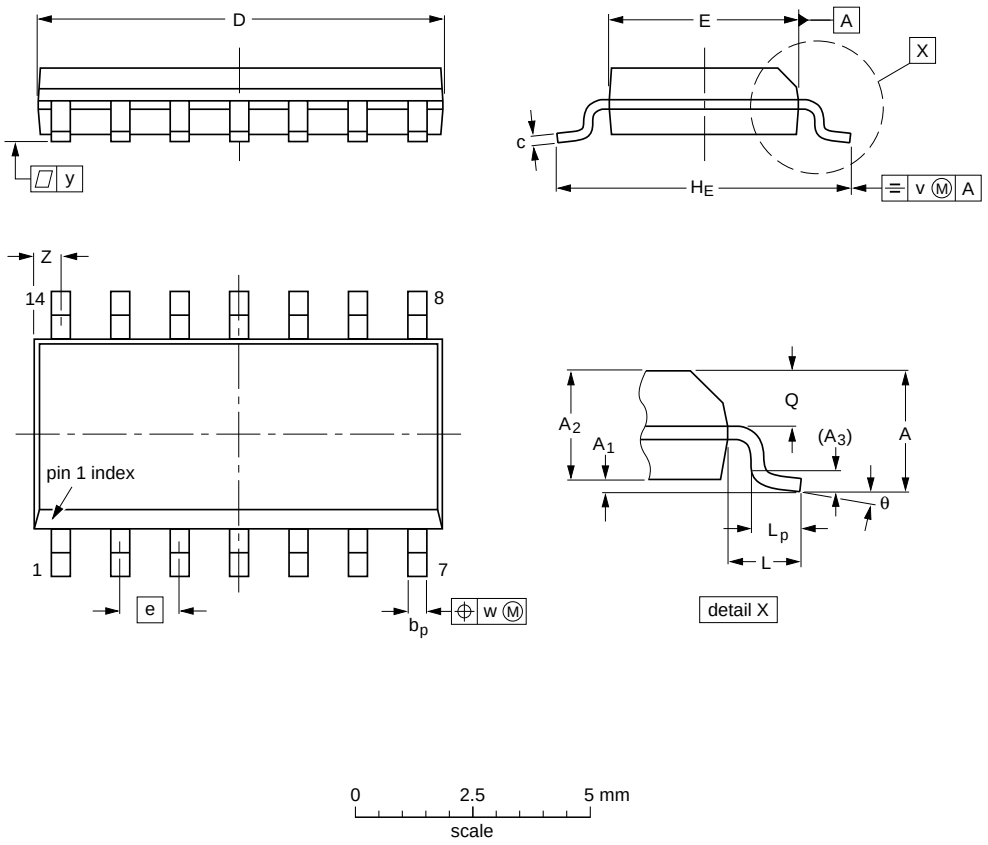
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT97-1 (DIP8)

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

13. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA2080_UBA2081 v.3	20120618	Product data sheet	-	UBA2080_UBA2081 v.2
Modifications:	• Data sheet status changed from Preliminary to Product. • Table 6 “Limiting values” has been updated.			
UBA2080_UBA2081 v.2	20120426	Preliminary data sheet	-	UBA2080_UBA2081 v 1.1
UBA2080_UBA2081 v.1.1	20111206	Objective data sheet	-	UBA2080_UBA2081 v.1
UBA2080_UBA2081 v.1	20111116	Objective data sheet	-	

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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