



# Z0103MN

4Q Triac

26 August 2013

Product data sheet

## 1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT223 (SC-73) surface-mountable plastic package intended for applications requiring direct interfacing to logic level ICs and low power gate drivers.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants
- Very sensitive gate in four quadrants

## 3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

## 4. Quick reference data

Table 1. Quick reference data

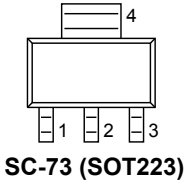
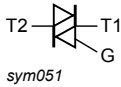
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{DRM}}$	repetitive peak off-state voltage		-	-	600	V
$I_{\text{TSM}}$	non-repetitive peak on-state current	full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_{\text{p}} = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	8	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{sp}} \leq 105\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	1	A
<b>Static characteristics</b>						
$I_{\text{GT}}$	gate trigger current	$V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2+ G+; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 9</a>	-	-	3	mA
		$V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 0.1\text{ A}$ ; T2+ G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 9</a>	-	-	3	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2\text{- G-};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	-	3	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2\text{- G+};$ $T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 9</a>	-	-	5	mA

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>SC-73 (SOT223)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
4	T2	main terminal 2		

## 6. Ordering information

Table 3. Ordering information

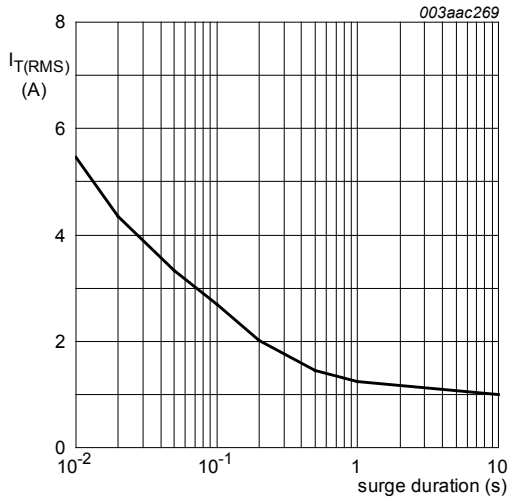
Type number	Package		
	Name	Description	Version
Z0103MN	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

## 7. Limiting values

**Table 4. Limiting values**

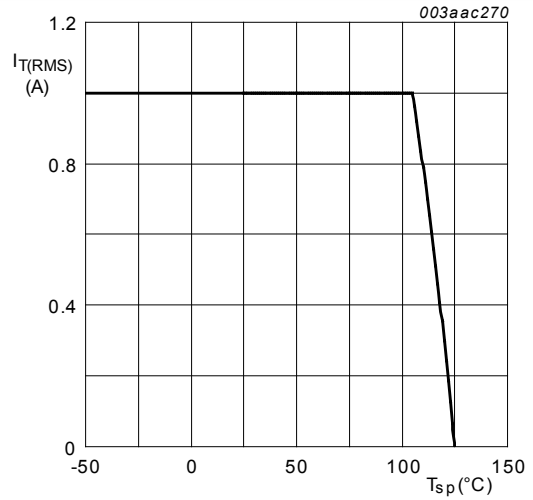
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 105\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	1	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	8	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	8.5	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	0.32	$A^2s$
$di_T/dt$	rate of rise of on-state current	$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu s$ ; T2+ G+	-	50	$A/\mu s$
		$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu s$ ; T2+ G-	-	50	$A/\mu s$
		$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu s$ ; T2- G-	-	50	$A/\mu s$
		$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu s$ ; T2- G+	-	20	$A/\mu s$
$I_{GM}$	peak gate current		-	1	A
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}C$
$T_j$	junction temperature		-	125	$^{\circ}C$

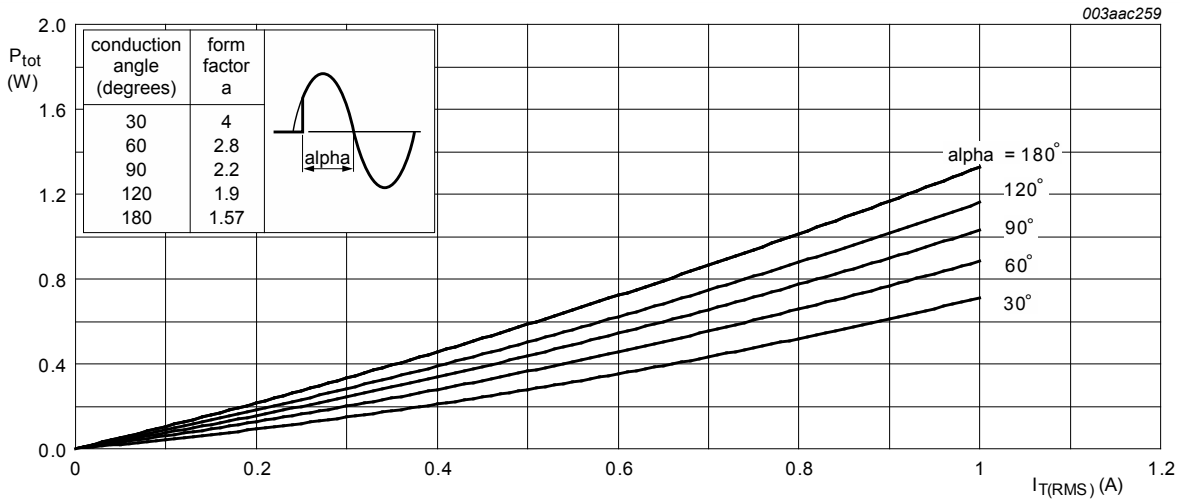


$f = 50 \text{ Hz}; T_{sp} = 105 \text{ }^\circ\text{C}$

**Fig. 1. RMS on-state current as a function of surge duration; maximum values**

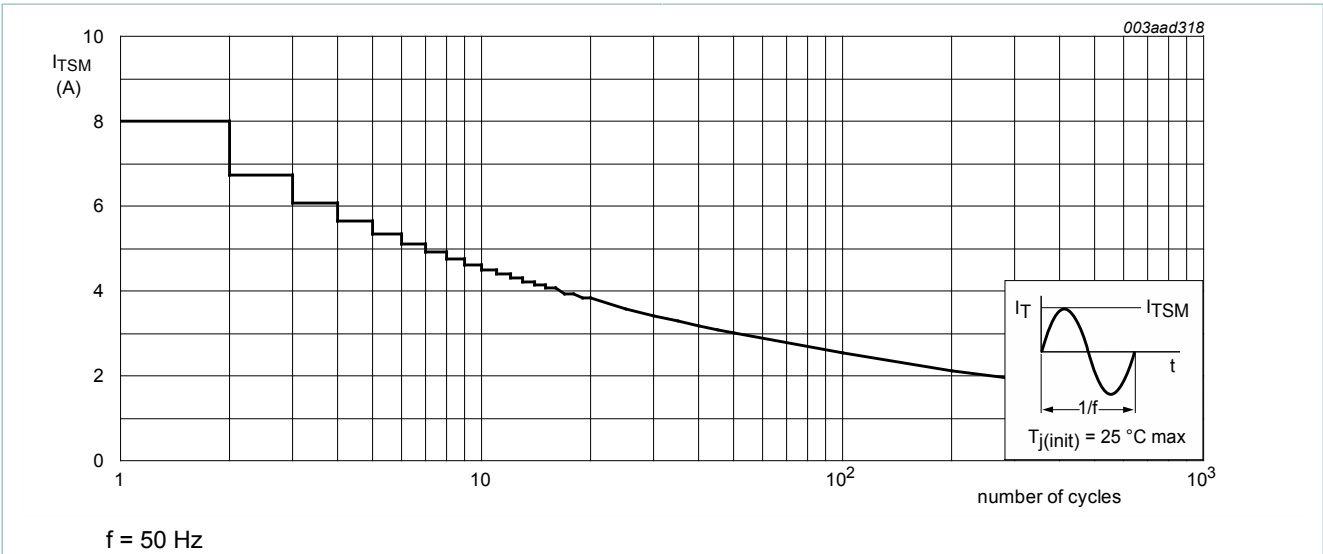


**Fig. 2. RMS on-state current as a function of solder point temperature; maximum values**

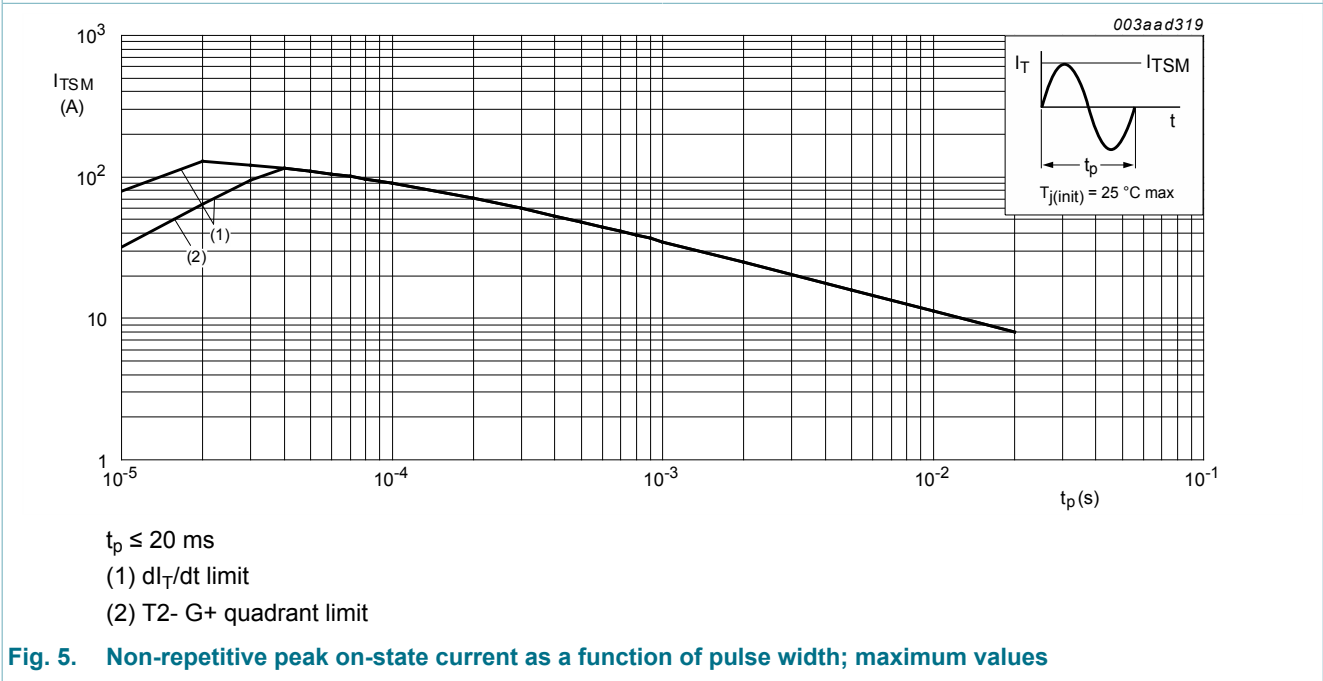


alpha = conduction angle  
 a = form factor =  $I_{T(RMS)} / I_{T(AV)}$

**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**



**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**

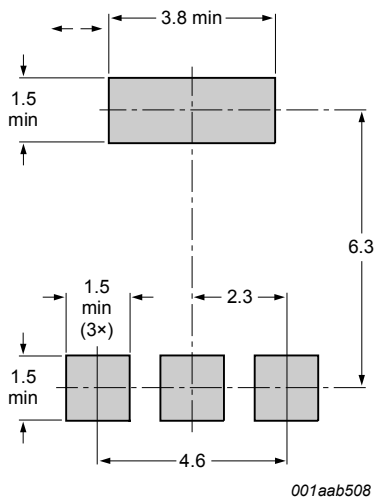


**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

## 8. Thermal characteristics

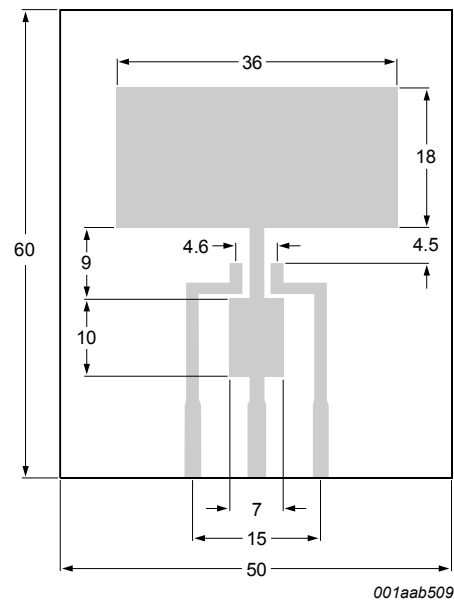
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle; <a href="#">Fig. 8</a>	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; printed circuit board mounted; minimum footprint; <a href="#">Fig. 6</a>	-	156	-	K/W
		full cycle; printed circuit board mounted; pad area; <a href="#">Fig. 7</a>	-	70	-	K/W



All dimensions are in mm

Fig. 6. Minimum footprint SOT223



All dimensions are in mm

Printed circuit board:

FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 7. Printed circuit board pad area: SOT223

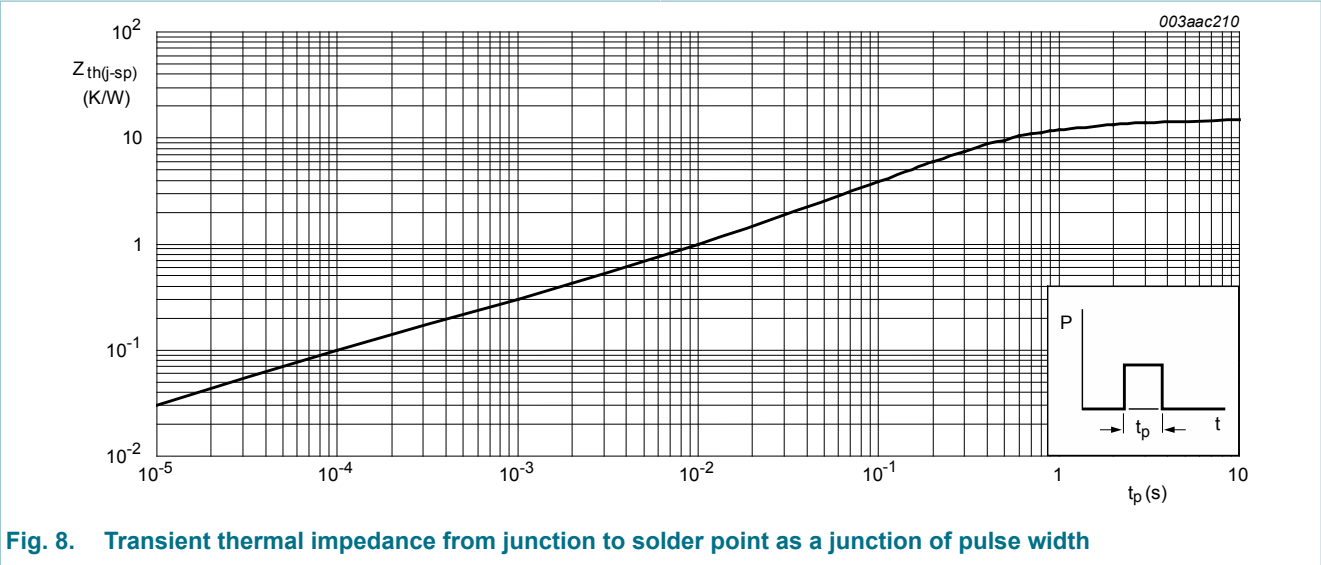


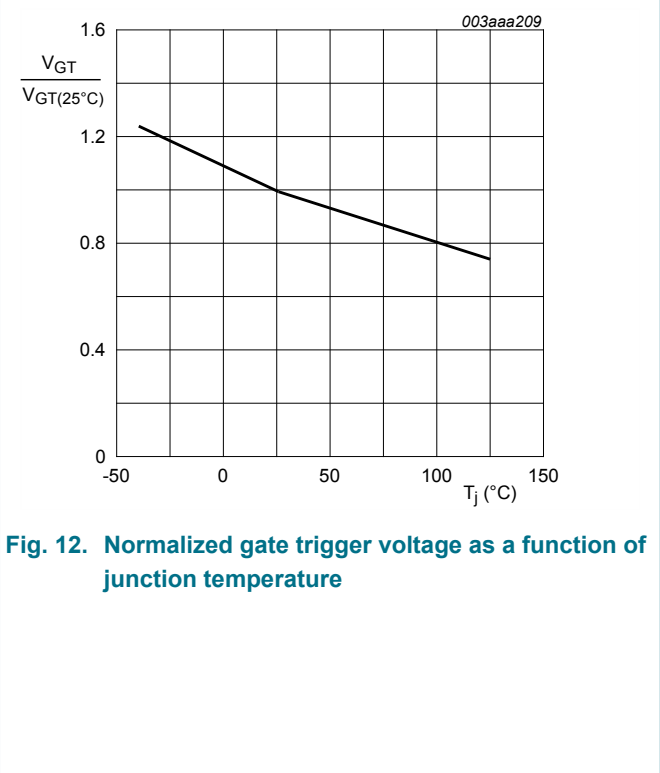
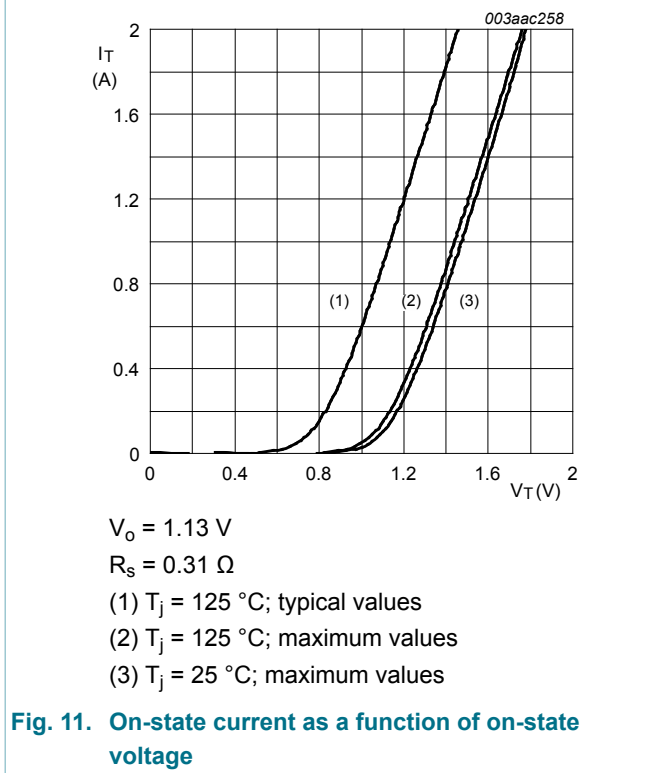
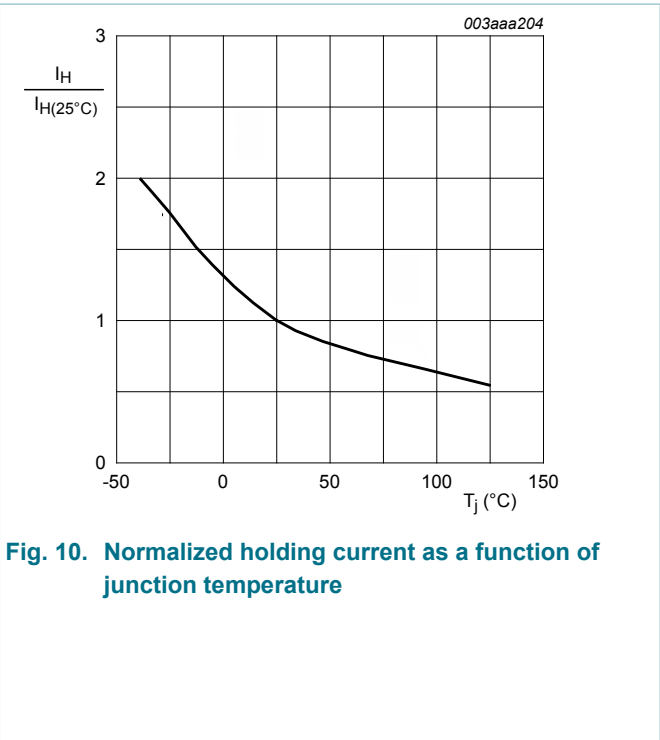
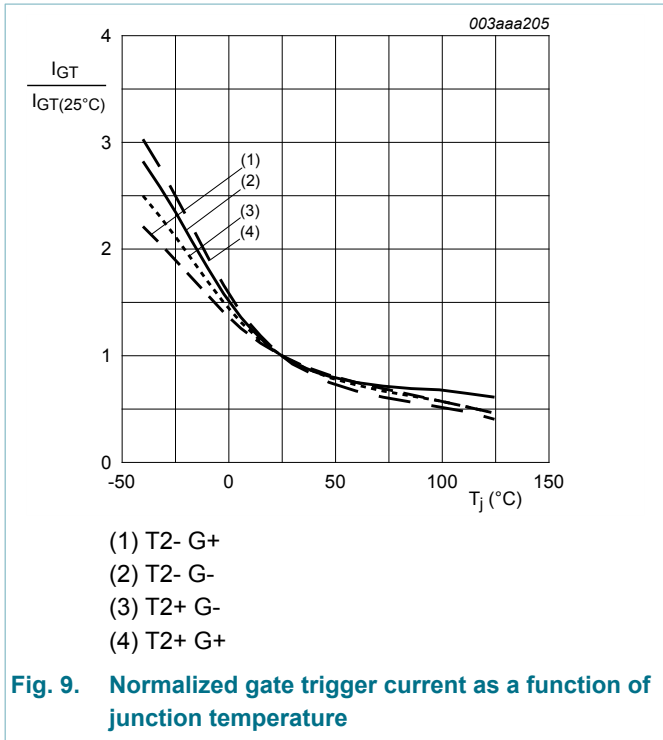
Fig. 8. Transient thermal impedance from junction to solder point as a junction of pulse width

## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	-	3	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	-	3	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	-	3	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	-	5	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	-	7	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	-	15	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	-	7	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	-	7	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	-	7	mA
$V_T$	on-state voltage	$I_T = 1.4\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	1.3	1.6	V
$V_{GT}$	gate trigger voltage	$V_D = 600\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ °C}$	0.2	-	-	V
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	-	1	V
$I_D$	off-state current	$V_D = 600\text{ V}$ ; $T_j = 125\text{ °C}$	-	-	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 110\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 13</a>	10	-	-	V/ $\mu$ s
$dV_{com}/dt$	rate of change of commutating voltage	$V_D = 400\text{ V}$ ; $T_j = 110\text{ °C}$ ; $dI_{com}/dt = 0.44\text{ A/ms}$ ; gate open circuit	0.5	-	-	V/ $\mu$ s





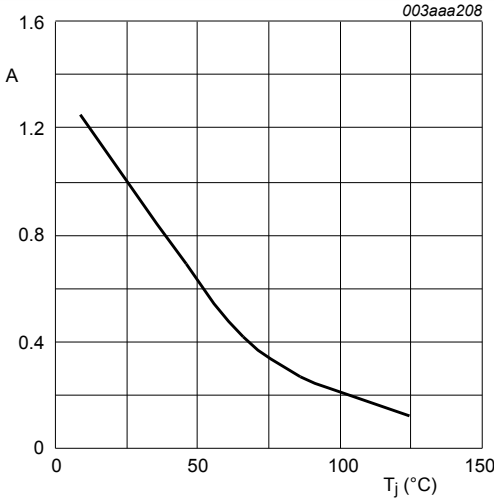


Fig. 13. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

$$A = \frac{dV_{D(T_j \text{ } ^\circ\text{C})} / dt}{dV_{D(25 \text{ } ^\circ\text{C})} / dt}$$

### 10. Package outline

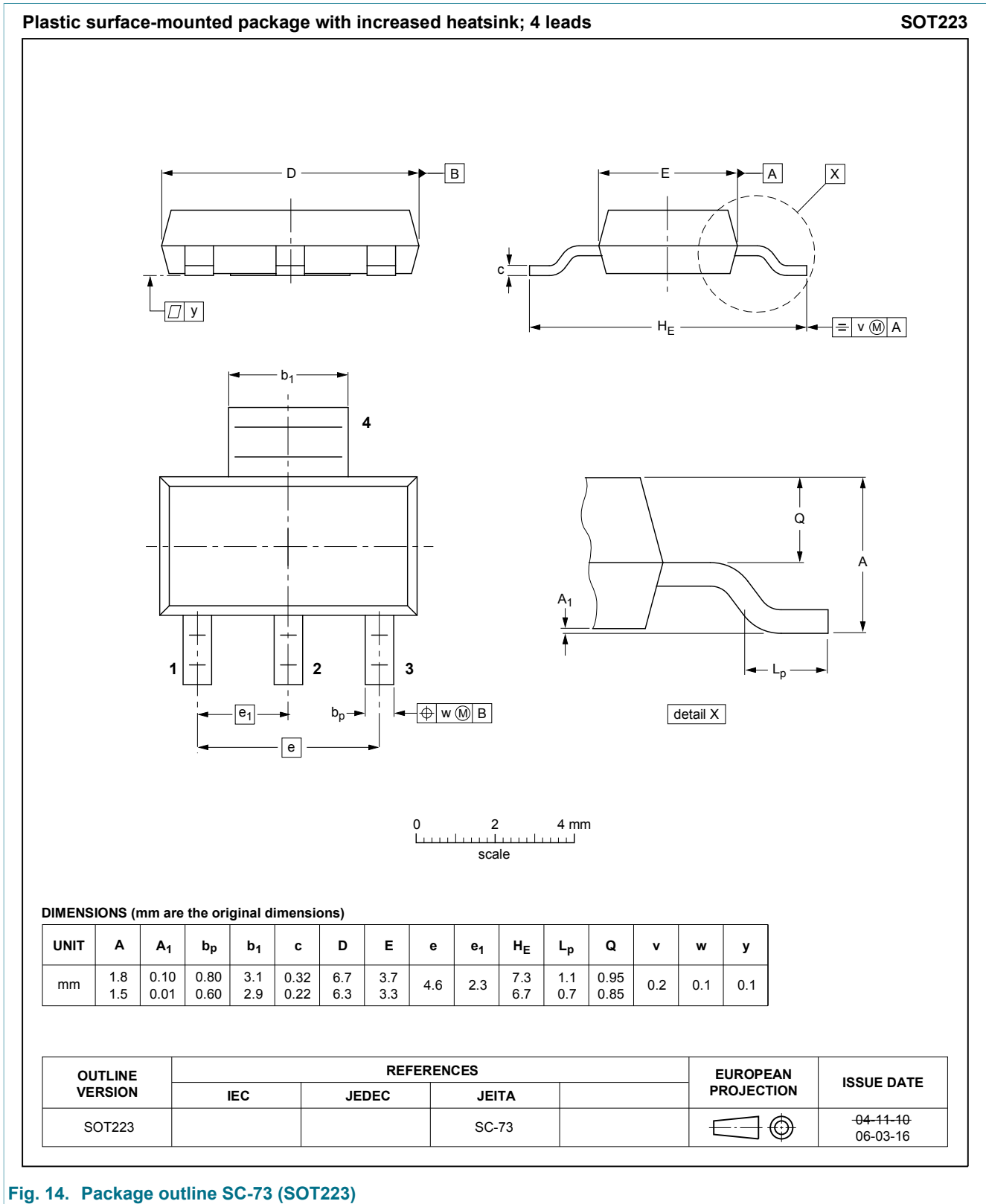


Fig. 14. Package outline SC-73 (SOT223)



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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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