



Z0109MA0

4Q Triac

23 August 2013

Product data sheet

1. General description

Planar passivated sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring enhanced noise immunity and direct interfacing to logic ICs and low power gate drivers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage of 600V
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate in four quadrants
- Triggering in all four quadrants

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

4. Quick reference data

Table 1. Quick reference data

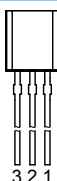
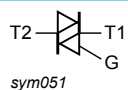
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|--|-----|-----|------|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 600 | V |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 12.5 | A |
| $I_{\text{T(RMS)}}$ | RMS on-state current | full sine wave; $T_{\text{lead}} \leq 45\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 1 | A |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G+; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7 | 0.4 | - | 10 | mA |
| | | $V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$; Fig. 7 | 0.4 | - | 10 | mA |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
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| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.4 | - | 10 | mA |
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5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|--|---|
| 1 | T2 | main terminal 2 |  <p>TO-92 (SOT54)</p> |  <p>sym051</p> |
| 2 | G | gate | | |
| 3 | T1 | main terminal 1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|---|---------|
| | Name | Description | Version |
| Z0109MA0 | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--------------------------------------|---|-----|------|------------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| $I_{\text{T(RMS)}}$ | RMS on-state current | full sine wave; $T_{\text{lead}} \leq 45\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 1 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 12.5 | A |
| | | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 16.7\text{ ms}$ | - | 13.8 | A |
| I^2t | I^2t for fusing | $t_{\text{p}} = 10\text{ ms}$; SIN | - | 0.78 | A^2s |
| di_{T}/dt | rate of rise of on-state current | $I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $dI_{\text{G}}/dt = 100\text{ mA}/\mu\text{s}$; T2+ G+ | - | 50 | $\text{A}/\mu\text{s}$ |
| | | $I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $dI_{\text{G}}/dt = 100\text{ mA}/\mu\text{s}$; T2+ G- | - | 50 | $\text{A}/\mu\text{s}$ |
| | | $I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $dI_{\text{G}}/dt = 100\text{ mA}/\mu\text{s}$; T2- G- | - | 50 | $\text{A}/\mu\text{s}$ |
| | | $I_{\text{T}} = 1\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $dI_{\text{G}}/dt = 100\text{ mA}/\mu\text{s}$; T2- G+ | - | 20 | $\text{A}/\mu\text{s}$ |
| I_{GM} | peak gate current | | - | 1 | A |
| P_{GM} | peak gate power | | - | 2 | W |
| $P_{\text{G(AV)}}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| T_{stg} | storage temperature | | -40 | 150 | $^{\circ}\text{C}$ |
| T_{j} | junction temperature | | - | 125 | $^{\circ}\text{C}$ |

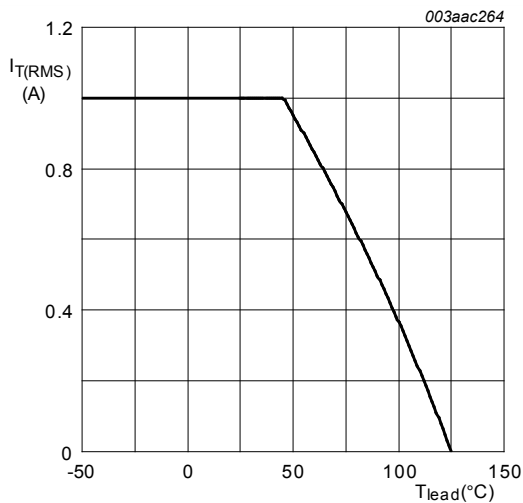
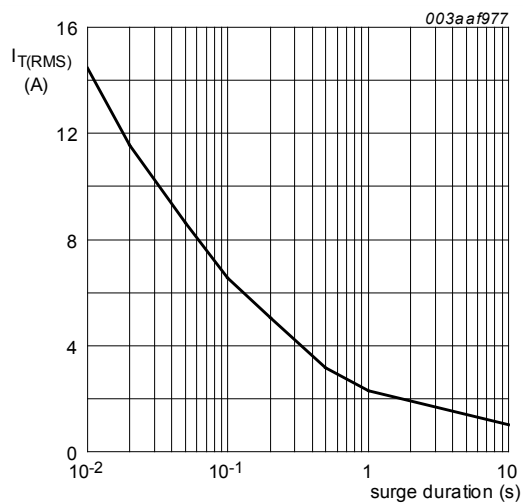
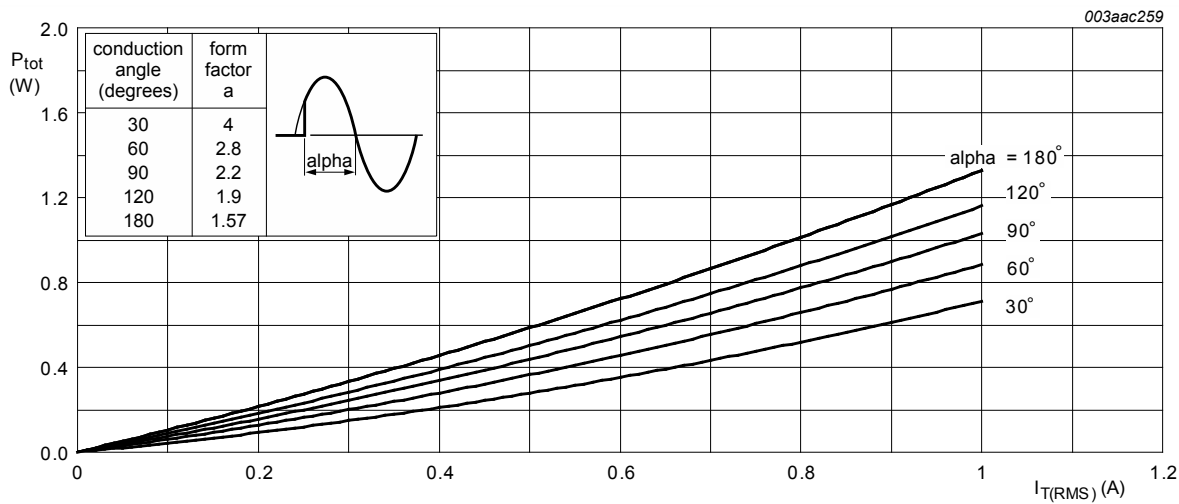


Fig. 1. RMS on-state current as a function of lead temperature; maximum values



$f = 50\text{ Hz}$; $T_{lead} = 45\text{ }^{\circ}C$

Fig. 2. RMS on-state current as a function of surge duration; maximum values



alpha = conduction angle

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

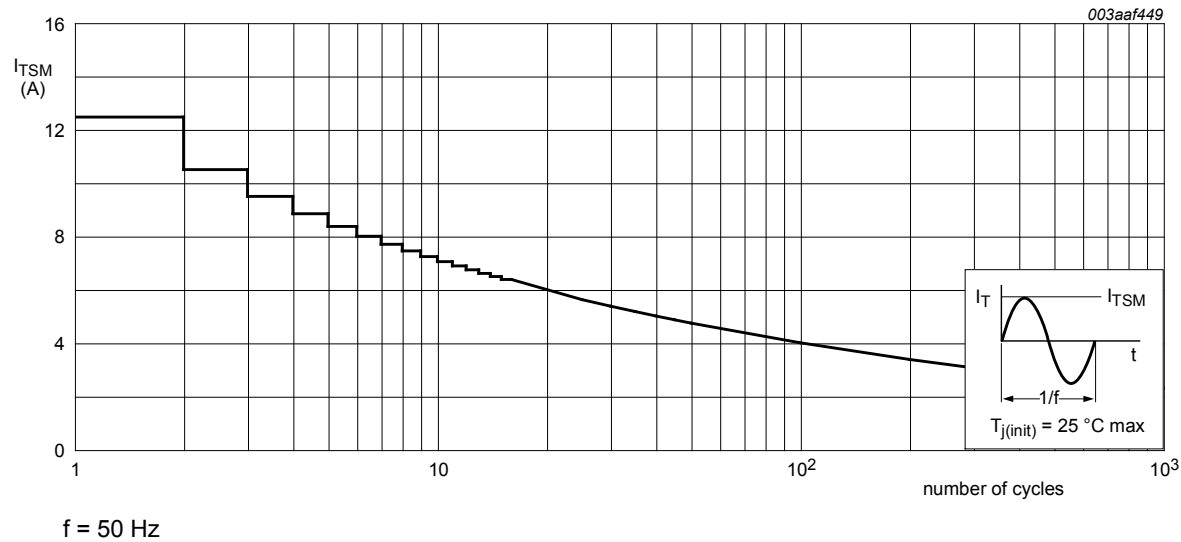


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

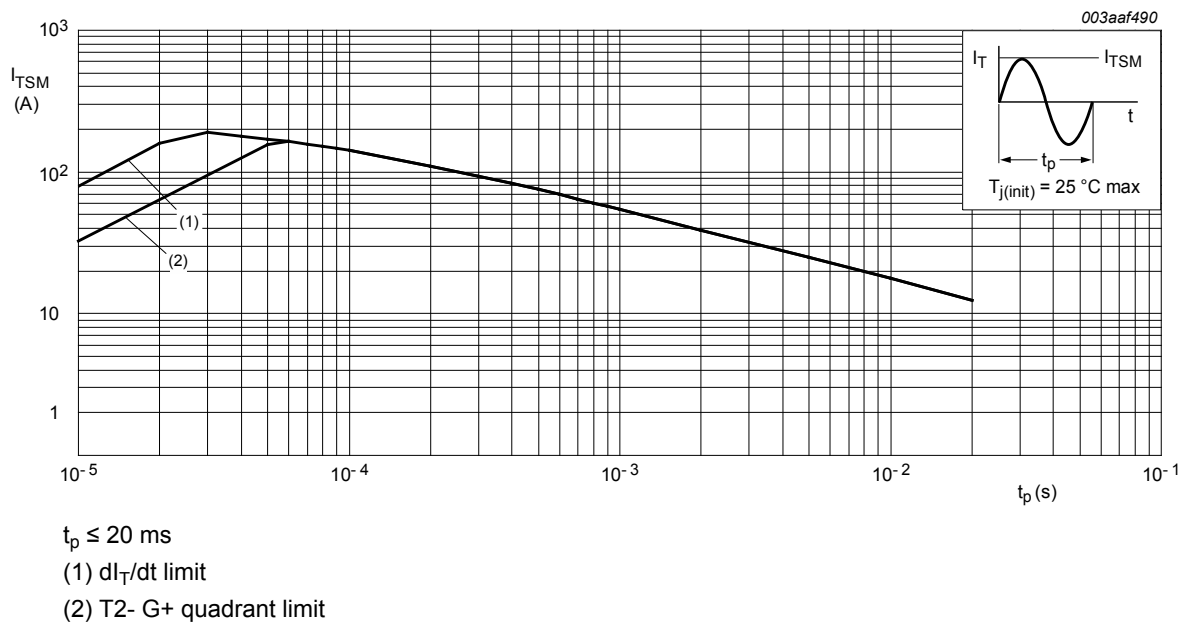


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|------------------|---|---|--|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead | full cycle; Fig. 6 | | - | - | 60 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | full cycle; printed circuit board mounted; lead length 4 mm | | - | 150 | - | K/W |

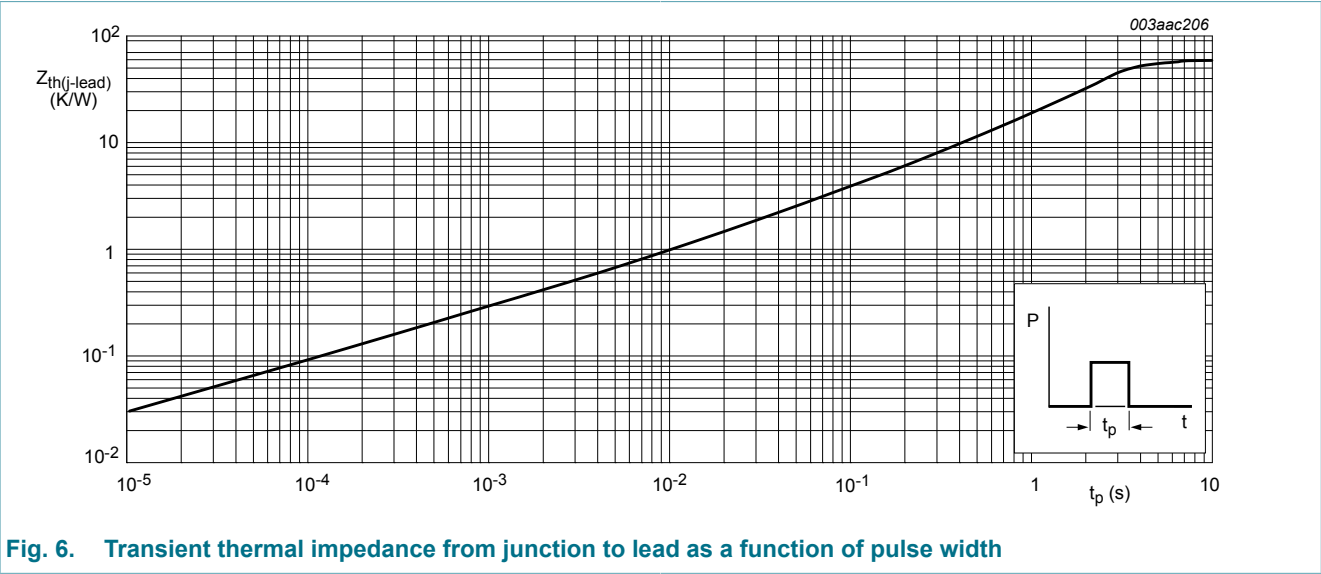
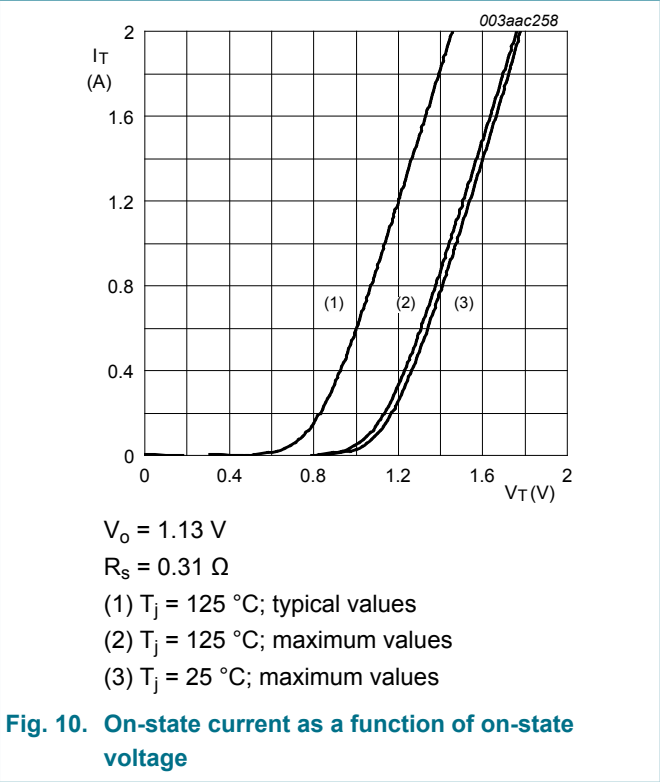
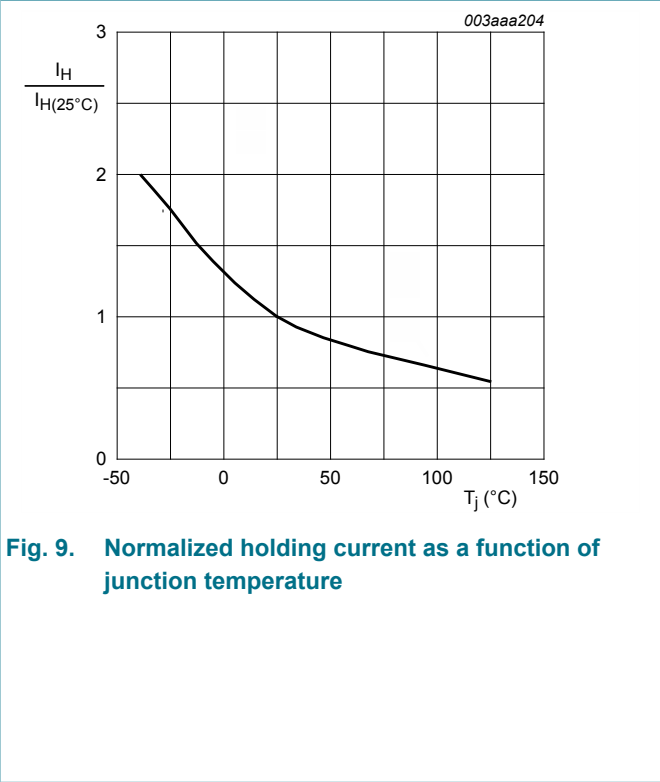
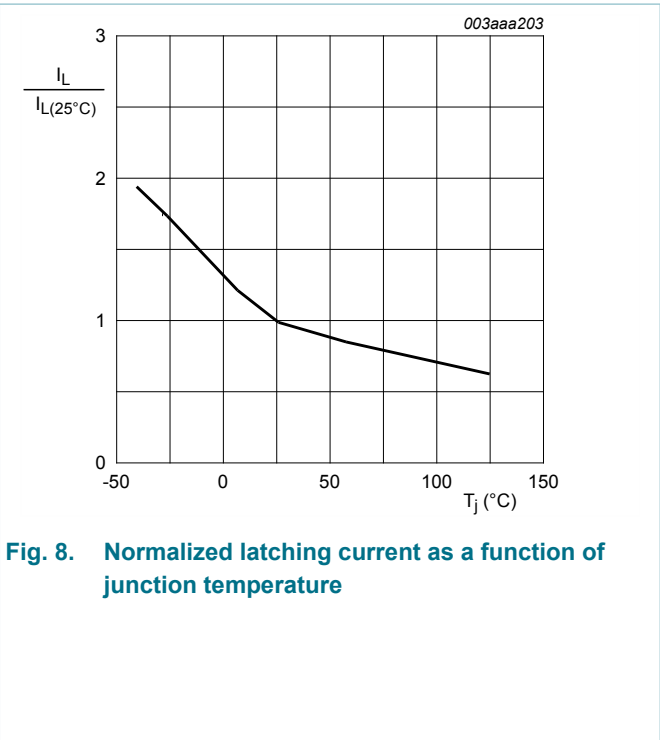
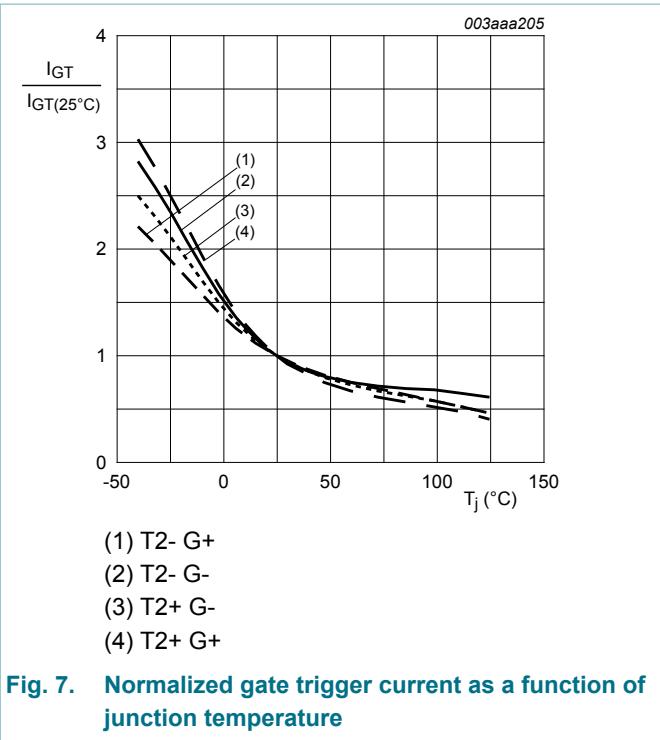


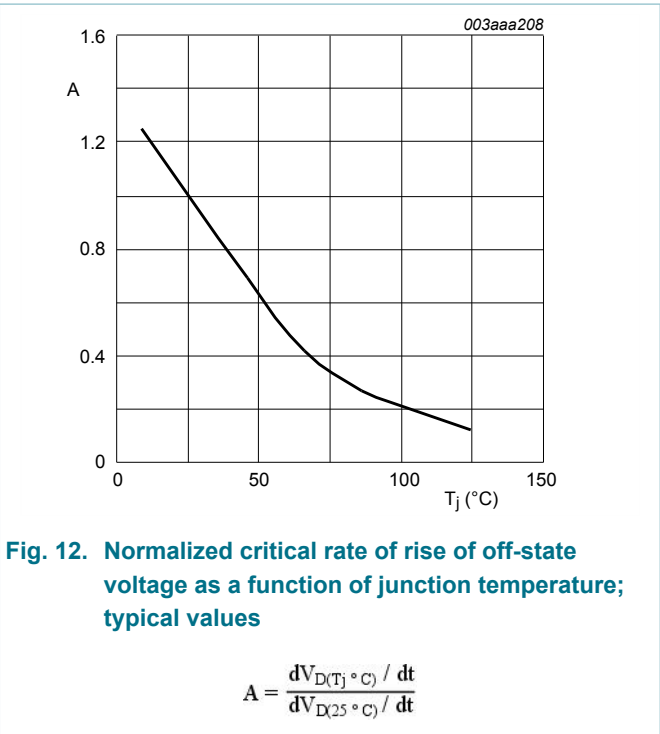
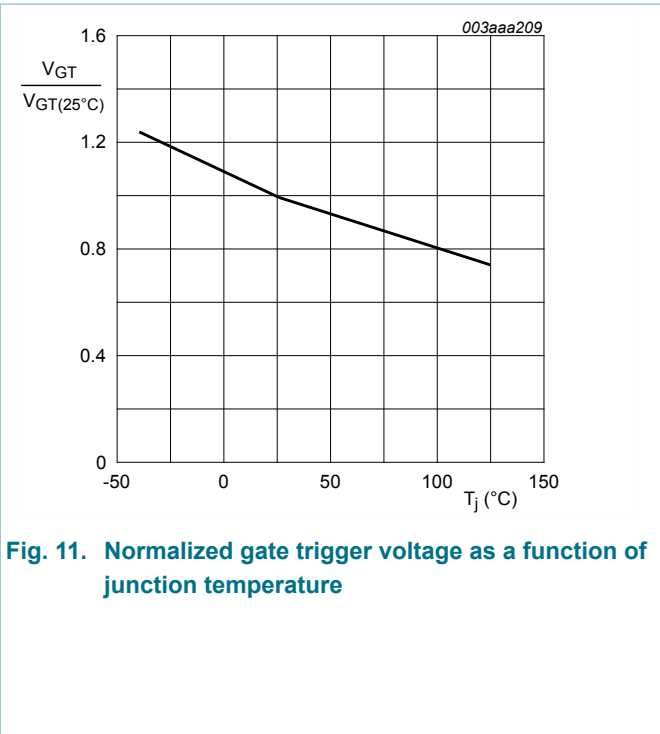
Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|-----|-----|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.4 | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.4 | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.4 | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7 | 0.4 | - | 10 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 15 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 30 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 15 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8 | - | - | 15 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 10 | mA |
| V_T | on-state voltage | $I_T = 1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | 1.3 | 1.6 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | - | - | 1 | V |
| | | $V_D = 600\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11 | 0.2 | - | - | V |
| I_D | off-state current | $V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$ | - | - | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12 | 120 | - | - | V/ μs |
| dV_{com}/dt | rate of change of commutating voltage | $V_D = 400\text{ V}$; $T_j = 110\text{ }^\circ\text{C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; gate open circuit | 2 | - | - | V/ μs |





10. Package outline

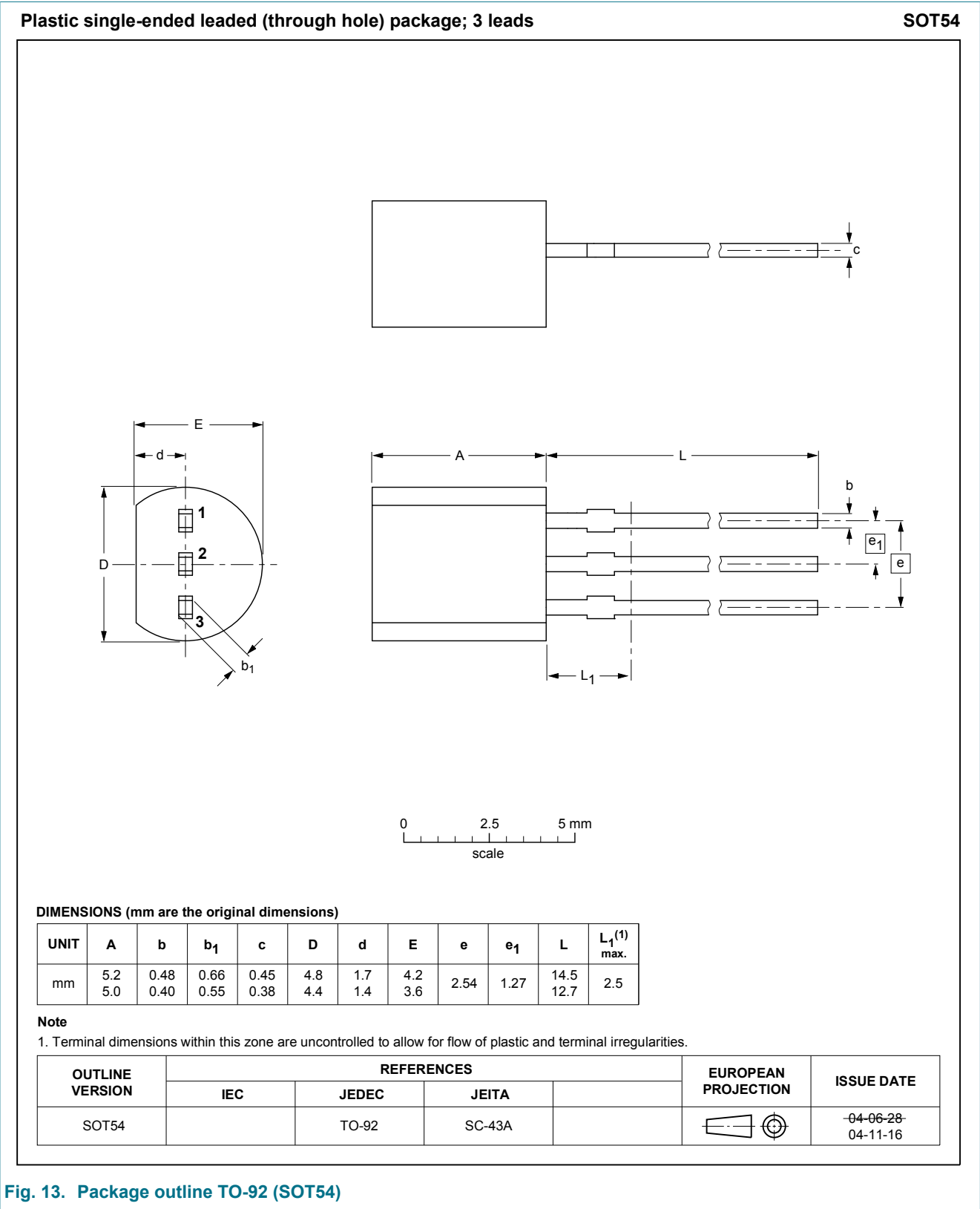


Fig. 13. Package outline TO-92 (SOT54)

11. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
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