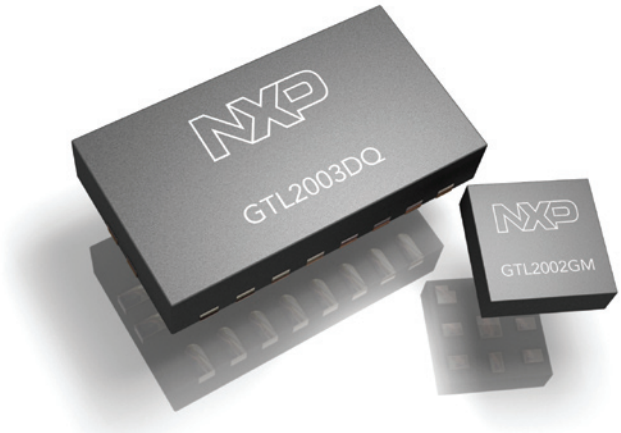


NXP bidirectional low-voltage translators GTL20xx

Low cost bidirectional voltage translation without directional control

Unlike level-shifting bus switches, which only translate between fixed voltages, these bidirectional low-voltage translators can translate any voltage between 1 and 5 V to any other voltage between 1 and 5 V. They also reduce ON-state resistance and minimize propagation delay.

Key features

- No directional control required for bidirectional voltage translations
- Low RON resistance (6.5 Ω) between input and output pins (Sn/Dn)
- Propagation delay: 1.5 ns (typ)
- Channel off-state capacitance: 7.5 pF
- Very low (5 µA) standby current
- No power supply required – prevents latch-ups
- Very small QFN package options

Applications

- Uni- and bidirectional translation for any voltage between 1 and 5 V
- Bidirectional translation of low-voltage and legacy I²C-bus signals
- Shifting processor sideband I/O signals between GTL and LVTTL/TTL levels

The NXP family of Gunning Transceiver Logic (GTL) bidirectional low-voltage translators includes the 22-bit GTL2000, the 2-bit GTL2002, the 8-bit GTL2003, and the 10-bit GTL2010.

Each delivers high-speed translation between different voltage levels with low ON-state resistance and minimal propagation delay.

They can translate any voltage between 1 and 5 V to any other voltage between 1 and 5 V as long as there is at least 1 V difference between the voltage levels, so they offer greater design flexibility than level-shifting bus switches, which only translate between fixed voltages.

Each GTL20xx device includes NMOS pass transistors (Sn and Dn pins) with a common gate (G_{REF} pin) and a reference transistor (S_{REF} and D_{REF} pins).

When one of the Sn or Dn ports is low, the clamp is in the ON-state and the Sn and Dn ports are linked through a low ON-resistance connection. Assuming the higher voltage is applied on the Dn port, when the Dn port is high, the voltage on the Sn port is limited to the voltage set by S_{REF}. When the Sn port is high, the Dn port is pulled to a higher voltage by a pull-up resistor.

This set-up enables seamless translation between user-selected voltages, without the need for directional control signals. All transistors have the same electrical characteristics so deviation from one output to another in voltage and propagation delay is kept to a minimum. The transistors also provide excellent ESD protection in case the low-voltage devices that are less resistant to ESD.

The translators can be used in any

NXP founded by Philips

application that requires uni- or bidirectional voltage translation for voltage levels between 1 and 5 V. The open-drain construction, which eliminates the need for directional control, makes the translators ideal for designs that combine low-voltage (1.0 to 1.8 V) and legacy (3.3 and/or 5.5 V) I²C-bus signals. The translators can change I²C-bus signal levels at speeds up to 3.4 MHz.

The translators can also be used in designs that combine GTL and LVTTL/TTL signals, shifting processor sideband I/O signals between voltage levels.

Bidirectional voltage translation

To configure the translators for bidirectional clamping, the G_{REF} input must be connected to D_{REF} and both pins must be pulled to the high-side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on D_{REF} is recommended.

The CPU output can be set as totem pole or open drain (pull-up resistors may be required), as can the chipset output (pull-up resistors are required to pull the Dn outputs to V_{CC}). No directional control is needed if both outputs are set as open drain. If either output is set to totem pole, however, there may be high-to-low contentions in either direction. To prevent this, set data as unidirectional or use 3-stateable outputs with a mechanism for direction control.

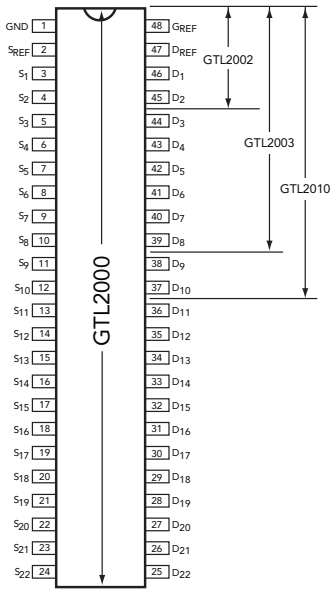
The opposite side of S_{REF} is connected to the CPU power-supply voltage. When D_{REF} is connected through a 200-kΩ resistor to V_{CC} and S_{REF} is set between 1.0 and V_{CC} minus 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF} and the output of each Dn has a maximum output voltage equal to the voltage of the pull-up resistor (3.3 and/or 5 V).

Unidirectional voltage translation

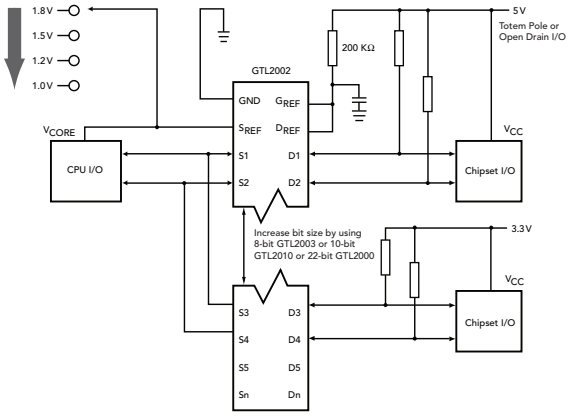
The same configuration can be used for one-way voltage translation, either up or down. For down-only translation, if the chipset I/O are open drain, pull-up resistors are required.

For up-only translation, a pull-up resistor is required on the high-side voltage (Dn). This is because the translator will only pass the reference source voltage (S_{REF}) as a high when doing up-translation. The driver on the low-side voltage only needs a pull-up resistor if it is set as open drain.

For more information on using the GTL20xx family, please refer to Application Note AN10145 at www.nxp.com/interface.



GTL20xx pinout diagram



Typical configuration for bidirectional voltage translation

Ordering information

Package	Container	GTL2000	GTL2002	GTL2003	GTL2010
SO	Tube	--	GTL2002D	--	--
	T&R	--	GTL2002D-T	--	--
SSOP	Tube	GTL2000DL	--	--	--
	T&R	GTL2000DL-T	--	--	--
TSSOP	Tube	GTL2000DGG	--	GTL2003PW	GTL2010PW
	T&R	GTL2000DGG-T	GTL2002DP-T	GTL2003PW-T	GTL2010PW-T
HVQFN	T&R	--	--	--	GTL2010BS-T
DHVQFN	T&R	--	--	GTL2003BQ-T	--
VSSOP	T&R	--	GTL2002DC-T	--	--
XQFN	T&R	--	GTL2002GM-T	--	--

Note: In Europe and Asia, for tube orders, add ", 112" (e.g. GTL2010PW, 112), and for tape and reel orders, replace "-T" with ", 118" (e.g. GTL2010PW, 118).

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