NXP AUP1Z04
Evaluation board

Easy test and evaluation of the 74AUP1Z04

This easy-to-use eval board lets you optimize for different system loads and evaluate the part under different test conditions.

Key features

- Wide supply voltage range: 0.8 V to 3.6 V
- High noise immunity
- Inputs accept voltages to 3.6 V
- No need for external biassing resistor
- Partial power-down mode
- Low noise overshoot and undershoot: < 10 % of V_{CC}
- Specified from 40 °C to +85 °C and 40 °C to +125 °C
- Very small footprint and availability in leadless MicroPak packages

Key benefits

- Reduced power consumption
- Fewer external components
- Stable operation over a wide range of conditions
- Increased flexibility in design and test

The AUP1Z04 demo board gives designers an easy way to test and evaluate the 74AUP1Z04, a low-power X-tal driver optimized for use in crystal oscillator applications. The 74AUP1Z04 combines the functions of the 74AUP1GU04 and the 74AUP1G04, thus delivering the benefits of a compact footprint, lower power dissipation, and stable operation over a wide range of frequency and temperature. The 74AUP1Z04 also integrates output enable circuitry and an internal bias resistor. The output enable circuitry saves power, while the internal bias resistor eliminates the need for an external resistor. It provides negative feedback and sets the mid-supply bias point for the inverter.

The board supports a supply voltage of 0.8 V to 3.6 V. When the $\overline{EN}$ input is not in use, it can be driven HIGH, pulling up the X1 input and putting the device in a low-power disable mode. Schmitt trigger action at the $\overline{EN}$ input lets the circuit tolerate slower input rise and fall times across the entire V_{CC} range.

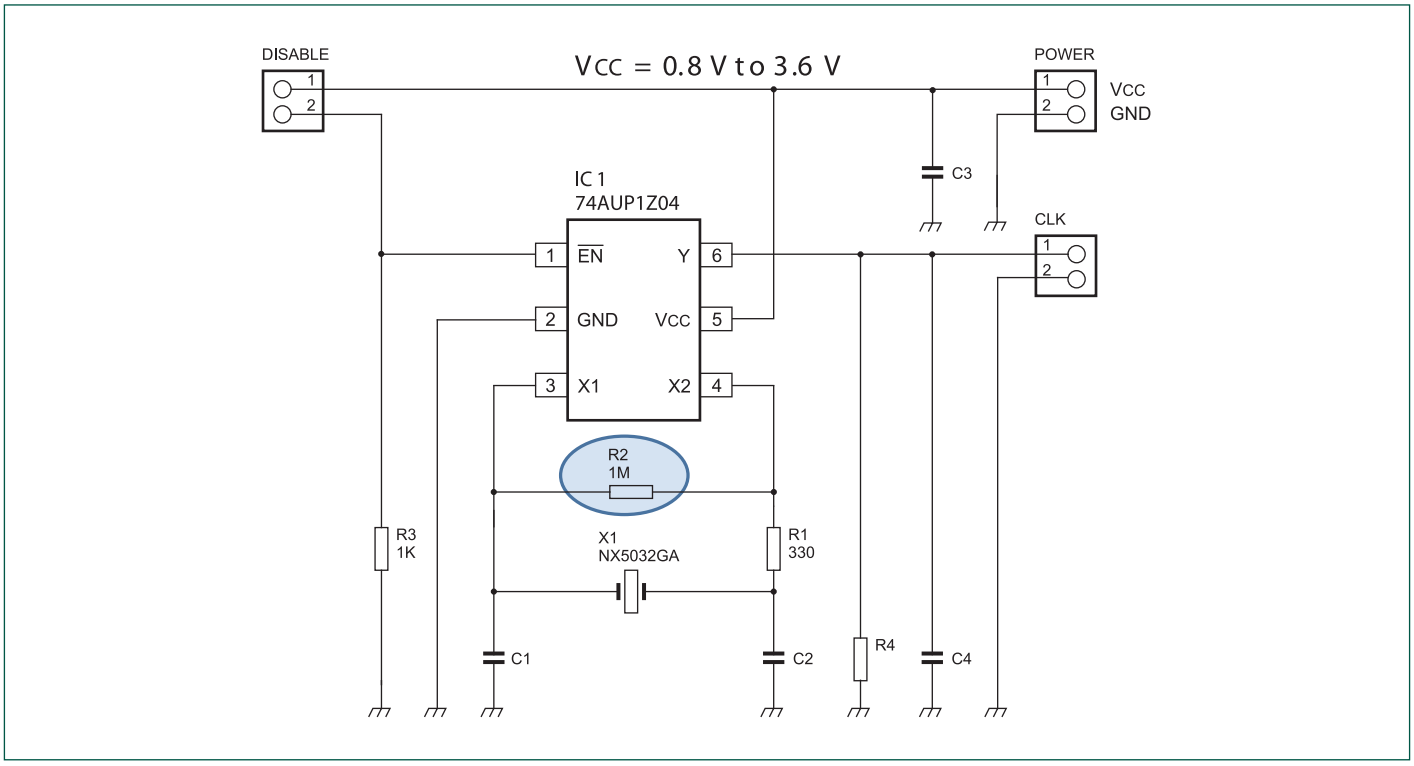
The 74AUP1Z04 is fully specified for partial power-down applications using I_{OFF} at output Y. The I_{OFF} circuitry disables the output Y, preventing backflow current from damaging the device when it is powered down.

The values of C1 and C2 are calculated so that a parallel combination of C1 and C2 is equal to the recommended load capacitance of the crystal (C_L), as specified in the crystal data sheet. A crystal with a range of frequencies can be used on the board without changing C1 and C2, as long as the load capacitance and footprint are the same. The reference board uses the NDK NX5032GA, a 25 MHz crystal with a load capacitance of 8 pF and a footprint of 5 mm x 3.2 mm. An alternate version of the NX5032GA, with the same footprint and capacitance but a range of 8 MHz to 25 MHz, is also available.

$$C_L = \frac{C1 \times C2}{(C1 + C2)}$$

To obtain a clean waveform, R1 isolates the output of the inverter from the crystal and prevents spurious high-frequency oscillation. The optimum value of R1 depends on the frequency of operation and the required stability. The minimum value of R1 depends on the recommended power consumption of the crystal. Crystal manufacturers usually specify a recommended R1 value in the data sheet. Using an R1 value lower than the one specified in the data sheet can cause overdriving of the crystal and could result in crystal damage or a shorter crystal life. Acceptable results can be achieved with an R1 value approximately equal to the capacitive reactance (R1 = X_{C2}), provided X_{C2} is greater than or equal to the manufacturer's recommended value.

C2 combines with R1 to form a low-pass filter. The value of C2 can be adjusted according to the desired cutoff frequency and start-up time. In a low-gain amplifier, C2 can be increased over C1 to increase the phase-shift and help in start-up, but C1 needs to be set such that the load capacitance introduced to the crystal does not exceed the manufacturer's recommended value of CL. The values of R4 and C4 can be adjusted to test how different loads effect the edge rates and the shape of the output clock. The $\overline{EN}$ pin is normally pulled down by R3, when the DISABLE jumper is open. When the DISABLE jumper is closed, the $\overline{EN}$ pin is pulled up to VCC and the clock output is turned off. The value of R3 can be increased or decreased to control the enable and disable times of the output clock. With a lower R3, the clock can be enabled or disabled faster.



NNP: Normally Not Populated. Schematic of AUP1Z04 demo board

Test results

Figure 1 shows the output of a 25 MHz crystal at a supply voltage of 3.3 V. Figure 2 shows the output at pin Y when the clock is enabled (that is, when the DISABLE jumper is open). Figure 3 shows the output waveform at a 1.8 V supply, when the clock is enabled. The load used for testing is R4 = 1 MΩ and C4 = 6 pF. The sinusoidal waveform of the crystal is converted into a square wave by using the buffered inverter channel of the AUP1Z04. Figure 4 shows the output when the clock is disabled (that is, when the DISABLE jumper is closed and the $\overline{EN}$ pin is pulled up to V_{cc}).

Figure 1

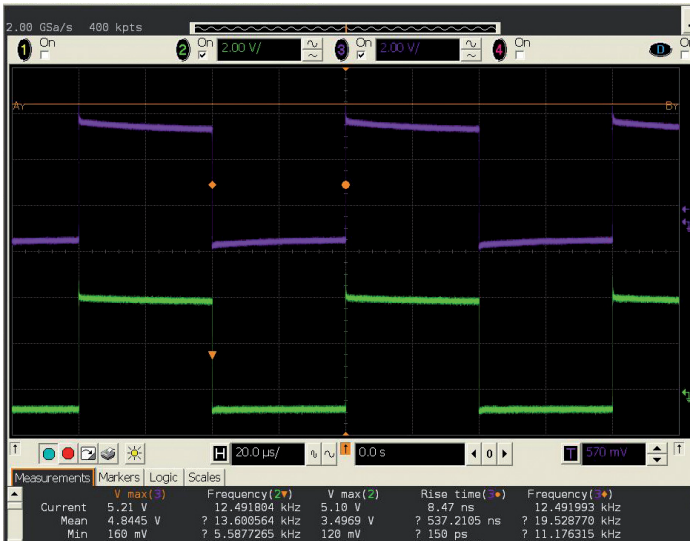


Figure 2

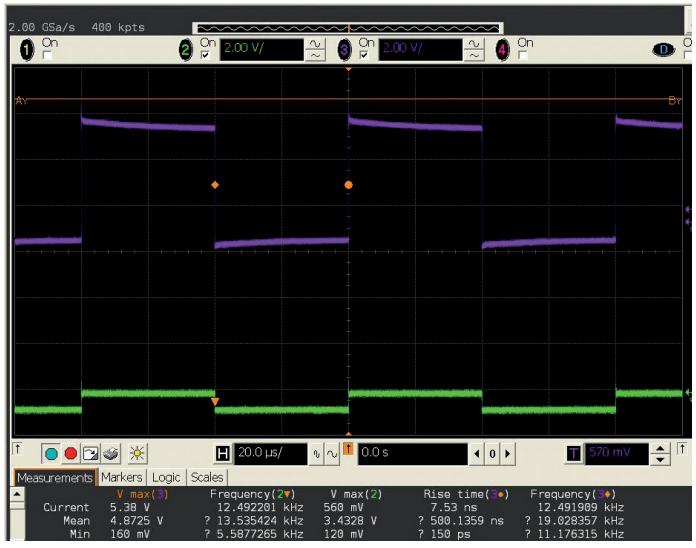


Figure 3

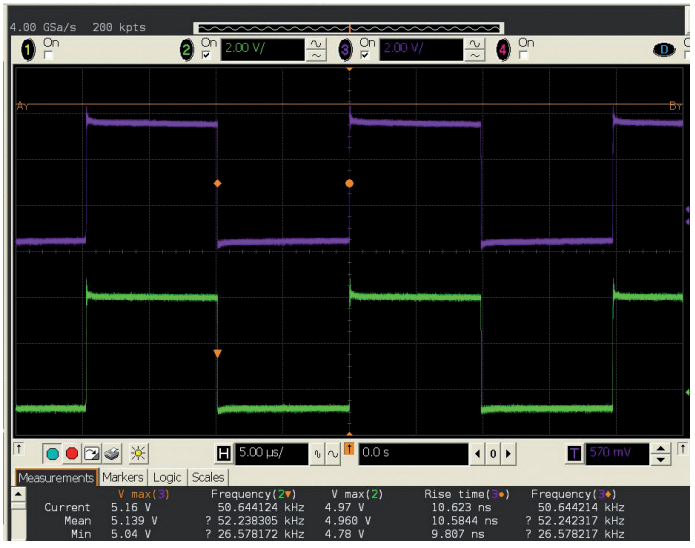
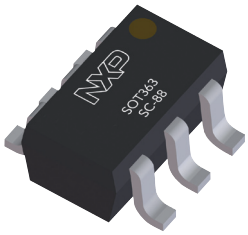
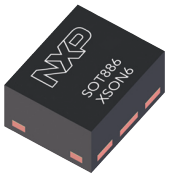


Figure 4

Packages

The 74AUP1Z04 is available in 6-pin SC88 and leadless XSON packages.

Package suffix	GW	GM	GF
			
	SOT363	SOT886	SOT891
	6-pin	6-pin	6-pin
Width (mm)	2.1	1	1
Length (mm)	2	1.45	1
Pitch (mm)	0,65	0.5	0.35

Ordering information

Part number	Package				
	Temp. range	Name	Type	Marking	Material
74AUP1Z04GW	-40 to 125 °C	SC-88	Surface mount	a4	Plastic
74AUP1Z04GM	-40 to 125 °C	XSON6	Thin small outline; no leads	a4	Plastic
74AUP1Z04GF	-40 to 125 °C	XSON6	Thin small outline; no leads	a4	Plastic

www.nxp.com

Date of release: June 2010
Document order number: 9397 750 16907
Printed in the Netherlands