

# 74ABT16240A

16-bit inverting buffer/line driver; 3-state

Rev. 6 — 3 November 2011

Product data sheet

## 1. General description

The 74ABT16240A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16240A is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs ( $\overline{1OE}$ ,  $\overline{2OE}$ ,  $\overline{3OE}$ ,  $\overline{4OE}$ ), each controlling four of the 3-state outputs.

## 2. Features and benefits

- 16-bit bus interface
- Multiple  $V_{CC}$  and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Output capability: +64 mA and -32 mA
- Live insertion and extraction permitted
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - ◆ HBM JESD-A114E exceeds 2000 V
  - ◆ CDM JESD22-C101-C exceeds 1000 V

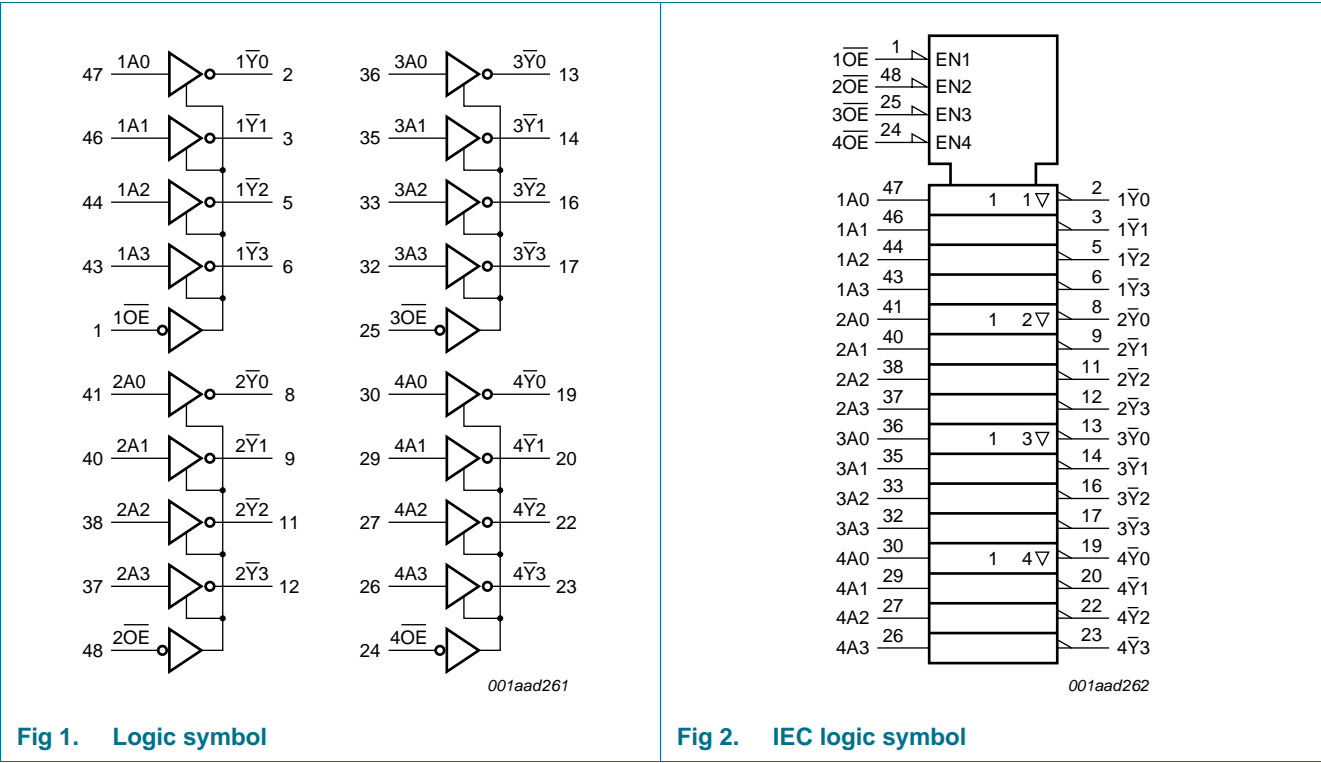
## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16240ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ABT16240ADL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1



4. Functional diagram



5. Pinning information

5.1 Pinning

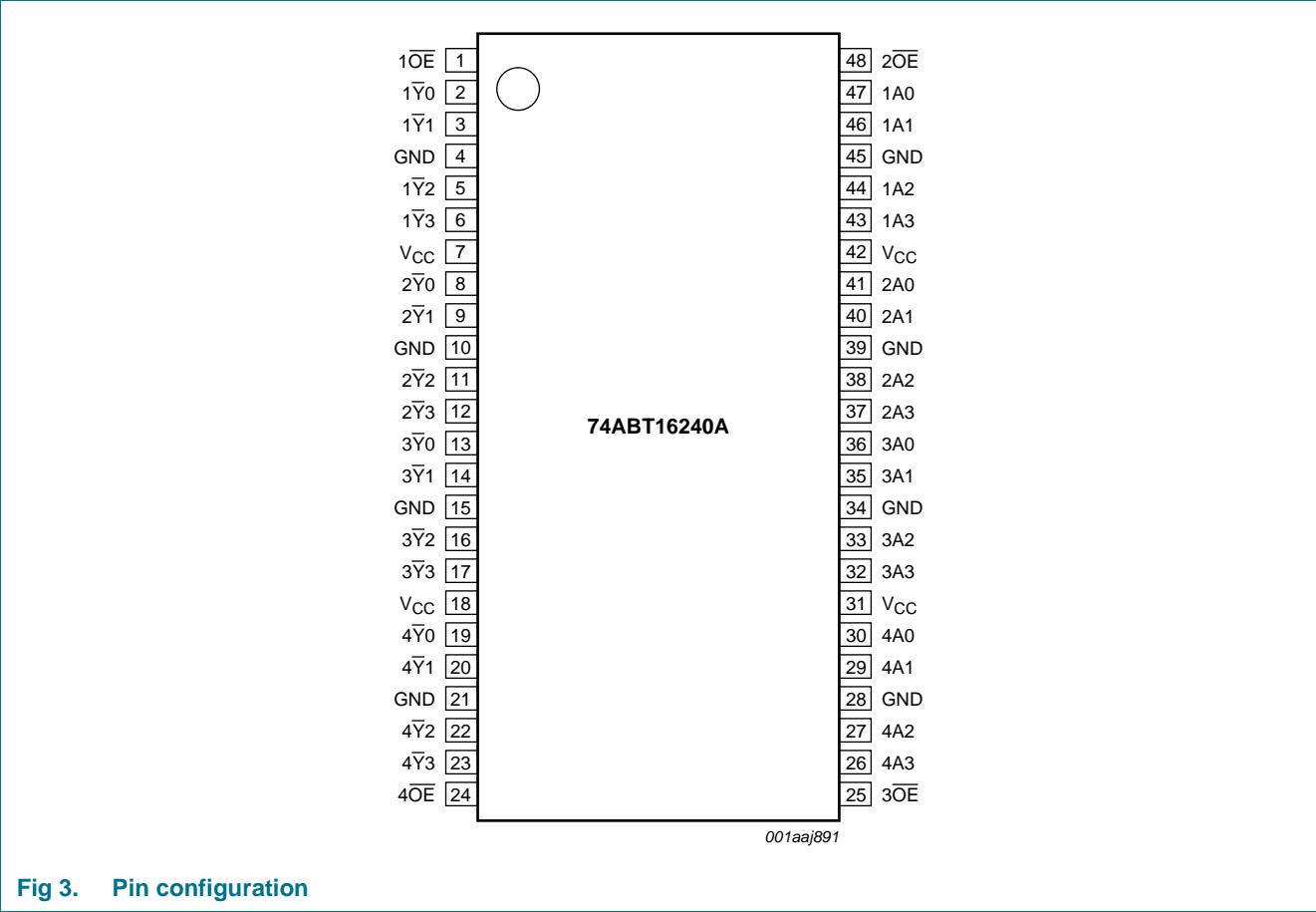


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1 $\overline{OE}$ , 2 $\overline{OE}$ , 3 $\overline{OE}$ , 4 $\overline{OE}$	1, 48, 25, 24	output enable (LOW active)
1 $\overline{Y0}$ , 1 $\overline{Y1}$ , 1 $\overline{Y2}$ , 1 $\overline{Y3}$	2, 3, 5, 6	1 data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
2 $\overline{Y0}$ , 2 $\overline{Y1}$ , 2 $\overline{Y2}$ , 2 $\overline{Y3}$	8, 9, 11, 12	2 data output
3 $\overline{Y0}$ , 3 $\overline{Y1}$ , 3 $\overline{Y2}$ , 3 $\overline{Y3}$	13, 14, 16, 17	3 data output
4 $\overline{Y0}$ , 4 $\overline{Y1}$ , 4 $\overline{Y2}$ , 4 $\overline{Y3}$	19, 20, 22, 23	4 data output
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	4 data input
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	3 data input
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	2 data input
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	1 data input

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

Control	Input	Output
$\overline{\text{nOE}}$	nAn	$\overline{\text{nYn}}$
L	L	H
L	H	L
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4.** Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		<sup>[1]</sup> -1.2	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	<sup>[1]</sup> -0.5	+5.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-18	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
$T_j$	junction temperature		<sup>[2]</sup> -	150	°C
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5.** Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$I_{OH}$	HIGH-level output current		-32	-	-	mA
$I_{OL}$	LOW-level output current		-	-	32	mA
		duty cycle $\leq 50$ %; $f_i \geq 1$ kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	-	10	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	-1.2	-	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IL}$ or $V_{IH}$						
		$V_{CC} = 4.5\text{ V}$ ; $I_{OH} = -3\text{ mA}$	2.5	2.9	-	2.5	-	V
		$V_{CC} = 5.0\text{ V}$ ; $I_{OH} = -3\text{ mA}$	3.0	3.4	-	3.0	-	V
		$V_{CC} = 4.5\text{ V}$ ; $I_{OH} = -32\text{ mA}$	2.0	2.4	-	2.0	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 4.5\text{ V}$ ; $I_{OL} = 64\text{ mA}$ ; $V_I = V_{IL}$ or $V_{IH}$	-	0.42	0.55	-	0.55	V
$I_I$	input leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{CC}$ or GND	-	$\pm 0.01$	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O \leq 4.5\text{ V}$	-	$\pm 5.0$	$\pm 100$	-	$\pm 100$	$\mu\text{A}$
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} = 2.0\text{ V}$ ; $V_O = 0.5\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $\overline{nOE} = \text{HIGH}$	[1]	$\pm 5.0$	$\pm 50$	-	$\pm 50$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$						
		output HIGH-state at $V_O = 5.5\text{ V}$	-	1.0	10	-	10	$\mu\text{A}$
		output LOW-state at $V_O = 0.5\text{ V}$	-	-1.0	-10	-	-10	$\mu\text{A}$
$I_{LO}$	output leakage current	HIGH-state; $V_O = 5.5\text{ V}$ ; $V_{CC} = 5.5\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$	-	1.0	50	-	50	$\mu\text{A}$
$I_O$	output current	$V_{CC} = 5.5\text{ V}$ ; $V_O = 2.5\text{ V}$	[2]	-180	-70	-50	-180	mA
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$						
		outputs HIGH-state	-	0.5	1.0	-	1.0	mA
		outputs LOW-state	-	8	19	-	19	mA
		outputs 3-state	-	0.5	1.0	-	1.0	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 5.5\text{ V}$ ; one input at 3.4 V and other inputs at $V_{CC}$ or GND	[3][4]	10	200	-	200	$\mu\text{A}$
$C_I$	input capacitance	$V_I = 0\text{ V}$ or $V_{CC}$	-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; $V_O = 0\text{ V}$ or $V_{CC}$	-	6	-	-	-	pF

[1] This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V, with a transition time of up to 10 ms. From  $V_{CC} = 2.1\text{ V}$  to  $V_{CC} = 5\text{ V} \pm 10\%$ , a transition time of up to 100  $\mu\text{s}$  is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

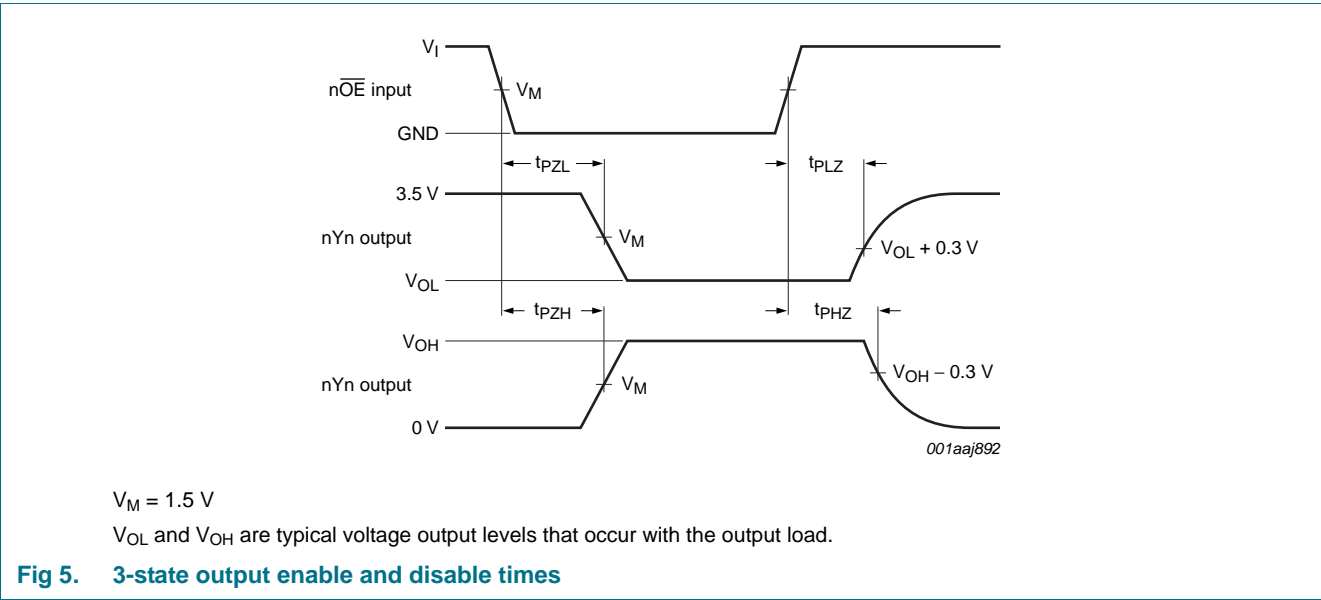
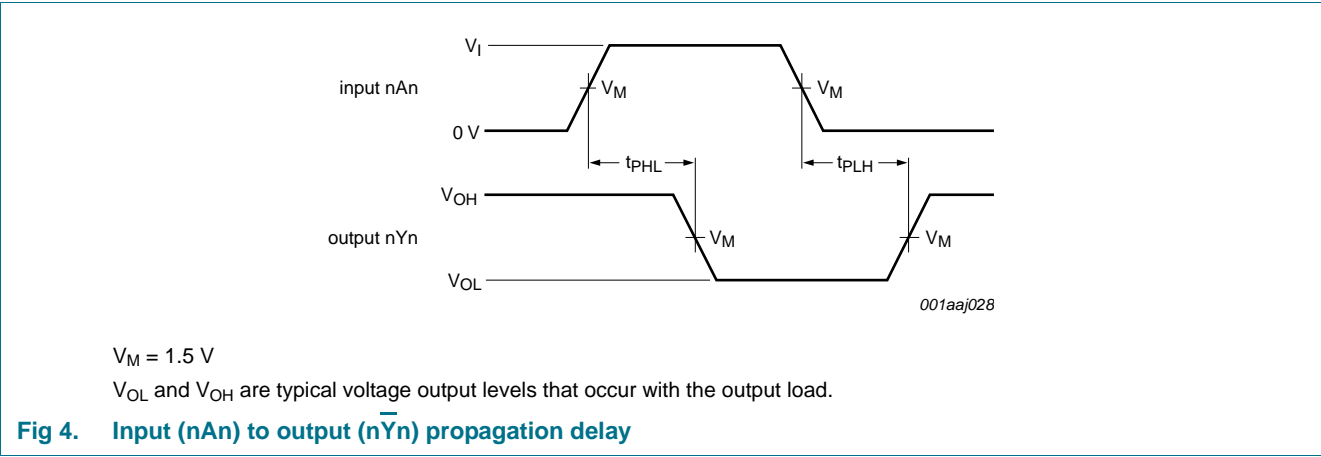
[4] This data sheet limit may vary among suppliers.

## 10. Dynamic characteristics

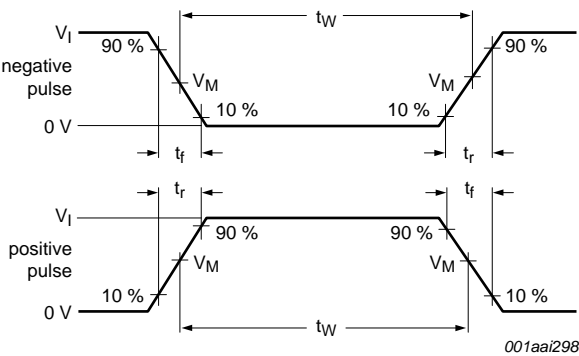
**Table 7. Dynamic characteristics**  
*GND = 0 V. For test circuit, see [Figure 6](#).*

Symbol	Parameter	Conditions	25 °C; V <sub>CC</sub> = 5.0 V			–40 °C to +85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to n $\bar{Y}$ n; see <a href="#">Figure 4</a>	1.0	2.0	3.0	1.0	3.7	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to n $\bar{Y}$ n; see <a href="#">Figure 4</a>	1.0	1.5	3.0	1.0	3.5	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	n $\bar{O}\bar{E}$ to n $\bar{Y}$ n; see <a href="#">Figure 5</a>	1.2	2.4	3.3	1.2	4.2	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	n $\bar{O}\bar{E}$ to n $\bar{Y}$ n; see <a href="#">Figure 5</a>	1.2	2.3	3.2	1.0	4.2	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\bar{O}\bar{E}$ to n $\bar{Y}$ n; see <a href="#">Figure 5</a>	1.3	2.7	4.1	1.6	4.7	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\bar{O}\bar{E}$ to n $\bar{Y}$ n; see <a href="#">Figure 5</a>	1.3	2.5	3.6	1.4	4.1	ns

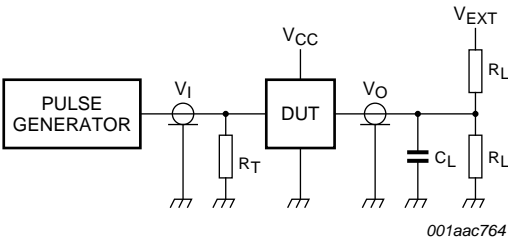
11. Waveforms



12. Test information



$V_M = 1.5\text{ V}$   
a. Input pulse definition



Test data is given in [Table 8](#).  
Definitions test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

b. Test circuit for 3-state outputs

Fig 6. Load circuitry for switching times

Table 8. Test data

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 $\Omega$	open	7.0 V	open



13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

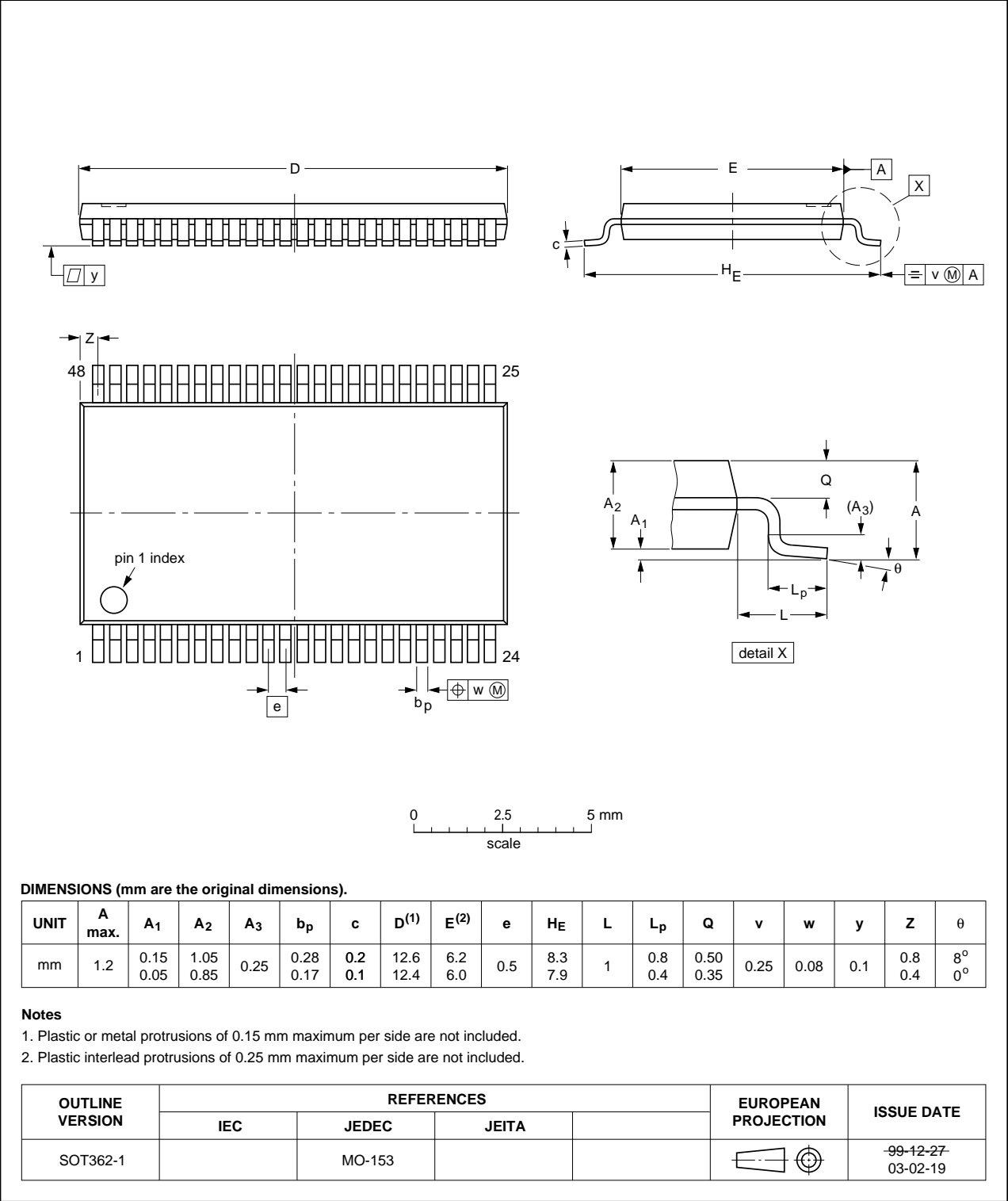


Fig 7. Package outline SOT362-1 (TSSOP48)

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

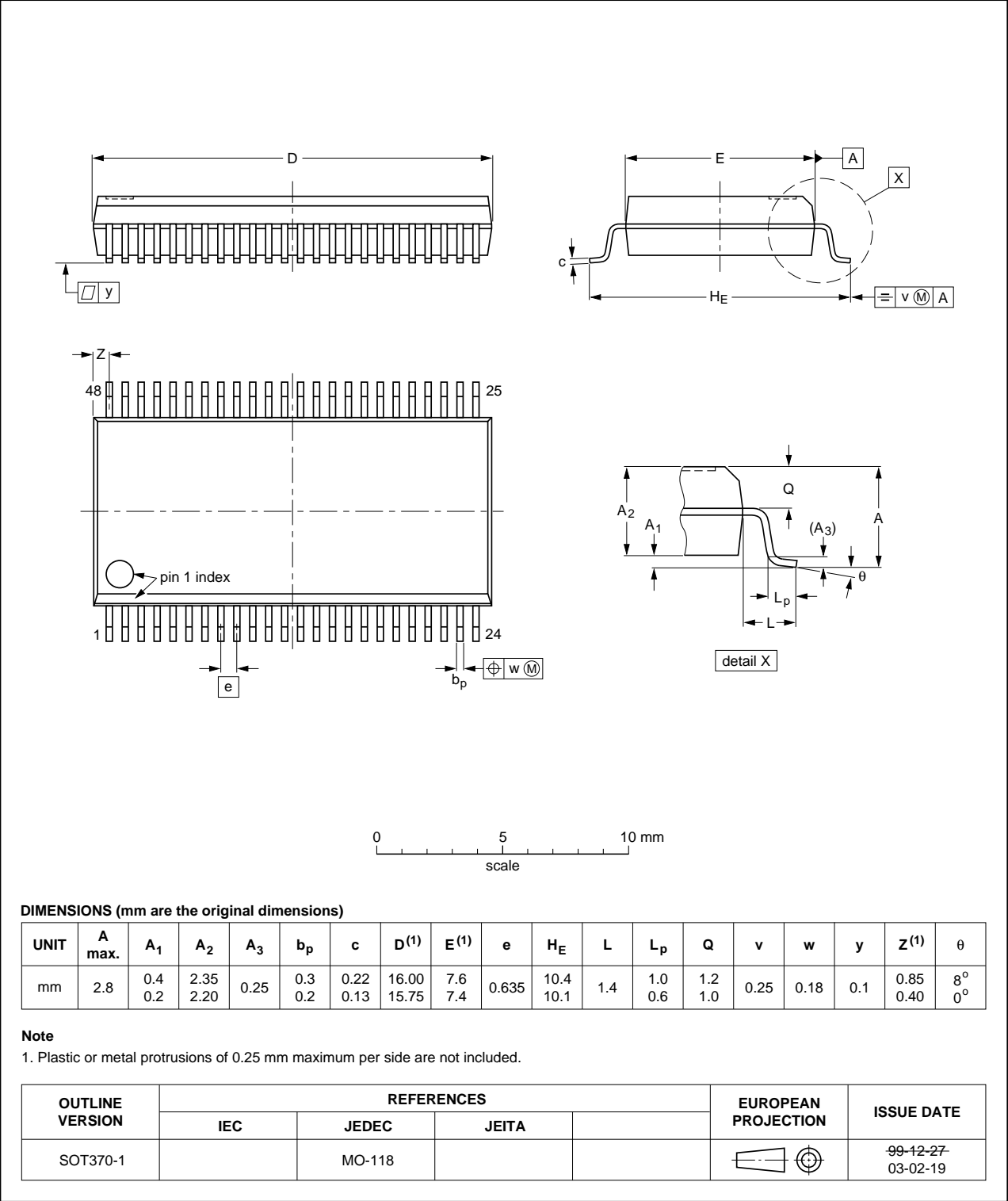


Fig 8. Package outline SOT370-1 (SSOP48)

## 14. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar CMOS
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
CDM	Charged Device Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16240A v.6	20111103	Product data sheet	-	74ABT16240A v.5
Modifications:	• Legal pages updated			
74ABT16240A v.5	20100525	Product data sheet	-	74ABT16240A v.4
74ABT16240A v.4	20090325	Product data sheet	-	74ABT16240A v.3
74ABT16240A v.3	20040212	Product specification	01-A15420	74ABT_H16240A v.2
74ABT_H16240A v.2	19980225	Product specification	853-1880 19019	74ABT_H16240A
74ABT_H16240A	19961001	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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