

# 74ABT646A

Octal bus transceiver/register; 3-state

Rev. 03 — 15 March 2010

Product data sheet

## 1. General description

The 74ABT646A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT646A transceiver/register consists of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A bus or B bus will be clocked into the registers as the appropriate clock pin (CPAB or CPBA) goes HIGH. Output Enable ( $\overline{OE}$ ) and Direction (DIR) pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or B register or both.

The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real-time. The DIR pin determines which bus receives data when  $\overline{OE}$  is active (LOW). In isolation mode ( $\overline{OE}$  = HIGH), data from bus A may be stored in the B register and/or data from bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. The examples in [Figure 5](#) “Real time bus transfer and storage” on page 6 demonstrate the four fundamental bus management functions that can be performed with the 74ABT646A.

## 2. Features and benefits

- Combines 74ABT245 and 74ABT373A type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Live insertion and extraction permitted
- Output capability: +64 mA to –32 mA
- Power-up 3-state
- Power-up reset
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

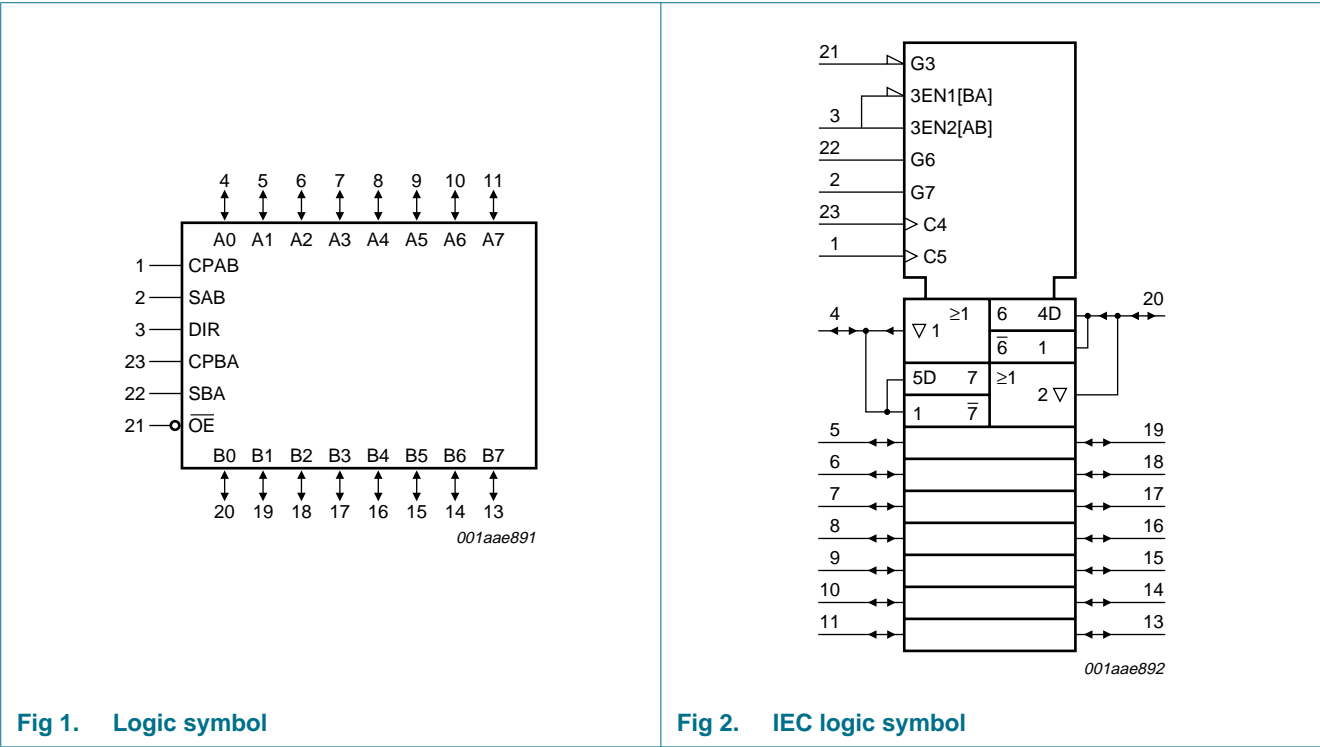


3. Ordering information

Table 1. Ordering information

| Type number | Package           |         |  | Version  |
|-------------|-------------------|---------|--|----------|
|             | Temperature range | Name    | Description  |          |
| 74ABT646AD  | −40 °C to +85 °C  | SO24    | plastic small outline package; 24 leads; body width 7.5 mm             | SOT137-1 |
| 74ABT646ADB | −40 °C to +85 °C  | SSOP24  | plastic shrink small outline package; 24 leads; body width 5.3 mm      | SOT340-1 |
| 74ABT646APW | −40 °C to +85 °C  | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |

4. Functional diagram



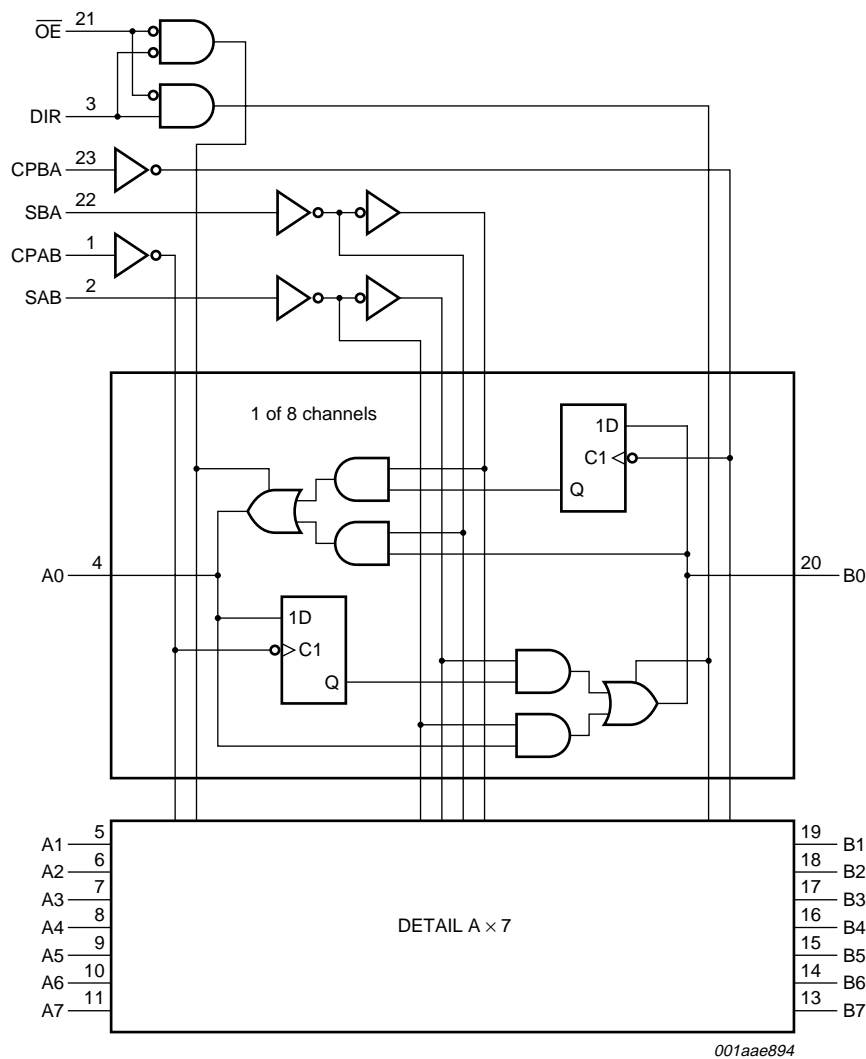
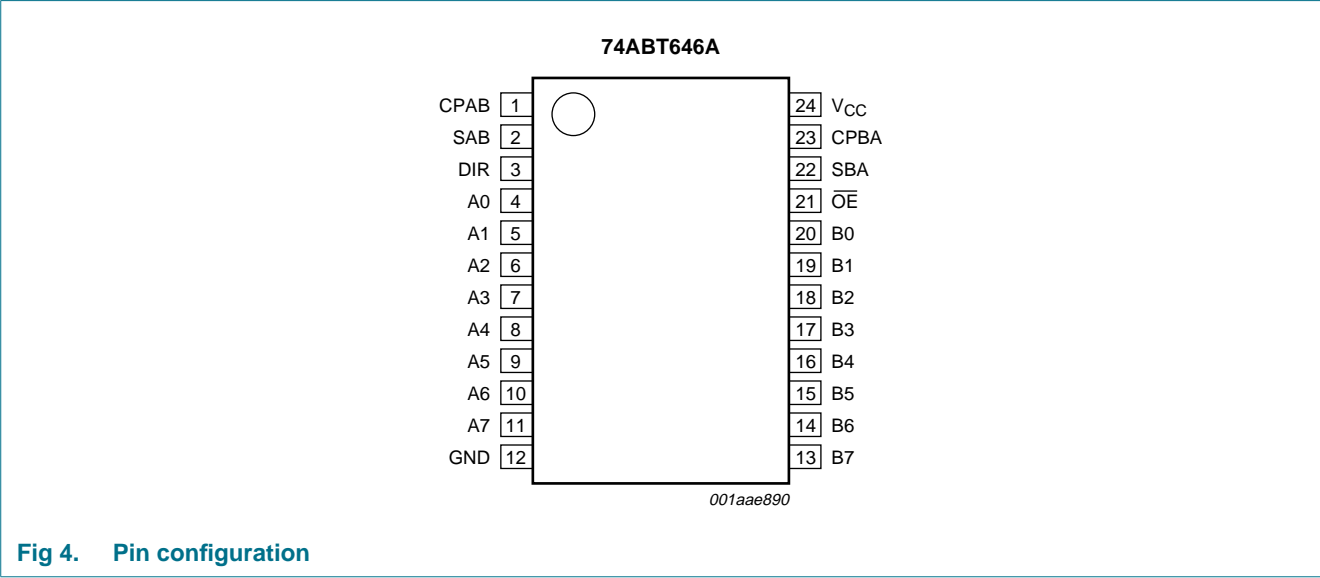


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol                         | Pin                            | Description                      |
|--------------------------------|--------------------------------|----------------------------------|
| CPAB                           | 1                              | A to B clock input               |
| SAB                            | 2                              | A to B select input              |
| DIR                            | 3                              | direction control input          |
| A0, A1, A2, A3, A4, A5, A6, A7 | 4, 5, 6, 7, 8, 9, 10, 11       | data input/output (A side)       |
| GND                            | 12                             | ground (0 V)                     |
| B0, B1, B2, B3, B4, B5, B6, B7 | 20, 19, 18, 17, 16, 15, 14, 13 | data input/output (B side)       |
| OE                             | 21                             | output enable input (active LOW) |
| SBA                            | 22                             | B to A select input              |
| CPBA                           | 23                             | B to A clock input               |
| V <sub>CC</sub>                | 24                             | positive supply voltage          |

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

| Inputs          |     |        |        |     |     | Data I/O                          |                                   | Operating mode            |
|-----------------|-----|--------|--------|-----|-----|-----------------------------------|-----------------------------------|---------------------------|
| $\overline{OE}$ | DIR | CPAB   | CPBA   | SAB | SBA | An                                | Bn                                |                           |
| X               | X   | ↑      | X      | X   | X   | input                             | unspecified output <sup>[2]</sup> | store A, B unspecified    |
| X               | X   | X      | ↑      | X   | X   | unspecified output <sup>[2]</sup> | input                             | store B, A unspecified    |
| H               | X   | ↑      | ↑      | X   | X   | input                             | input                             | store A and B data        |
| H               | X   | H or L | H or L | X   | X   | input                             | input                             | isolation, hold storage   |
| L               | L   | X      | X      | X   | L   | output                            | input                             | real time B data to A bus |
| L               | L   | X      | H or L | X   | H   | output                            | input                             | stored B data to A bus    |
| L               | H   | X      | X      | L   | X   | input                             | output                            | real time A data to B bus |
| L               | H   | H or L | X      | H   | X   | input                             | output                            | stored A data to B bus    |

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 ↑ = LOW-to-HIGH clock transition;

- [2] The data output function may be enabled or disabled by various signals at the  $\overline{OE}$  input. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

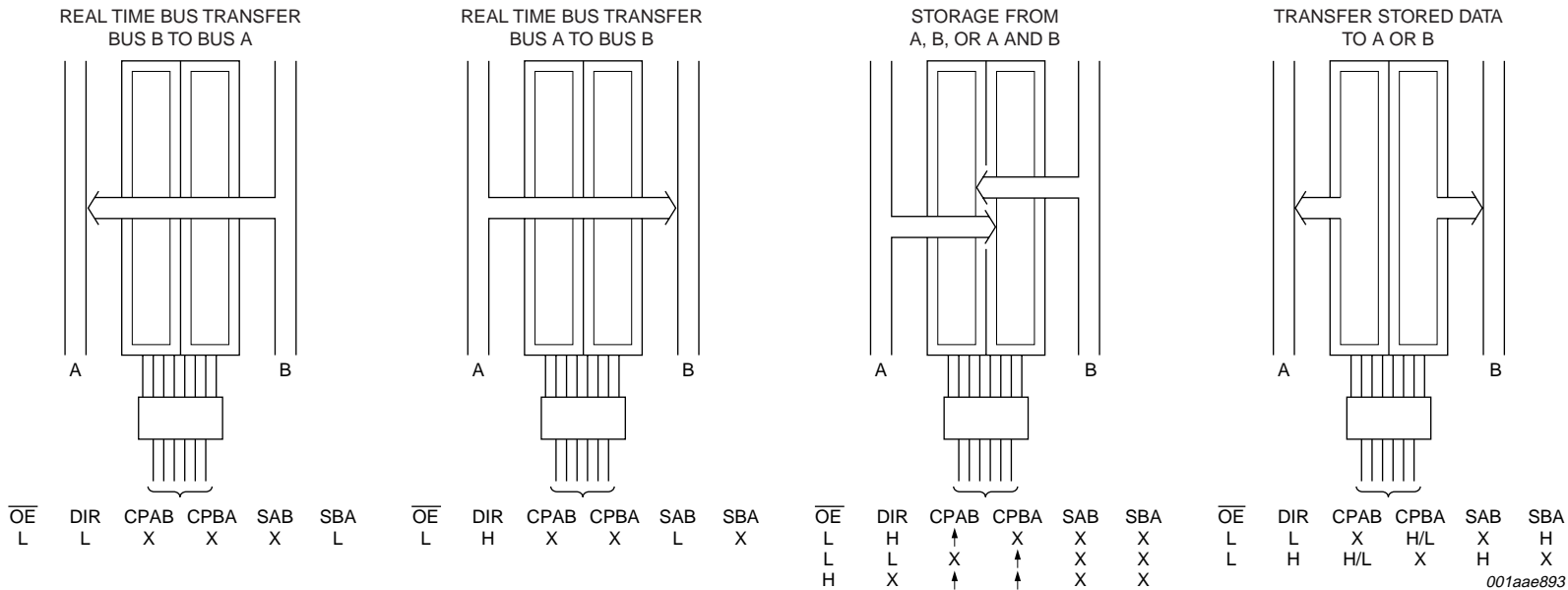


Fig 5. Real time bus transfer and storage

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol    | Parameter               | Conditions                        | Min      | Max  | Unit |
|-----------|-------------------------|-----------------------------------|----------|------|------|
| $V_{CC}$  | supply voltage          |                                   | -0.5     | +7.0 | V    |
| $V_I$     | input voltage           |                                   | [1] -1.2 | +7.0 | V    |
| $V_O$     | output voltage          | output in OFF-state or HIGH-state | [1] -0.5 | +5.5 | V    |
| $I_{IK}$  | input clamping current  | $V_I < 0$ V                       | -18      | -    | mA   |
| $I_{OK}$  | output clamping current | $V_O < 0$ V                       | -50      | -    | mA   |
| $I_O$     | output current          | output in LOW-state               | -        | 128  | mA   |
| $T_j$     | junction temperature    |                                   | [2] -    | 150  | °C   |
| $T_{stg}$ | storage temperature     |                                   | -65      | +150 | °C   |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol              | Parameter                           | Conditions  | Min | Typ | Max      | Unit |
|---------------------|-------------------------------------|-------------|-----|-----|----------|------|
| $V_{CC}$            | supply voltage                      |             | 4.5 | -   | 5.5      | V    |
| $V_I$               | input voltage                       |             | 0   | -   | $V_{CC}$ | V    |
| $V_{IH}$            | HIGH-level input voltage            |             | 2.0 | -   | -        | V    |
| $V_{IL}$            | LOW-level input voltage             |             | -   | -   | 0.8      | V    |
| $I_{OH}$            | HIGH-level output current           |             | -32 | -   | -        | mA   |
| $I_{OL}$            | LOW-level output current            |             | -   | -   | 64       | mA   |
| $\Delta t/\Delta V$ | input transition rise and fall rate |             | 0   | -   | 10       | ns/V |
| $T_{amb}$           | ambient temperature                 | in free air | -40 | -   | +85      | °C   |

## 9. Static characteristics

Table 6. Static characteristics

| Symbol                | Parameter                          | Conditions  | 25 °C  |           |      | –40 °C to 85 °C |      | Unit |    |
|-----------------------|------------------------------------|---|--------|-----------|------|-----------------|------|------|----|
|                       |                                    |   | Min    | Typ       | Max  | Min             | Max  |      |    |
| V <sub>IK</sub>       | input clamping voltage             | V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = –18 mA   | –1.2   | –0.9      | -    | –1.2            | -    | V    |    |
| V <sub>OH</sub>       | HIGH-level output voltage          | V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>   |        |           |      |                 |      |      |    |
|                       |                                    | V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = –3 mA  | 2.5    | 3.0       | -    | 2.5             | -    | V    |    |
|                       |                                    | V <sub>CC</sub> = 5.0 V; I <sub>OH</sub> = –3 mA  | 3.0    | 3.5       | -    | 3.0             | -    | V    |    |
|                       |                                    | V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = –32 mA   | 2.0    | 2.4       | -    | 2.0             | -    | V    |    |
| V <sub>OL</sub>       | LOW-level output voltage           | V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 64 mA;<br>V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>                            | -      | 0.3       | 0.55 | -               | 0.55 | V    |    |
| V <sub>OL(pu)</sub>   | power-up LOW-level output voltage  | V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 1 mA;<br>V <sub>I</sub> = GND or V <sub>CC</sub>  | [1]    | -         | 0.13 | 0.55            | -    | 0.55 | V  |
| I <sub>I</sub>        | input leakage current              | V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V  |        |           |      |                 |      |      |    |
|                       |                                    | control pins  | -      | ±0.0<br>1 | ±1.0 | -               | ±1.0 | μA   |    |
|                       |                                    | data pins   | -      | ±5        | ±100 | -               | ±100 | μA   |    |
| I <sub>OFF</sub>      | power-off leakage current          | V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V   | -      | ±5.0      | ±100 | -               | ±100 | μA   |    |
| I <sub>O(pu/pd)</sub> | power-up/power-down output current | V <sub>CC</sub> = 2.1 V; V <sub>O</sub> = 0.5 V;<br>V <sub>I</sub> = GND or V <sub>CC</sub> ; OE HIGH                               | [2]    | -         | ±5.0 | ±50             | -    | ±50  | μA |
| I <sub>OZ</sub>       | OFF-state output current           | V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>  |        |           |      |                 |      |      |    |
|                       |                                    | V <sub>O</sub> = 2.7 V  | -      | 5.0       | 50   | -               | 50   | μA   |    |
|                       |                                    | V <sub>O</sub> = 0.5 V  | -      | –5.0      | –50  | -               | –50  | μA   |    |
| I <sub>LO</sub>       | output leakage current             | V <sub>CC</sub> = 5.5 V; HIGH-state;<br>V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 5.5 V;<br>V <sub>I</sub> = GND or V <sub>CC</sub> | -      | 5.0       | 50   | -               | 50   | μA   |    |
| I <sub>O</sub>        | output current                     | V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V   | [3][5] | –180      | –65  | –40             | –180 | –40  | mA |
| I <sub>CC</sub>       | supply current                     | V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>  |        |           |      |                 |      |      |    |
|                       |                                    | outputs HIGH-state  | -      | 110       | 250  | -               | 250  | μA   |    |
|                       |                                    | outputs LOW-state   | -      | 20        | 30   | -               | 30   | mA   |    |
|                       |                                    | outputs disabled  | -      | 110       | 250  | -               | 250  | μA   |    |
| ΔI <sub>CC</sub>      | additional supply current          | per input pin; V <sub>CC</sub> = 5.5 V; one input at 3.4 V; other inputs at V <sub>CC</sub> or GND                                  | [4]    | -         | 0.6  | 1.5             | -    | 1.5  | mA |
| C <sub>I</sub>        | input capacitance                  | control pins; V <sub>I</sub> = 0 V or V <sub>CC</sub>   | -      | 4         | -    | -               | -    | pF   |    |
| C <sub>I/O</sub>      | input/output capacitance           | I/O pins; outputs disabled; V <sub>O</sub> = 0 V or V <sub>CC</sub>   | -      | 7         | -    | -               | -    | pF   |    |

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any  $V_{CC}$  between 0 V and 2.1 V with a transition time of up to 10 ms. For  $V_{CC} = 2.1\text{ V}$  to  $V_{CC} = 5\text{ V} \pm 10\%$ , a transition time of up to 100  $\mu\text{s}$  is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

[5] This data sheet limit may vary among suppliers.



## 10. Dynamic characteristics

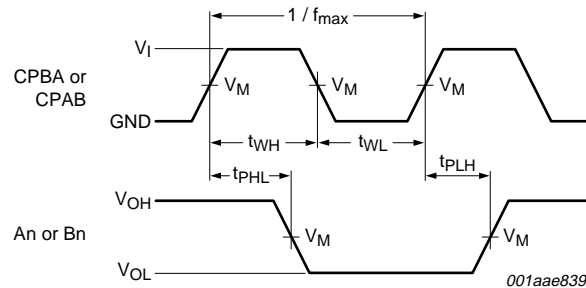
**Table 7. Dynamic characteristics**

$GND = 0\text{ V}$ ; for test circuit, see [Figure 11](#).

| Symbol      | Parameter                           | Conditions  | 25 °C; $V_{CC} = 5.0\text{ V}$ |      |                    | –40 °C to +85 °C;<br>$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ |                    | Unit |
|-------------|-------------------------------------|---|--------------------------------|------|--------------------|---|--------------------|------|
|             |                                     |   | Min                            | Typ  | Max                | Min   | Max                |      |
| $f_{\max}$  | maximum frequency                   | see <a href="#">Figure 6</a>                              | 125                            | 350  | -                  | 125   | -                  | MHz  |
| $t_{PLH}$   | LOW to HIGH propagation delay       | CPAB to Bn or CPBA to An; see <a href="#">Figure 6</a>    | 2.2                            | 3.9  | 5.1                | 2.2   | 5.6                | ns   |
|             |                                     | An to Bn or Bn to An; see <a href="#">Figure 7</a>        | 1.5                            | 3.2  | 4.3                | 1.5   | 4.8                | ns   |
|             |                                     | SAB to Bn or SBA to An; see <a href="#">Figure 7</a>      | 1.5                            | 3.8  | 5.1                | 1.5   | 6.5                | ns   |
| $t_{PHL}$   | HIGH to LOW propagation delay       | CPAB to Bn or CPBA to An; see <a href="#">Figure 6</a>    | 1.7                            | 4.4  | 5.2 <sup>[1]</sup> | 1.7   | 5.6                | ns   |
|             |                                     | An to Bn or Bn to An; see <a href="#">Figure 7</a>        | 1.5                            | 3.7  | 4.6                | 1.5   | 5.4                | ns   |
|             |                                     | SAB to Bn or SBA to An; see <a href="#">Figure 7</a>      | 1.5                            | 4.4  | 5.3 <sup>[1]</sup> | 1.5   | 5.9                | ns   |
| $t_{PZH}$   | OFF-state to HIGH propagation delay | $\overline{OE}$ to An or Bn; see <a href="#">Figure 8</a> | 1.5                            | 3.5  | 5.3                | 1.5   | 6.3                | ns   |
|             |                                     | DIR to An or Bn; see <a href="#">Figure 8</a>             | 1.5                            | 3.9  | 5.7                | 1.2   | 6.7                | ns   |
| $t_{PZL}$   | OFF-state to LOW propagation delay  | $\overline{OE}$ to An or Bn; see <a href="#">Figure 9</a> | 3.0                            | 4.5  | 7.4                | 3.0   | 8.8                | ns   |
|             |                                     | DIR to An or Bn; see <a href="#">Figure 9</a>             | 2.5                            | 4.7  | 9.0                | 2.5   | 9.5                | ns   |
| $t_{PHZ}$   | HIGH to OFF-state propagation delay | $\overline{OE}$ to An or Bn; see <a href="#">Figure 8</a> | 1.5                            | 4.0  | 4.8 <sup>[1]</sup> | 1.5   | 5.3 <sup>[1]</sup> | ns   |
|             |                                     | DIR to An or Bn; see <a href="#">Figure 8</a>             | 1.5                            | 4.0  | 5.0                | 1.5   | 5.7                | ns   |
| $t_{PLZ}$   | LOW to OFF-state propagation delay  | $\overline{OE}$ to An or Bn; see <a href="#">Figure 9</a> | 1.5                            | 3.3  | 4.0                | 1.5   | 4.5                | ns   |
|             |                                     | DIR to An or Bn; see <a href="#">Figure 9</a>             | 1.5                            | 3.5  | 4.7                | 1.5   | 6.0                | ns   |
| $t_{su(H)}$ | set-up time HIGH                    | An to CPAB, Bn to CPBA; see <a href="#">Figure 10</a>     | 3.0                            | 0.7  | -                  | 3.0   | -                  | ns   |
| $t_{su(L)}$ | set-up time LOW                     | An to CPAB, Bn to CPBA; see <a href="#">Figure 10</a>     | 3.0                            | 0.7  | -                  | 3.0   | -                  | ns   |
| $t_{h(H)}$  | hold time HIGH                      | An to CPAB, Bn to CPBA; see <a href="#">Figure 10</a>     | +0.0                           | –0.5 | -                  | 0.0   | -                  | ns   |
| $t_{h(L)}$  | hold time LOW                       | An to CPAB, Bn to CPBA; see <a href="#">Figure 10</a>     | +0.0                           | –0.5 | -                  | 0.0   | -                  | ns   |
| $t_{WH}$    | pulse width HIGH                    | CPAB, CPBA; see <a href="#">Figure 6</a>                  | 4.0                            | 0.9  | -                  | 4.0   | -                  | ns   |
| $t_{WL}$    | pulse width LOW                     | LE; see <a href="#">Figure 6</a>                          | 4.0                            | 1.4  | -                  | 4.0   | -                  | ns   |

[1] This data sheet limit may vary among suppliers.

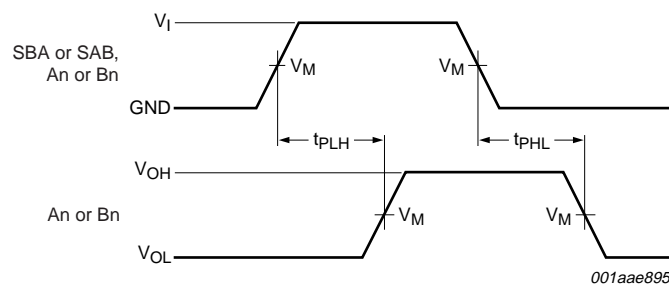
## 11. Waveforms



$V_M = 1.5 \text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

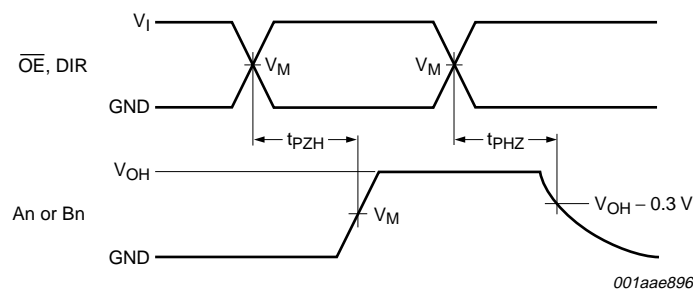
**Fig 6. Propagation delay clock input to output and clock pulse width, maximum clock frequency**



$V_M = 1.5 \text{ V}$

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

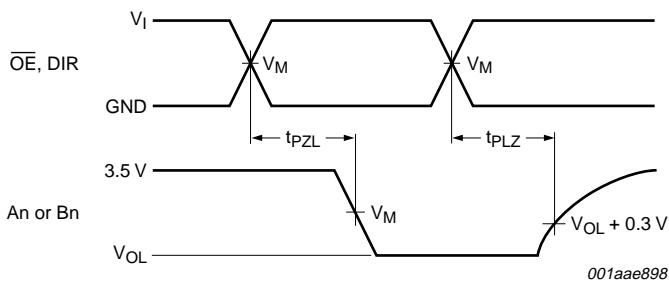
**Fig 7. Propagation delay, SAB to Bn or SBA to An, An to Bn or Bn to An**



$V_M = 1.5 \text{ V}$

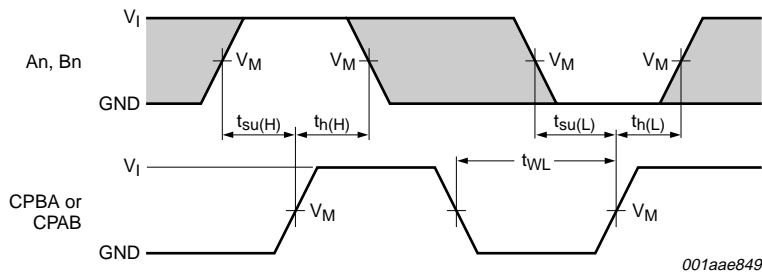
$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. 3-state output enable time to HIGH-level and output disable time from HIGH-level**



$V_M = 1.5 \text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig 9. 3-state output enable time to LOW-level and output disable time from LOW-level



$V_M = 1.5 \text{ V}$   
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.  
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 10. Data set-up and hold times

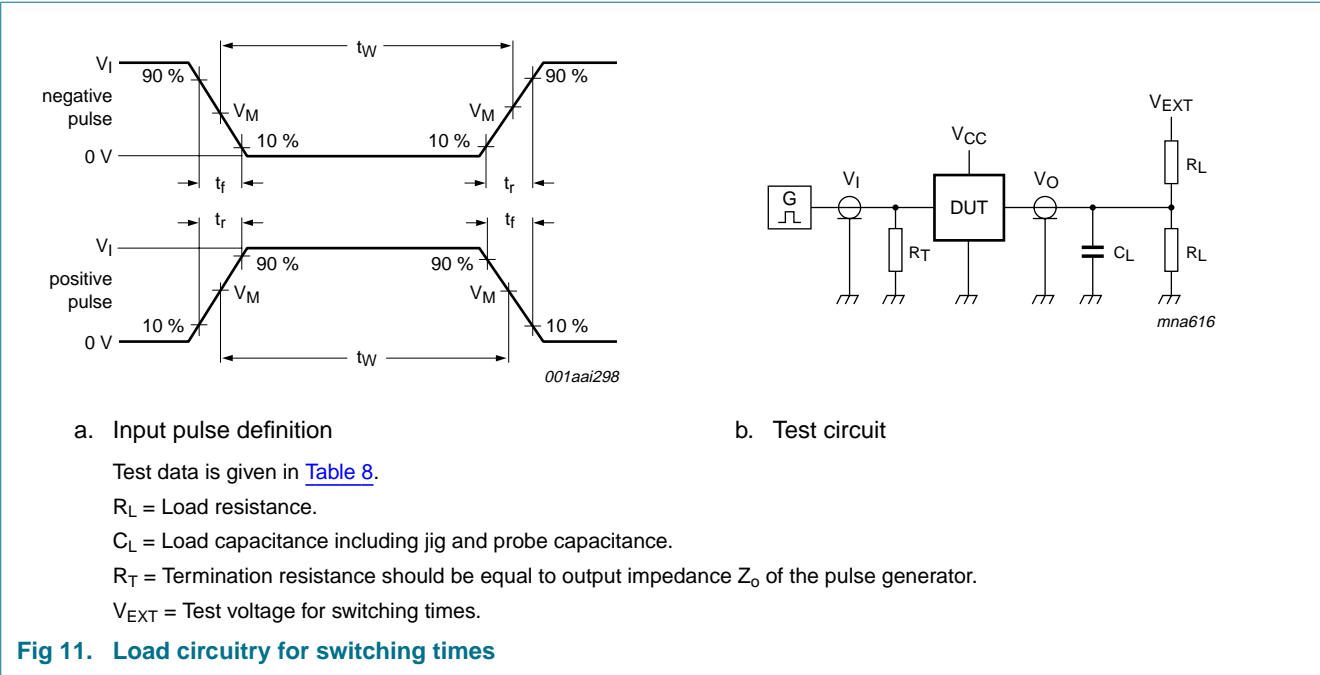


Table 8. Test data

| Input |       |        |               | Load  |              | $V_{EXT}$          |                    |                    |
|-------|-------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| $V_I$ | $f_I$ | $t_W$  | $t_r, t_f$    | $C_L$ | $R_L$        | $t_{PHL}, t_{PLH}$ | $t_{PZH}, t_{PHZ}$ | $t_{PZL}, t_{PLZ}$ |
| 3.0 V | 1 MHz | 500 ns | $\leq 2.5$ ns | 50 pF | 500 $\Omega$ | open               | open               | 7.0 V              |

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

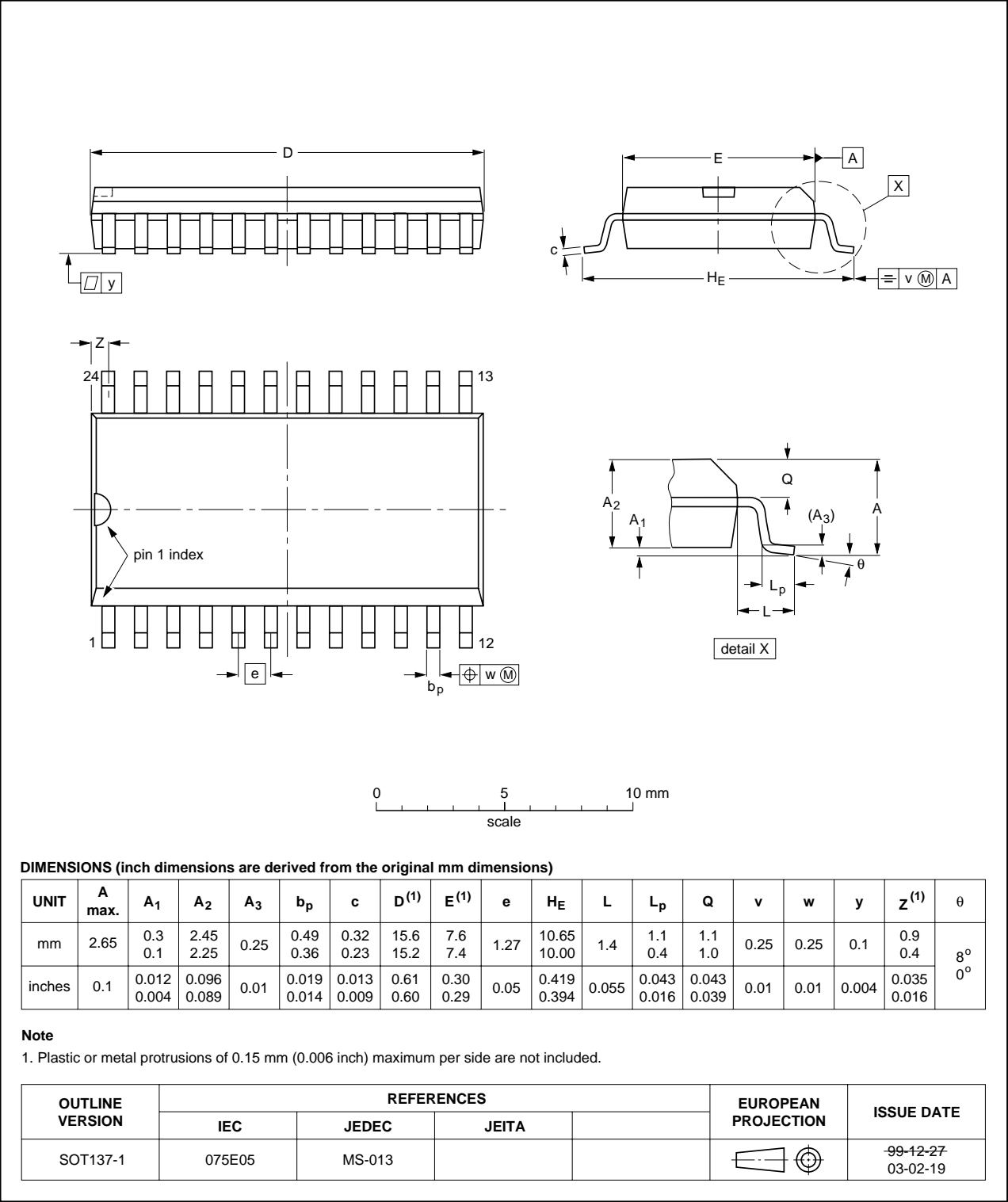


Fig 12. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

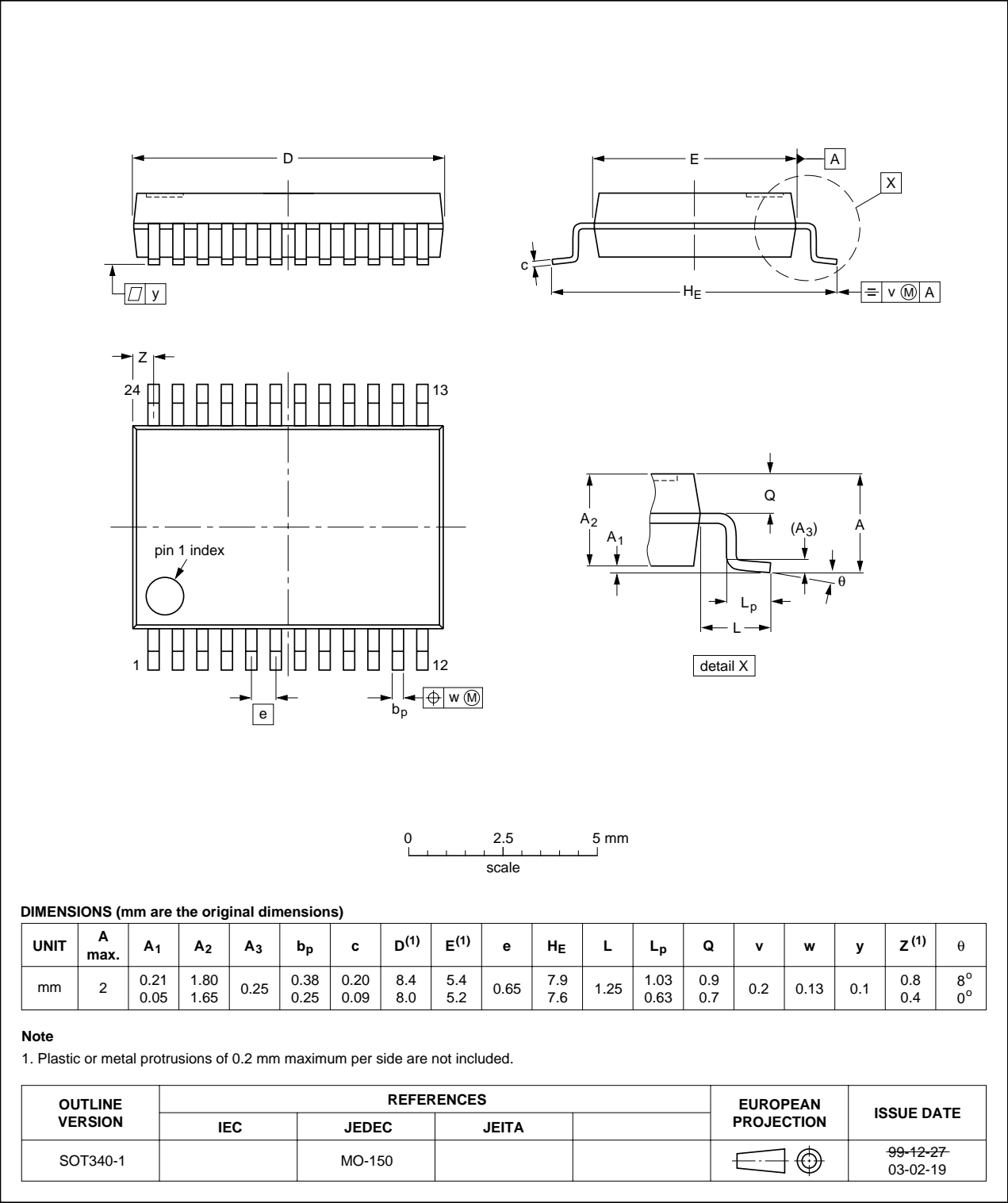


Fig 13. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

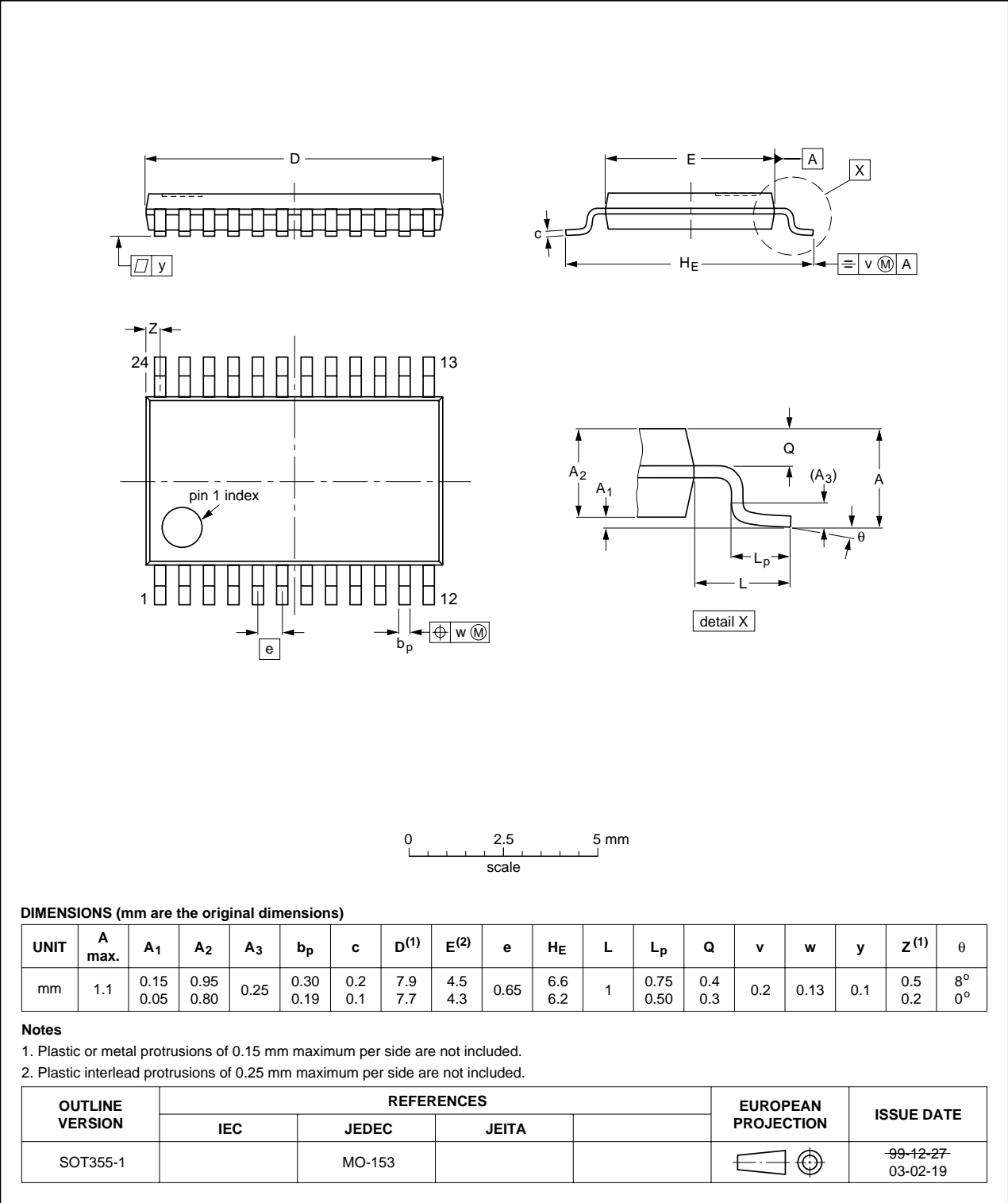


Fig 14. Package outline SOT355-1 (TSSOP24)

## 13. Abbreviations

Table 9. Abbreviations

| Acronym | Description                                     |
|---------|---|
| BiCMOS  | Bipolar Complementary Metal-Oxide Semiconductor |
| DUT     | Device Under Test                               |
| ESD     | ElectroStatic Discharge                         |
| HBM     | Human Body Model                                |
| MM      | Machine Model                                   |

## 14. Revision history

Table 10. Revision history

| Document ID    | Release date   | Data sheet status     | Change notice | Supersedes  |
|----------------|--|-----------------------|---------------|-------------|
| 74ABT646A_3    | 20100315   | Product data sheet    | -             | 74ABT646A_2 |
| Modifications: | <ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• DIP 24 (SOT222-1) package removed from <a href="#">Section 3 “Ordering information”</a> and <a href="#">Section 12 “Package outline”</a>.</li></ul> |                       |               |             |
| 74ABT646A_2    | 19980217   | Product specification | -             | 74ABT646A_1 |
| 74ABT646A_1    | 19950906   | Product specification | -             | -           |



## 15. Legal information

### 15.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

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