UM10404

Greenchip 45 W TEA1733(L)T demo board for LCD monitor

Rev. 1 — 25 June 2010 **User manual**

Document information

Info	Content
Keywords	45 W typical, LCD monitor application, evaluation board with GreenChip, flyback, controller, SMPS, TEA1733(L)T.
Abstract	This manual describes the specification, schematics and PCB layout of the 45 W TEA1733(L)T demo board. For details on the controller device, please refer to TEA1733(L)T application note AN10868.

Revision history

Rev	Date	Description
v1	20100625	First issue

Contact information

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1. Introduction

The GreenChip 45 W TEA1733(L)T demo board for LCD monitor demonstrates the capabilities of the TEA1733T and TEA1733LT Switched-Mode Power Supply (SMPS) controller for typical LCD monitor applications. This user manual provides the 45 W TEA1733(L)T demo board's specification, schematics and PCB layout. Details of the TEA1733T and TEA1733LT SMPS controller are available in application note *AN10868* Ref. 1 and data sheet *TEA1733T_TEA1733LT* Ref. 2.

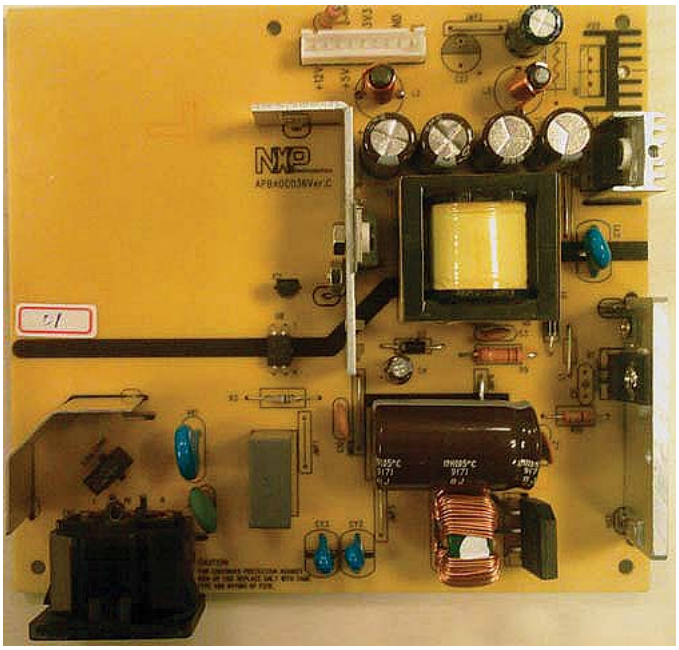

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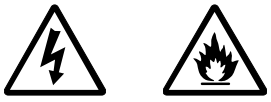
Fig 1. 45 W TEA1733(L)T demo board

WARNING

Lethal voltage and fire ignition hazard



The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire.

This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel that is qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

2. Features

The features below enable the power supply engineer to design a reliable and cost-effective SMPS using a minimum number of external components and the possibility to deal with the high efficiency requirements.

- Universal mains supply operation (70 V AC to 276 V AC)
- High level of integration, resulting in very low external component count
- Constant frequency operation
- Safe restart mode for system fault conditions
- UnderVoltage Protection (UVP) (foldback during overload)
- IC OverTemperature Protection (OTP) (latched)
- Low and adjustable OverCurrent Protection (OCP) trip level
- Soft restart
- Mains voltage dependent operation enabling level
- General purpose input for latched or safe protection and timing such as OverVoltage Protection (OVP), output Short Circuit Protection (SCP) or system OverTemperature Protection (OTP)

3. Specification

Table 1. Input specification

Symbol	Description	Conditions	Specification	Unit
V_i	input voltage		90 to 264	V
f_i	input frequency		47 to 60	Hz
$P_{i(no\ load)}$	no load input power	at 230 V (AC)	< 100	mW

Table 2. Output specification

Symbol	Description	Conditions	Specification	Unit
V_{o1}	output voltage 1	-	5	V
V_{o2}	output voltage 2	-	12	V
$V_{o(ripple)(p-p)}$	peak-to-peak output ripple voltage	20 MHz bandwidth	≤ 100	mV
I_{o1}	output current 1	continuous	0 to 2	A
I_{o2}	output current 2	continuous	0 to 3	A
P_o	output power	0 °C to 40 °C	45	W
t_{holdup}	hold-up time	at 115 V/60 Hz; full load	5	ms
-	line regulation	-	±1	%
-	load regulation	-	±5	%
$t_{startup}$	start-up time	at 115 V/60 Hz	≥2	s
η	efficiency	according to ENERGY STAR (EPS 2)	≥82	%
-	EMI	CISPR22 compliant	pass	-

4. Performance data

4.1 Test facility

- Programmable AC source: Chroma 61503
- Power analyzer: Chroma 6630
- DC electronic load: Chroma 63102
- Digital phosphor oscilloscope: Tektronix TDS5104B
- 6½ digit multimeter: Agilent 34401A

4.2 Standby power consumption

4.2.1 Test conditions

Measure input power (P_i) at no load and light load conditions.

4.2.2 Test results

Table 3. Input power test results

Input voltage	Load output 1	Load output 2	5 V output	12 V output	Input power (P_i)	Specification	Audible noise	Result
90 V, 60 Hz	0 A	0 A	4.85 V	12.16 V	33 mW	< 100 mW	free	pass
90 V, 60 Hz	5 mA	0 A	4.78 V	12.25 V	67 mW	< 100 mW	free	pass
264 V, 50 Hz	0 A	0 A	4.85 V	12.15 V	70 mW	< 100 mW	free	pass
264 V, 50 Hz	5 mA	0 A	4.78 V	12.24 V	97 mW	< 100 mW	free	pass

4.3 Start-up time

4.3.1 Test conditions

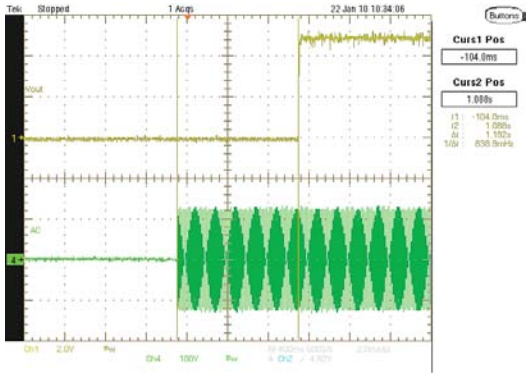
Set output (V_o) to full load and measure the interval ($t_{startup}$) from input voltage applied to stable output.

4.3.2 Test results

Table 4. Start-up time test results

Input voltage	$t_{startup}$ at 5 V output	Specification	Result
90 V, 60 Hz	1.19 s	< 2.0 s	pass
264 V, 50 Hz	608 ms	< 2.0 s	pass

4.3.3 Start-up time waveforms



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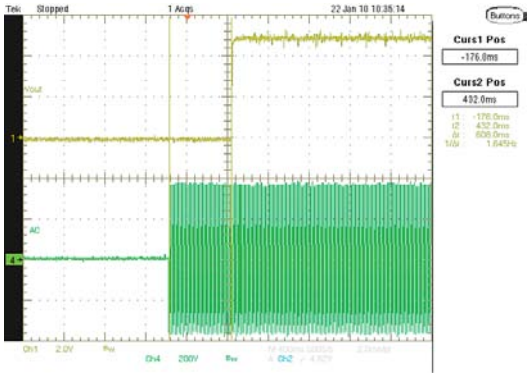
a. 90 V, 60 Hz at full load



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b. 264 V, 50 Hz at full load

Fig 2. Start-up time waveforms

4.4 Line and load regulation

4.4.1 Test conditions

Measure line and load voltage regulation ($V_{L(reg)}$) at no load and full load conditions.

4.4.2 Test results

Table 5. Load voltage regulation test conditions

Input voltage	Output conditions				Specifications	Result
90 V, 60 Hz	5 V at 0 A	12.16 V	5 V at 2 A	11.94 V	5 V ± 1 % line regulation; 5 V ± 5 % load regulation	pass
	12 V at 0 A	4.85 V	12 V at 3 A	4.98 V		
180 V, 50 Hz	5 V at 0 A	12.16 V	5 V at 2 A	11.94 V		
	12 V at 0 A	4.85 V	12 V at 3 A	4.97 V		
264 V, 50 Hz	5 V at 0 A	12.15 V	5 V at 2 A	11.94 V		
	12 V at 0 A	4.86 V	12 V at 3 A	4.97 V		

4.5 Efficiency

4.5.1 Test conditions

Output power at maximum load by universal input voltage.

4.5.2 Test results

Table 6. Efficiency test results

Input voltage	Input power (P_i)	Output power (P_o)	Efficiency (η)	Specification	Result
90 V, 60 Hz	53.7 W	45.46 W	84.65 %	> 80 %	pass
110 V, 60 Hz	53.0 W	45.45 W	85.76 %	> 80 %	pass
180 V, 50 Hz	52.5 W	45.46 W	86.59 %	> 80 %	pass
220 V, 50 Hz	52.5 W	45.47 W	86.61 %	> 80 %	pass
264 V, 50 Hz	52.6 W	45.48 W	86.47 %	> 80 %	pass

4.6 Dynamic loading

4.6.1 Test conditions

- Dynamic loading. Step load change: 1 A to 2 A load at 5 V.
- Dwell time: 1 kHz to 20 kHz at 5 V at the same time.
- Slew rate: 0.1 A/μs.

4.6.2 Test results

Table 7. Dynamic loading test results: dwell time = 1 kHz, T = 0.5 ms

Input voltage	Output	$V_{o(ripple)(p-p)}$
90 V, 47 Hz	12 V	32 mV
90 V, 47 Hz	5 V	168 mV
264 V, 63 Hz	12 V	40 mV
264 V, 63 Hz	5 V	176 mV

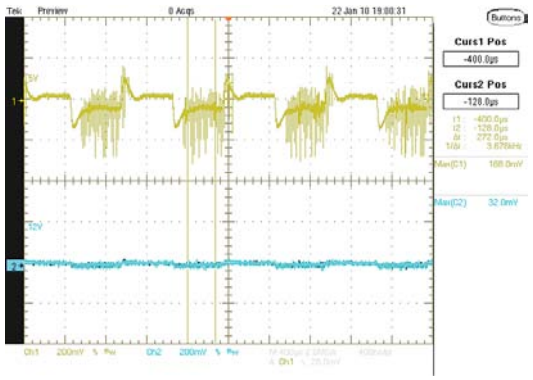
Table 8. Dynamic loading test results: dwell time = 10 kHz, T = 0.05 ms

Input voltage	Output	$V_{o(ripple)(p-p)}$
90 V, 47 Hz	12 V	40 mV
90 V, 47 Hz	5 V	144 mV
264 V, 63 Hz	12 V	32 mV
264 V, 63 Hz	5 V	144 mV

Table 9. Dynamic loading test results: dwell time = 20 kHz, T = 0.025 ms

Input voltage	Output	$V_{o(ripple)(p-p)}$
90 V, 47 Hz	12 V	40 mV
90 V, 47 Hz	5 V	112 mV
264 V, 63 Hz	12 V	40 mV
264 V, 63 Hz	5 V	104 mV

4.6.3 Output voltage transient response waveforms



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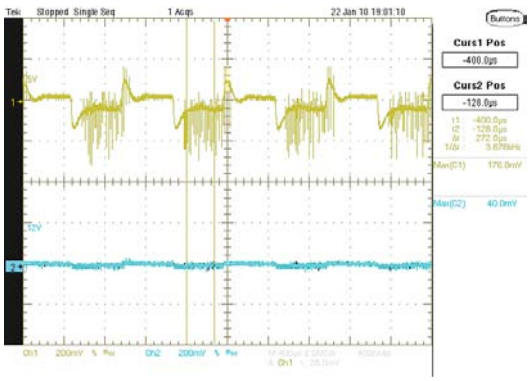

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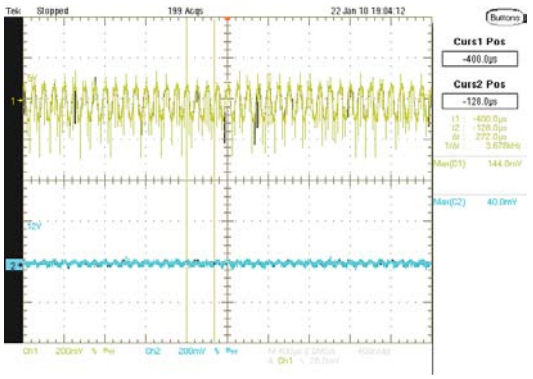
a. 90 V; 47 Hz.

b. 264 V; 63 Hz.

Fig 3. Load transient response, ripple and noise; 1 kHz dwell time



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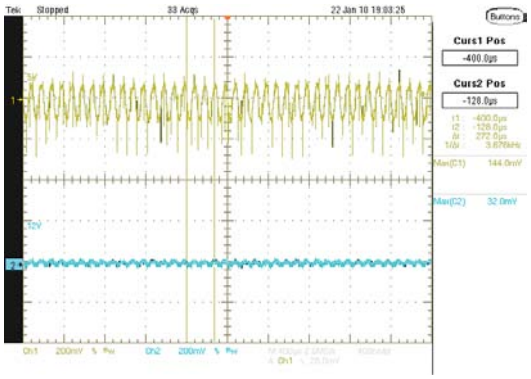

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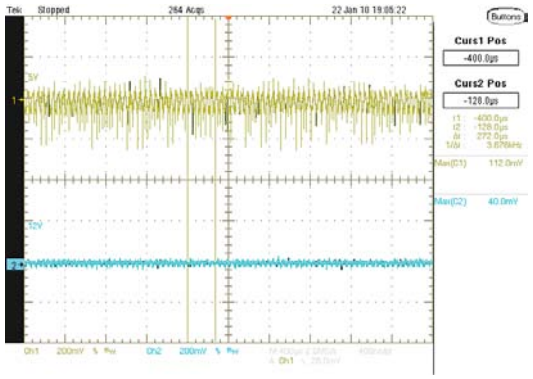
a. 90 V; 47 Hz.

b. 264 V; 63 Hz.

Fig 4. Load transient response, ripple and noise; 10 kHz dwell time



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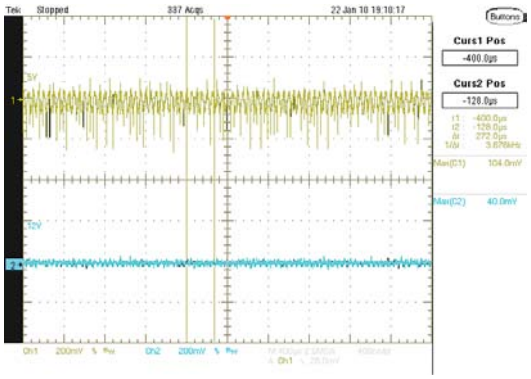
a. 90 V; 47 Hz.



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b. 264 V; 63 Hz.

Fig 5. Load transient response, ripple and noise; 20 kHz dwell time

4.7 Output ripple and noise

4.7.1 Test conditions

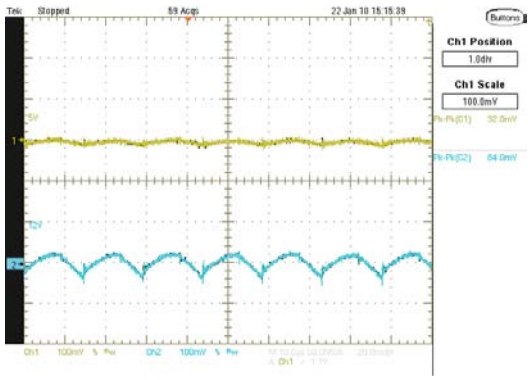
Ripple and noise are measured using a 20 MHz bandwidth-limited oscilloscope with a 10 µF capacitor in parallel with a high frequency 0.1 µF capacitor across each output at full load.

4.7.2 Test results

Table 10. Output ripple and noise test results

Input voltage	Output	Load	Ripple and noise	Specification	Result
90 V, 60 Hz	5 V	2 A	32 mV	< 100 mV	pass
90 V, 60 Hz	12 V	3 A	84 mV	< 100 mV	pass
264 V, 50 Hz	5 V	2 A	32 mV	< 100 mV	pass
264 V, 50 Hz	12 V	3 A	80 mV	< 100 mV	pass

4.7.3 Output voltage ripple and noise waveforms



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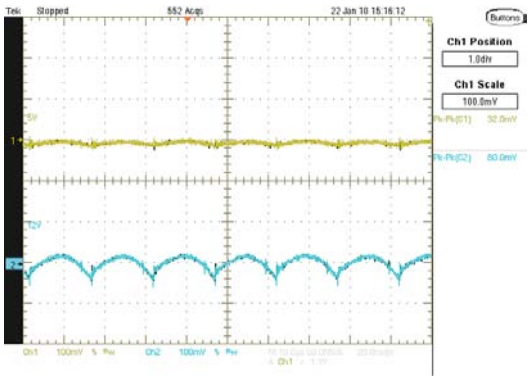
a. 90 V, 60 Hz



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b. 264 V, 50 Hz

Fig 6. Output voltage ripple and noise waveforms

4.8 Overpower protection

4.8.1 Test conditions

Measure the overpower protection point by increasing the output load gradually at minimum and maximum universal input voltage.

4.8.2 Test results

Table 11. Overpower protection test results (output 2 = 12 V, 3 A, 36 W fixed)

Input voltage	Overpower protection		Comment	Note
	Output	Measured		
90 V, 60 Hz	5 V output 1	4.15 A output	same results at maximum and minimum input voltage	auto-restart
264 V, 50 Hz	5 V output 1	4.02 A output		auto-restart

4.9 Hold-up time

4.9.1 Test conditions

Set the output to full load and measure the time interval [hold-up time (t_{holdup})] between input voltage off (at zero-crossing) and the output voltage falling to the lower limit of the rated value.

4.9.2 Test results

Table 12. Hold-up time test results

Input voltage	t_{holdup} at output 1	Specification	Result
90 V, 60 Hz	13.6 ms	> 6 ms	pass

4.9.3 Hold-up time output voltage waveform

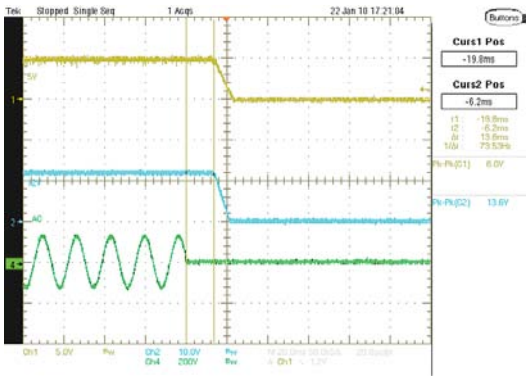

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Fig 7. Waveform of output: 90 V, 60 Hz

4.10 Short-circuit protection

4.10.1 Test conditions

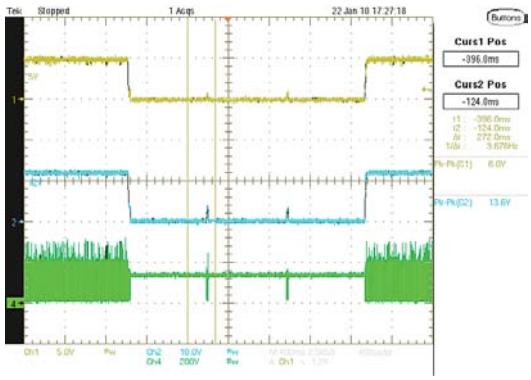
Short the output of the power supply, it should enter safe restart mode with less than 5 W input power.

4.10.2 Test results

Table 13. Short-circuit protection test results

Input voltage	Specification	Result
90 V, 60 Hz	safe restart	pass
264 V, 50 Hz	safe restart	pass

4.10.3 Short-circuit protection output voltage waveforms



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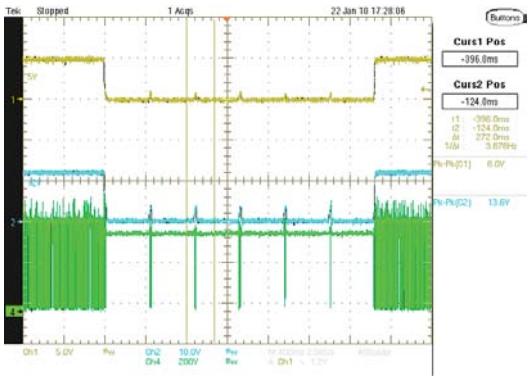
a. 90 V, 60 Hz



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b. 264 V, 50 Hz

Fig 8. Short-circuit protection output voltage waveforms

4.11 Overvoltage protection

4.11.1 Test conditions

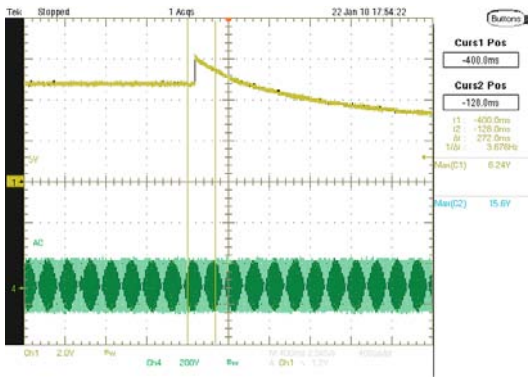
Measure the output voltage while shorting the secondary side of the photocoupler. The system should enter the safe restart mode or the latch mode. The output voltage should meet the specification for no load and for the 0.2 A load condition.

4.11.2 Test results

Table 14. Overvoltage protection test results

5 V load	5 V output with OVP	Specification	Result
0 A	6.24 V	7 V	pass
0.2 A	6.16 V	7 V	pass

4.11.3 Overvoltage protection output voltage waveforms



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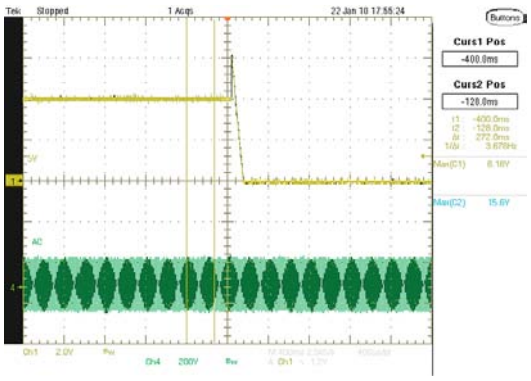
a. Output voltage at 0 A



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b. Output voltage at 0.2 A

Fig 9. Overvoltage protection output voltage waveforms

4.12 Conduction EMI

Conditions:

- Type: conducted EMC measurement
- Frequency range: 150 kHz to 30 MHz
- Output power: full load condition
- Supply voltage: 115 V and 230 V
- Margin: 10 dB below limit
- Measuring time: 160 ms
- Secondary ground connected to mains earth ground

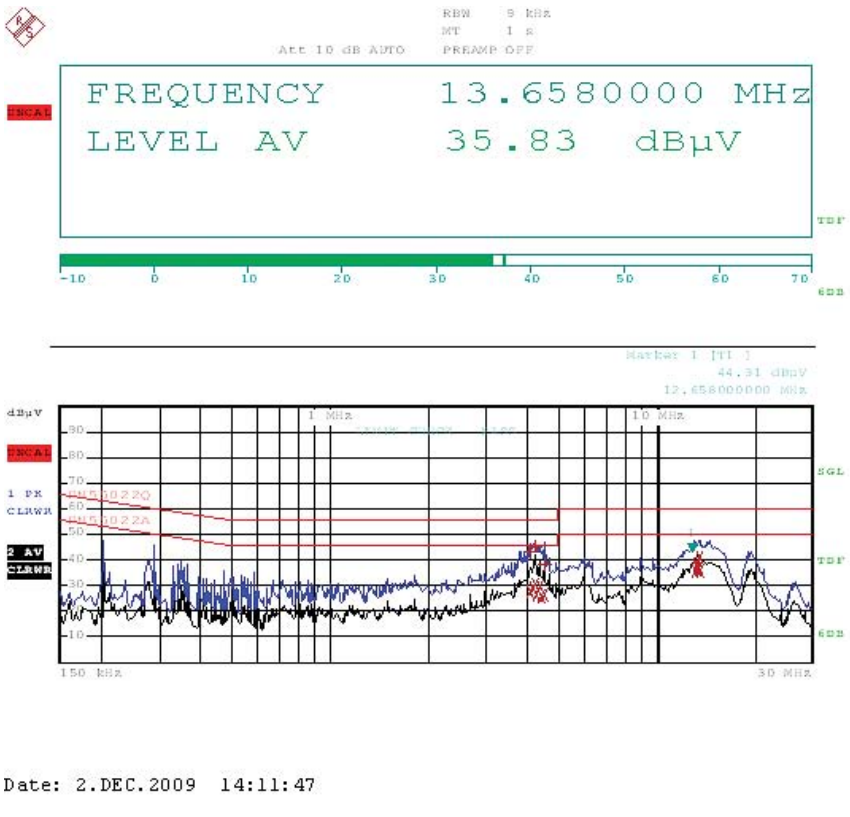

Fig 10. Conduction EMI, 115 V supply voltage

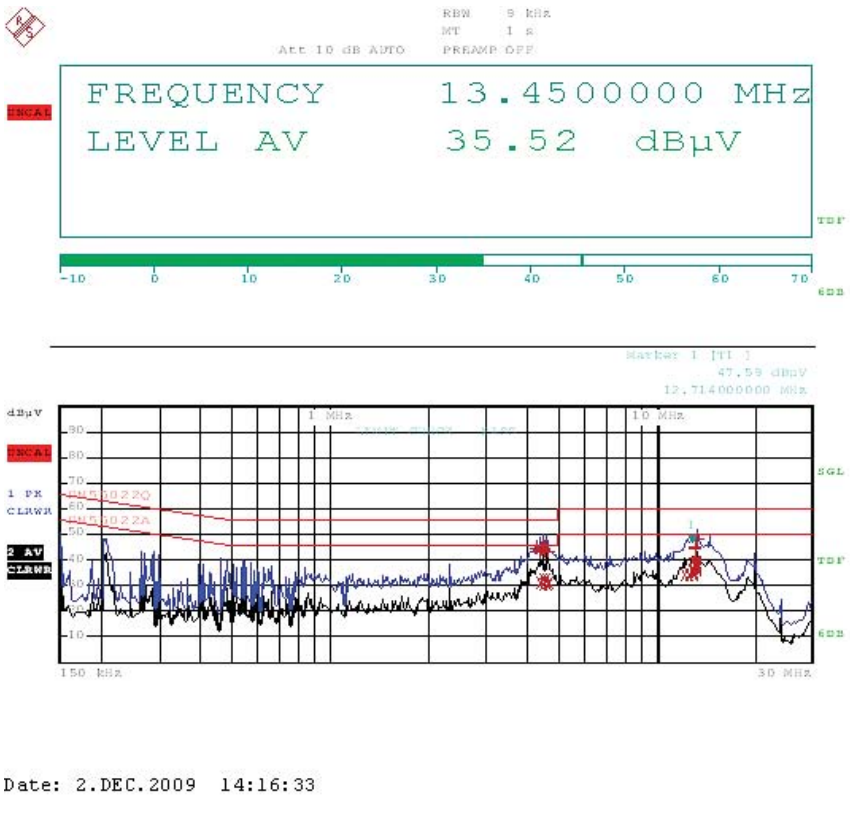

Fig 11. Conduction EMI, 230 V supply voltage

5. Circuit description

The 45 W TEA1733(L)T demo board for LCD monitor applications comprises the following:

- input section, containing a bridge diode rectifier and filtering section
- primary switching section operating in flyback mode
- two output sections (5 V and 12 V)
- optional third output (3V3)
- feedback section

5.1 Input section

The input section consists of a start-up circuit that generates the initial supply voltage for the TEA1733 device from the mains input voltage. After start-up, the device is powered from the auxiliary winding. A common-mode choke and capacitors are used to reduce noise and harmonics generated by the primary switching section. A bridge diode rectifier and bulk capacitor are connected after the filter section. Finally, a resistive divider network is applied for start-up and for brown-out and OVP protection.

5.2 Primary switching circuit

The primary switching circuit uses the NXP Semiconductor's TEA1733 device in combination with a N-channel high voltage MOSFET switch. A RCD snubber circuit is connected to deal with the energy stored in the stray inductance of the primary winding of the transformer.

5.3 Output sections

There are two controlled secondary flyback stages, delivering two DC outputs of 5 V and 12 V respectively. Both outputs contain low-pass chokes to filter out high frequency content. The demo board provides an optional 3V3 output derived from the 5 V voltage. If required, the 3V3 output can be implemented by adding resistor R28, capacitor C23 and regulator IC U9 as shown in the complete circuit diagram Figure 12.

5.4 Feedback section

The feedback section measures the output voltages of both secondary sections (5 V and 12 V) and feeds the information back to the TEA1733 device via an optocoupler circuit. The demo board uses an accurate voltage reference device (TL431: reference voltage 2.5 V) to produce two well-regulated outputs.

6. Circuit diagram

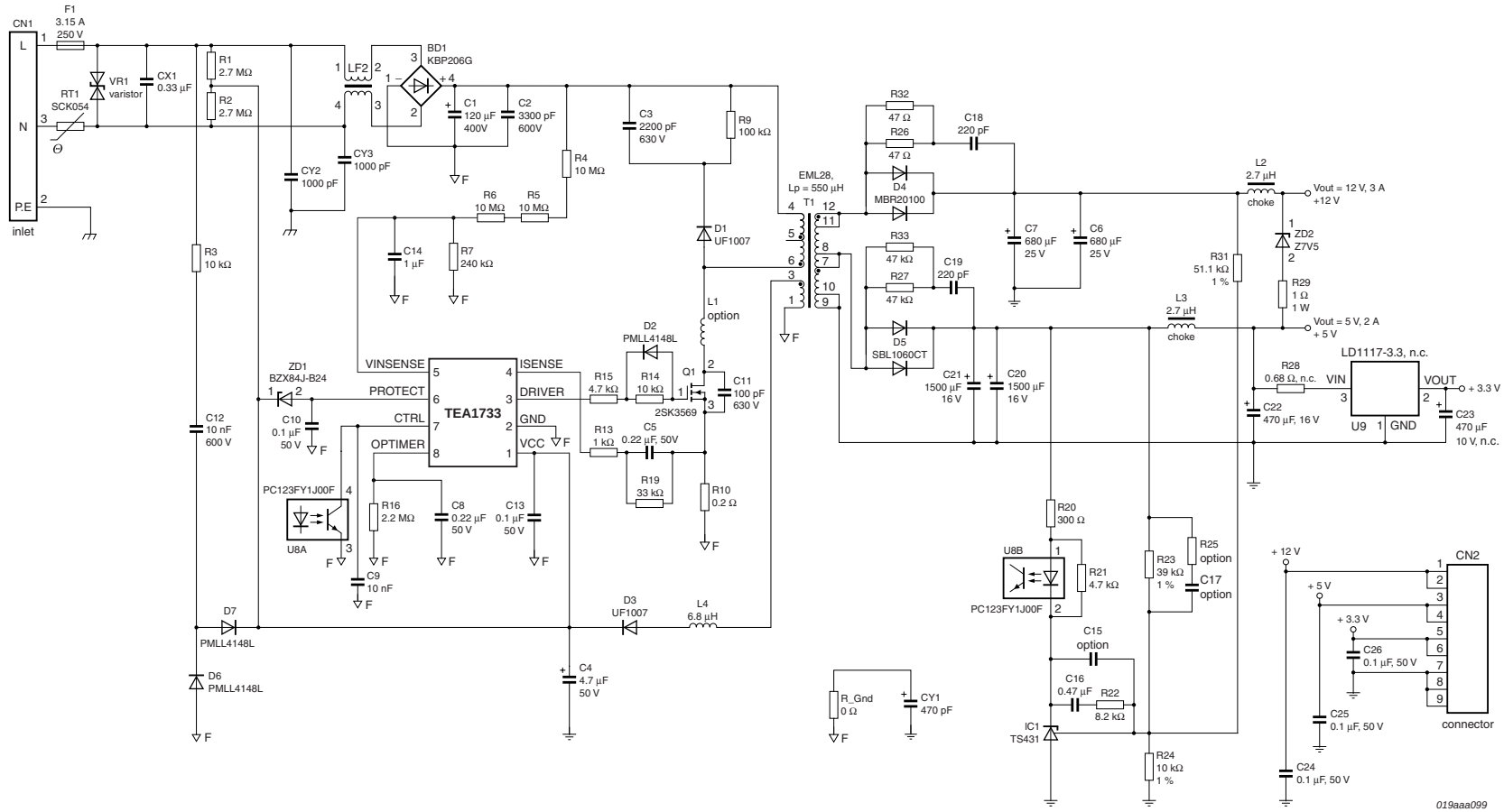

Fig 12. Complete circuit diagram

7. Bill of materials

Table 15. Resistors

Item	Description	Value	Designation	Quantity
1	resistor, SMD 1206 thin film chip	2.7 MΩ; 5 %	R1; R2	2
2	resistor, SMD 1206 thin film chip	10 MΩ; 5 %	R4; R5; R6	3
3	resistor, SMD 0805 thin film chip	0 Ω; 5 %	R_GND	1
4	resistor, SMD 0603 thin film chip	330 Ω; 5 %	R20	1
5	resistor, SMD 0805 thin film chip	10 Ω; 5 %	R14	1
6	resistor, axial lead, MOF 0.125 W	10 kΩ; 5 %	R3	1
7	resistor, SMD 0805 thin film chip	4.7 Ω; 5 %	R15	1
8	resistor, SMD 0805 thin film chip	47 Ω; 5 %	R26; R27; R32; R33	4
9	resistor, SMD 0603 thin film chip	240 kΩ; 5 %	R7	1
10	resistor, SMD 0603 thin film chip	1 kΩ; 5 %	R13	1
11	resistor, SMD 0603 thin film chip	2.2 MΩ; 5 %	R16	1
12	resistor, SMD 0603 thin film chip	33 kΩ; 5 %	R19	1
13	resistor, axial lead, MOF 1 W, small size	1 Ω; 5 %	R29	1
14	resistor, SMD 0603 thin film chip	4.7 kΩ; 5 %	R21	1
15	resistor, SMD 0603 thin film chip	8.2 kΩ; 5%	R22	1
16	resistor, SMD 0603 thin film chip	39 kΩ; 1 %	R23	1
17	resistor, SMD 0603 thin film chip	10 kΩ; 1 %	R24	1
18	resistor, axial lead, MOF 1 W, small size	100 kΩ; 5 %	R9	1
19	resistor, axial lead, MOF 0.5 W, small size	0.2 Ω; 5 %	R10	1
20	resistor, SMD 0603 thin film chip	51.1 kΩ; 1 %	R31	1
21	thermistor, pitch 10 mm	2.5 Ω; 5 A	RT1	1

Table 16. Capacitors

Item	Description	Value	Designation	Quantity
1	ceramic; Y1-cap; disc 9ϕ; KX/Murata	470 pF; 250 V AC	CY1	1
2	ceramic; Y2-cap; disc 9ϕ; KX/Murata	1000 pF; 250 V AC	CY2; CY3	2
3	MPX; x-cap	0.33 μF; 275 V AC	CX1	1
4	ceramic capacitor; disc 5ϕ	10 nF; 630 V	C12	1
5	E/C; radial lead; 105 °C; 18 × 35 mm; TY/LTEC	120 μF; 400 V	C1	1
6	ceramic capacitor; disc; 5ϕ	3300 pF; 630 V	C2	1
7	ceramic capacitor; disc; 5ϕ	2200 pF; 630 V	C3	1
8	MLCC; SMD 0603; X7R	100 nF; 50 V	C10; C13; C24; C25; C26	5

Table 16. Capacitors *…continued*

Item	Description	Value	Designation	Quantity
9	MLCC; SMD 0603; X7R	1 μF; 50 V	C14	1
10	MLCC; SMD 1206	100 pF; 630 V	C11	1
11	MLCC; SMD 0603; X7R	0.22 μF; 50 V	C5; C8	2
12	MLCC; SMD 0805; X7R	220 pF; 50 V	C18; C19	2
13	E/C; radial lead; 105 °C; 5 × 11 mm; LZP/LTEC	4.7 μF; 50 V	C4	1
14	E/C; radial lead; 105 °C; 10 × 20 mm; LZP/LTEC	680 μF; 25 V	C6; C7	2
15	E/C; radial lead; 105 °C; 10 × 20 mm; LZP/LTEC	1500 μF; 16 V	C20; C21	2
16	MLCC; SMD 0603; X7R	470 nF; 50 V	C16	1
17	MLCC; SMD 0603; X7R	10 nF; 50 V	C9	1
18	E/C; radial lead; 105 °C; 8 × 15 mm; LZP/LTEC	470 μF; 16 V	C22	1

Table 17. Diodes and transistors

Item	Description	Value	Designation	Quantity
1	bridge diode; flat/mini; KBP206G	2 A; 600 V	BD1	1
2	varistor; TVR10471K		VR1	1
3	switching diode; SMD SOD-80; LL4148; Philips	0.2 A; 75 V	D2; D6; D7	3
4	diode; ultra/super fast diode; UF1007	1 A; 1000 V	D1; D3	2
5	Zener diode; SMD SOD323F; BZX84J-B22; Philips	24 V	ZD1	1
6	Zener diode; SMD SOD323F; BZX84J-B7V5; Philips	7.5 V	ZD2	1
7	Schottky diode; TO220AB; MBR20100CT; Lite-On (SP10100)	20 A; 100 V	D4	1
8	Schottky diode; TO220AB; SBL1060CT (SP1060)	10 A; 60 V	D5	1
9	MOSFET; TO220-3-31; 2SK3569; Hitachi	7.3 A; 650 V	Q1	1

Table 18. Integrated circuits

Item	Description	Value	Designation	Quantity
1	SMPS controller IC; SO8; TEA1733T; NXP		U2	1
2	optocoupler; CTR = 130 ~ 260; PC123		U8	1
3	voltage regulator; TO92; TS431		IC1	1

Table 19. Choke, transformer and other items

Item	Description	Value	Designation	Quantity
1	transformer; SP09Z317; ERL-28; 3C90; 3900G/TDK	550 μH	T1	1
2	bead	Z45/100 MHz	L1	1
3	line choke; SP05D100; T12 × 6 × 4; 0.6ϕ × 9.5 T; /Send power	380 μH	LF1 (not mounted)	1
4	line choke; SP09Z271; T16 × 12 × 8 C; 0.6ϕ × 48.5 T; /Send power	5 mH	LF2	1
5	power choke; R4 × 15; 1.2 D × 7.5 T; /Send power	2.7 μH	L2; L3	2
6	MLCC; SMD 0603	6.8 μH	L4	1
7	fuse; /MST	3.15 A; 250 V	F1	1
8	connector; 3-pin		CN1	1
9	connector; 9-pin		CN2	1
10	jumper; 1D; pitch 10 mm		JMP6	1
11	jumper; 0.6D; pitch 10 mm		JMP2; JMP3	2
12	jumper; 0.6D; pitch 12.7 mm		JMP5	1
13	jumper; 0.6D; pitch 15 mm		JMP4	1

7.1 Transformer specification

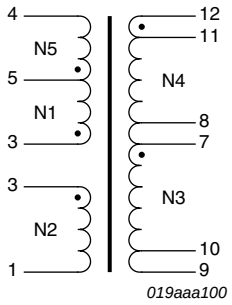

Fig 13. Transformer

7.1.1 Transformer winding specification

Table 20. Transformer winding

Layer	Winding		Wire	Turns	Winding method	Tape insulation		
	Start	Finish				No	Turns	Width
N1	6	5	0.35ϕ × 2	21	uniform	S1	1	16.2 mm
COPPER		1	0.025T; 12 mm (copper foil)	1	center			
N2	11	7	0.6ϕ × 2 (3L)	4	uniform	S2	1	16.2 mm
N3	3	1	0.3ϕ × 2	11	uniform	S3	1	16.2 mm
N4	7	9	0.6ϕ × 2 (3L)	3	parallel and uniform	S4	1	16.2 mm
	8	10						
COPPER		1	0.025T; 12 mm (copper foil)	1	center			
N5	5	4	0.35ϕ × 2	21	uniform	S5	3	16.2 mm

7.1.2 Electrical characteristics

Table 21. Electrical characteristics

Description	Pin	Specification	Remark
Inductance	4 to 6	550 μH ± 5 %	60 kHz; 1 V
Leakage inductance	4 to 6	< 8 μH	secondary side all shorted

7.1.3 Core and bobbin

- **Core**: ER2828 (TDK PC40)
- **Bobbin**: ER-28-H-12P (12-pin, horizontal type)

$\mathbf{A_e}$: 81.4 mm^2

8. TEA1733(L)T demo board PCB layout

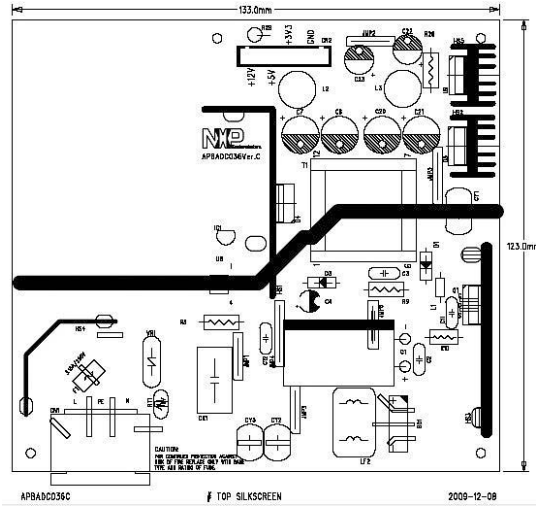

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Fig 14. Top silkscreen

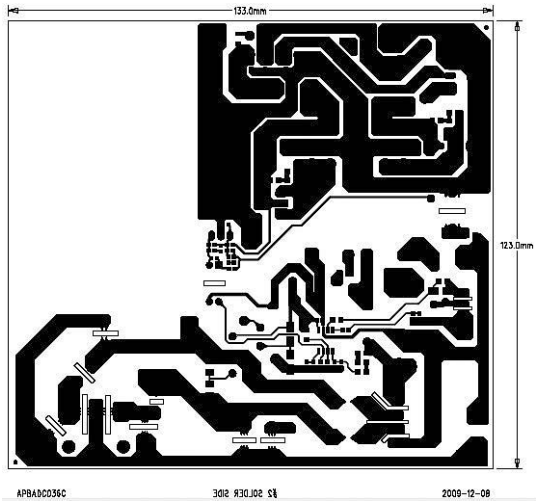

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Fig 15. Bottom view

The TEA1733(L)T demo board for LCD monitor applications is a single-sided board, with the following specification and size:

- Technology: single-sided, CEM-3, 1-OZ
- Dimensions: 133 mm (L), 123 mm (W) and 23 mm (H)

8.1 PCB layout considerations

Important points for correct layout are:

- On the primary side, keep large signal and small signal tracks separate
- Connect a resistor in series with the soft start capacitor to prevent EMI distortion and offset level
- Keep the area and the length of the drain track (high alternating voltages) as small as possible
- Noise can be reduced by minimizing the area of current loops with fast alternating currents, such as locations 1 and 2 in Figure 16
- Keep the components as close as possible to IC pins PROTECT, CTRL and ISENSE and keep their lead lengths as short as possible
- Use a single GND on the primary side connection to the bulk capacitor negative (–) terminal.
- Do not use a “floating” heatsink, but connect the heatsink to the primary GND directly or via a capacitor. Use the heatsink as an EMI shield between the small signal and the large signal parts.
- Connect the CY1 capacitor between the primary GND and the secondary GND with a short track to the primary buffer capacitor. Prevent a common GND with the controller.
- Keep the track length of the loops from ground to ISENSE, DRIVER and CTRL as short as possible. Also keep these high impedance input loops away from the MOSFET drain track which contains high current spikes.
- Use a serial resistor between V (DC) to drain (pin 8) to obtain enough maximum voltage rating

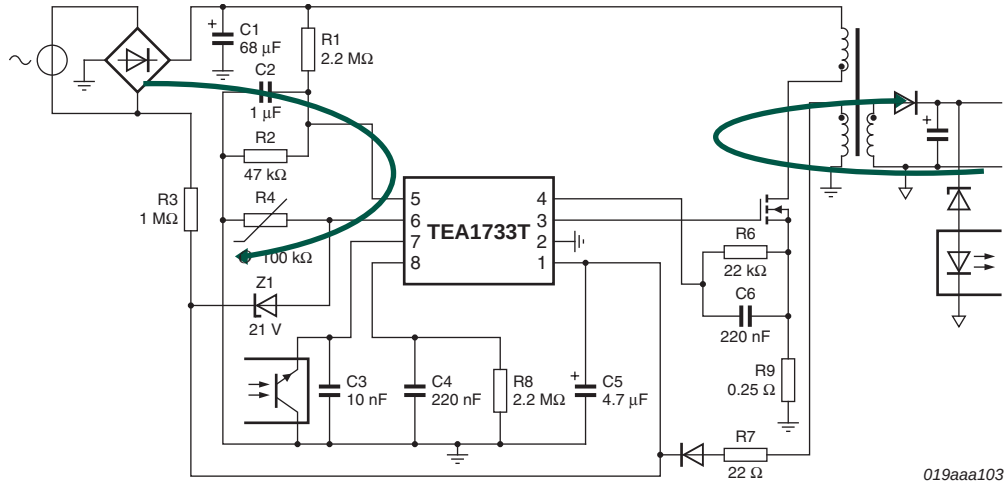

Fig 16. TEA1733(L)T demo board layout considerations

9. Abbreviations

Table 22. Abbreviations

Acronym	Description
CTR	Current Transfer Ratio
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
MLCC	Multi-Layer Ceramic Capacitor
MOF	Metal Oxide Film
MPX	Metallized PolyPropylene film (capacitor)
PCB	Printed-Circuit Board
RCD	Residual Current Detector
SMD	Surface Mounted Device

10. References

[1] **AN10868 —** GreenChip TEA1733(L) fixed frequency flyback controller, application note, revision 01, 9 December 2009.

[2] **TEA1733T_TEA1733LT —** GreenChip SMPS control IC, data sheet, revision 01, 26 October 2009.

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