

74AVC4TD245

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 2 — 9 December 2011

Product data sheet

1. General description

The 74AVC4TD245 is a 4-bit, dual supply transceiver that enables bidirectional level translation. It features eight 1-bit input-output ports (A_n and B_n), four direction control inputs (DIR1, DIR2, DIR3 and DIR4), an output enable input (\overline{OE}) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins A_n , \overline{OE} and DIRn are referenced to $V_{CC(A)}$ and pins B_n are referenced to $V_{CC(B)}$. A HIGH on DIRn allows transmission from A_n to B_n and a LOW on DIRn allows transmission from B_n to A_n . The output enable input (\overline{OE}) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both A_n and B_n are in the high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range:
 - ◆ $V_{CC(A)}$: 0.8 V to 3.6 V
 - ◆ $V_{CC(B)}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
 - ◆ JESD8-12 (0.8 V to 1.3 V)
 - ◆ JESD8-11 (0.9 V to 1.65 V)
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
 - ◆ 380 Mbit/s (\geq 1.8 V to 3.3 V translation)
 - ◆ 200 Mbit/s (\geq 1.1 V to 3.3 V translation)
 - ◆ 200 Mbit/s (\geq 1.1 V to 2.5 V translation)
 - ◆ 200 Mbit/s (\geq 1.1 V to 1.8 V translation)
 - ◆ 150 Mbit/s (\geq 1.1 V to 1.5 V translation)
 - ◆ 100 Mbit/s (\geq 1.1 V to 1.2 V translation)



- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

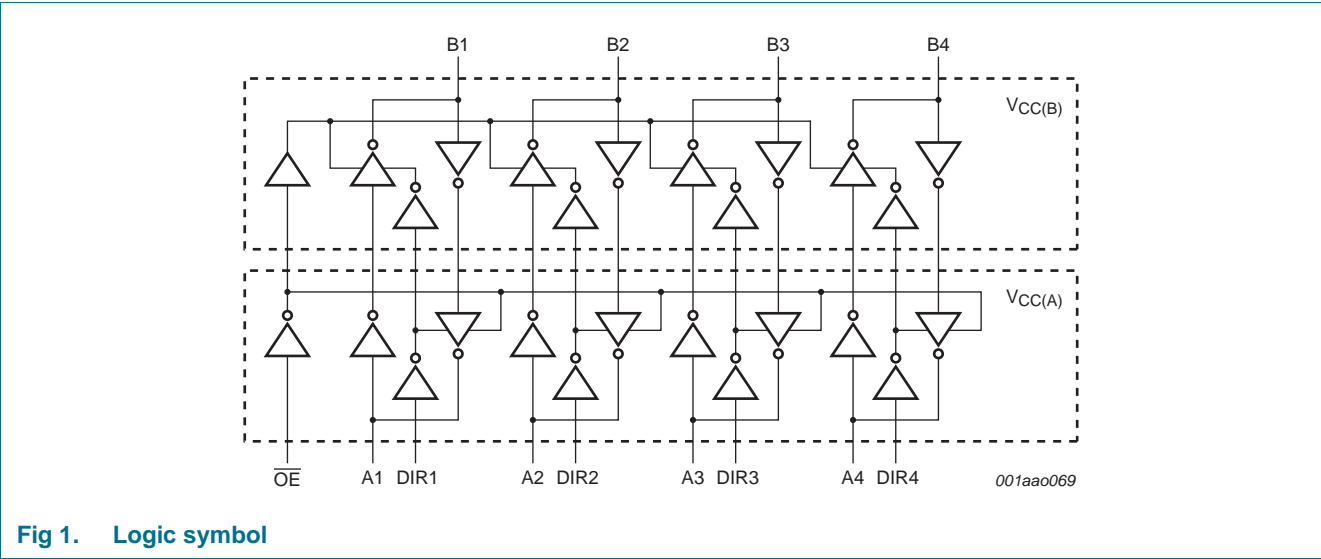
Type number	Package			
	Temperature range	Name	Description	Version
74AVC4TD245PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AVC4TD245BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AVC4TD245GU	−40 °C to +125 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm	SOT1161-1

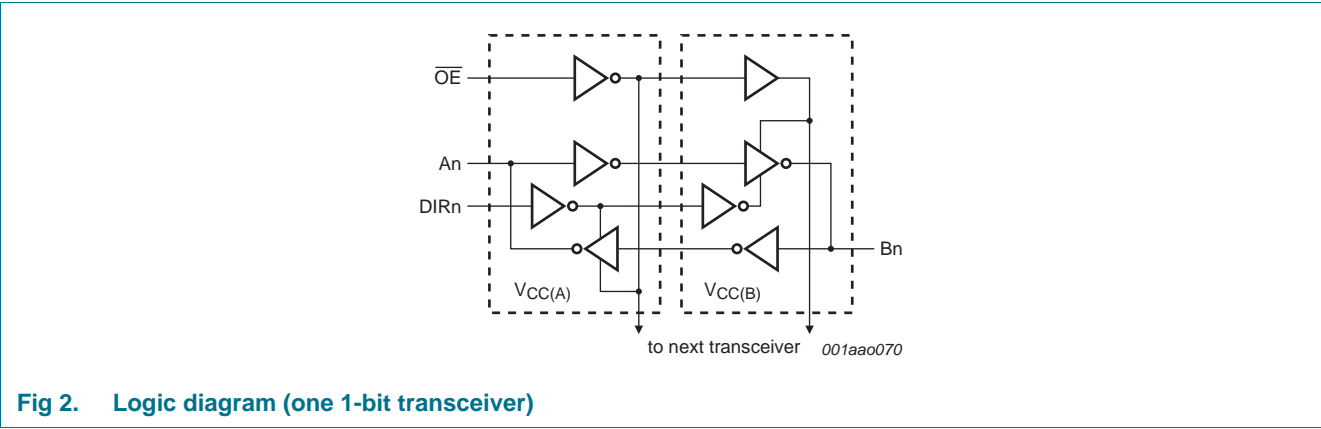
4. Marking

Table 2. Marking codes

Type number	Marking code
74AVC4TD245PW	C4TD245
74AVC4TD245BQ	4TD245
74AVC4TD245GU	BD4

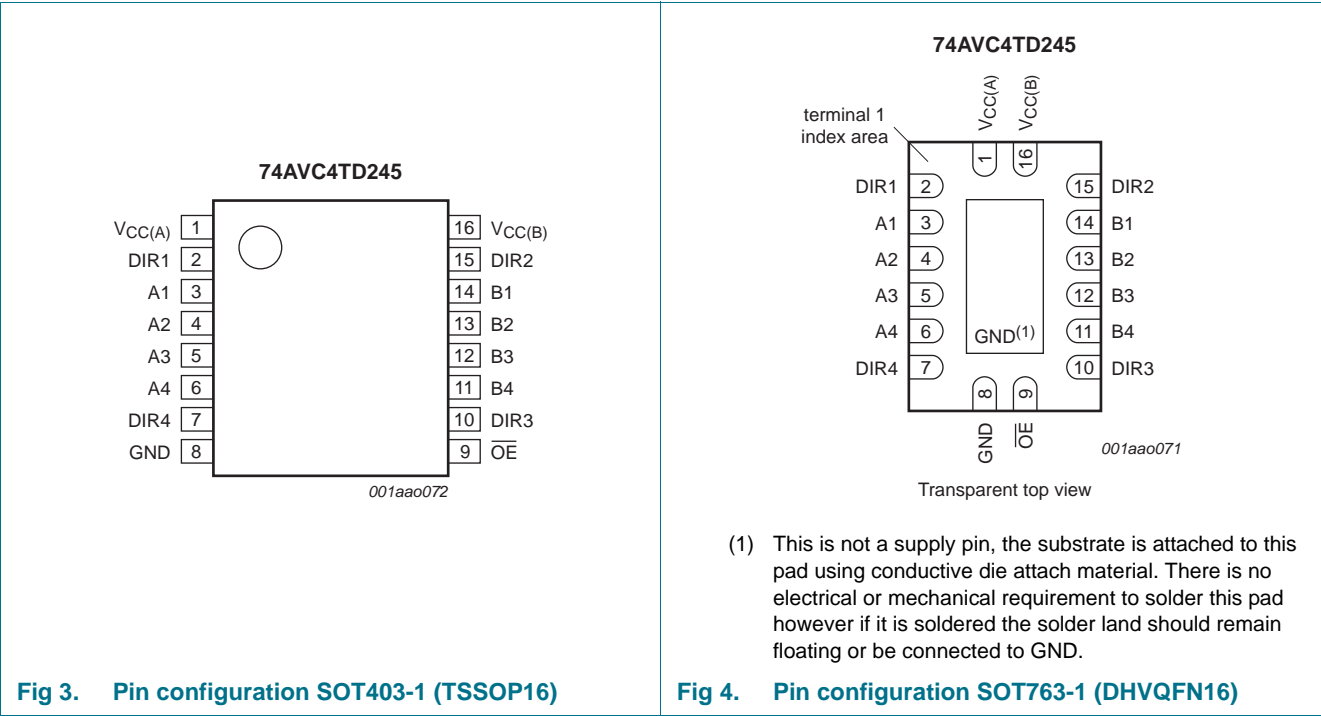
5. Functional diagram

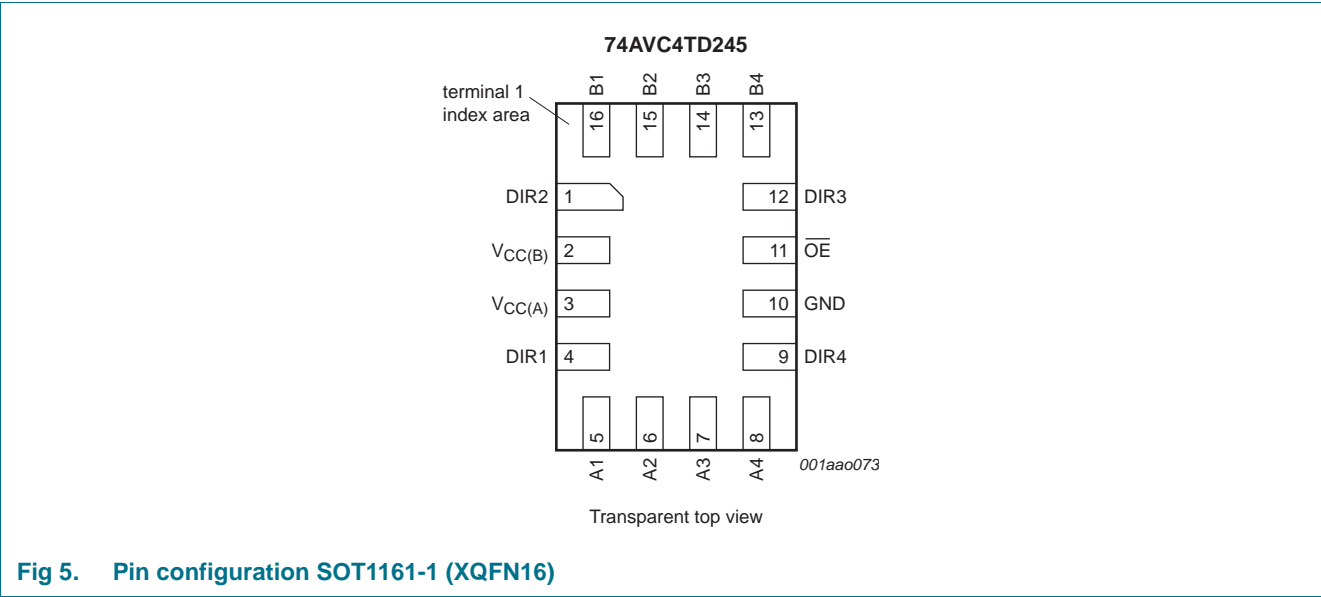




6. Pinning information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT403-1 and SOT763-1	SOT1161-1	
V _{CC(A)}	1	3	supply voltage A (An, \overline{OE} and DIRn inputs are referenced to V _{CC(A)})
DIR1, DIR2, DIR3, DIR4	2, 15, 10, 7	4, 1, 12, 9	direction control input
A1, A2, A3, A4	3, 4, 5, 6	5, 6, 7, 8	data input or output
GND	8	10	ground (0 V)
B1, B2, B3, B4	14, 13, 12, 11	16, 15, 14, 13	data input or output
\overline{OE}	9	11	output enable input (active LOW)
V _{CC(B)}	16	2	supply voltage B (Bn pins are referenced to V _{CC(B)})

7. Functional description

Table 4. Function table^{[1][2]}

Supply voltage	Input					Input/output	
$V_{CC(A)}, V_{CC(B)}$	\overline{OE}	DIR1	DIR2	DIR3	DIR4	An	Bn
0.8 V to 3.6 V	L	L	X	X	X	A1 = B1	input B1
0.8 V to 3.6 V	L	H	X	X	X	input A1	B1 = A1
0.8 V to 3.6 V	L	X	L	X	X	A2 = B2	input B2
0.8 V to 3.6 V	L	X	H	X	X	input A2	B2 = A2
0.8 V to 3.6 V	L	X	X	L	X	A3 = B3	input B3
0.8 V to 3.6 V	L	X	X	H	X	input A3	B3 = A3
0.8 V to 3.6 V	L	X	X	X	L	A4 = B4	input B4
0.8 V to 3.6 V	L	X	X	X	H	input A4	B4 = A4
0.8 V to 3.6 V	H	X	X	X	X	Z	Z
GND ^[3]	X	X	X	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The An, DIRn and \overline{OE} input circuit is referenced to $V_{CC(A)}$; The Bn input circuit is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		^[1] -0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode	^{[1][2][3]} -0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	^[1] -0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CCO}	^[2] -	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C

Table 5. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		TSSOP16 and DHVQFN16	[4] -	500	mW
		XQFN16	[4] -	250	mW

- [1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] V_{CCO} is the supply voltage associated with the output port.
- [3] V_{CCO} + 0.5 V should not exceed 4.6 V.
- [4] For TSSOP16 package: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
 For DHVQFN16 package: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.
 For XQFN16 package: above 133 °C the value of P_{tot} derates linearly with 14.5 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC(A)}	supply voltage A		0.8	3.6	V
V _{CC(B)}	supply voltage B		0.8	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	Active mode	[1] 0	V _{CCO}	V
		Suspend or 3-state mode	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CCI} = 0.8 V to 3.6 V	[2] -	10	ns/V

- [1] V_{CCO} is the supply voltage associated with the output port.
- [2] V_{CCI} is the supply voltage associated with the input port.

10. Static characteristics

Table 7. Typical static characteristics at T_{amb} = 25 °C [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -1.5 mA; V _{CC(A)} = V _{CC(B)} = 0.8 V	-	0.69	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 1.5 mA; V _{CC(A)} = V _{CC(B)} = 0.8 V	-	0.07	-	V
I _I	input leakage current	DIRn, OE input; V _I = 0 V or 3.6 V; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	±0.025	±0.25	μA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 3.6 V	[3] -	±0.5	±2.5	μA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V	[3] -	±0.5	±2.5	μA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V	[3] -	±0.5	±2.5	μA

Table 7. Typical static characteristics at $T_{amb} = 25\text{ }^{\circ}\text{C}$ [1][2] ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC(A)} = 0\text{ V}$; $V_{CC(B)} = 0.8\text{ V}$ to 3.6 V	-	± 0.1	± 1	μA
		B port; V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC(B)} = 0\text{ V}$; $V_{CC(A)} = 0.8\text{ V}$ to 3.6 V	-	± 0.1	± 1	μA
C_I	input capacitance	DIRn, \overline{OE} input; $V_I = 0\text{ V}$ or 3.3 V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V}$ or 0 V ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	4.0	-	pF

[1] V_{CCO} is the supply voltage associated with the output port.[2] V_{CCI} is the supply voltage associated with the data input port.[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.**Table 8.** Static characteristics [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	$0.70V_{CCI}$	-	$0.70V_{CCI}$	-	V
		$V_{CCI} = 1.1\text{ V}$ to 1.95 V	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		$V_{CCI} = 2.3\text{ V}$ to 2.7 V	1.6	-	1.6	-	V
		$V_{CCI} = 3.0\text{ V}$ to 3.6 V	2	-	2	-	V
		DIRn, \overline{OE} input					
		$V_{CC(A)} = 0.8\text{ V}$	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)} = 1.1\text{ V}$ to 1.95 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)} = 2.3\text{ V}$ to 2.7 V	1.6	-	1.6	-	V
		$V_{CC(A)} = 3.0\text{ V}$ to 3.6 V	2	-	2	-	V
V_{IL}	LOW-level input voltage	data input					
		$V_{CCI} = 0.8\text{ V}$	-	$0.30V_{CCI}$	-	$0.30V_{CCI}$	V
		$V_{CCI} = 1.1\text{ V}$ to 1.95 V	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		$V_{CCI} = 2.3\text{ V}$ to 2.7 V	-	0.7	-	0.7	V
		$V_{CCI} = 3.0\text{ V}$ to 3.6 V	-	0.8	-	0.8	V
		DIRn, \overline{OE} input					
		$V_{CC(A)} = 0.8\text{ V}$	-	$0.30V_{CC(A)}$	-	$0.30V_{CC(A)}$	V
		$V_{CC(A)} = 1.1\text{ V}$ to 1.95 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)} = 2.3\text{ V}$ to 2.7 V	-	0.7	-	0.7	V
		$V_{CC(A)} = 3.0\text{ V}$ to 3.6 V	-	0.8	-	0.8	V

Table 8. Static characteristics ...continued [\[1\]\[2\]](#)

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = –100 µA; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	V _{CCO} – 0.1	-	V _{CCO} – 0.1	-	V
		I _O = –3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	0.85	-	0.85	-	V
		I _O = –6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	1.05	-	1.05	-	V
		I _O = –8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	1.2	-	1.2	-	V
		I _O = –9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	1.75	-	1.75	-	V
		I _O = –12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	2.3	-	2.3	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}					
		I _O = 100 µA; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I _O = 3 mA; V _{CC(A)} = V _{CC(B)} = 1.1 V	-	0.25	-	0.25	V
		I _O = 6 mA; V _{CC(A)} = V _{CC(B)} = 1.4 V	-	0.35	-	0.35	V
		I _O = 8 mA; V _{CC(A)} = V _{CC(B)} = 1.65 V	-	0.45	-	0.45	V
		I _O = 9 mA; V _{CC(A)} = V _{CC(B)} = 2.3 V	-	0.55	-	0.55	V
		I _O = 12 mA; V _{CC(A)} = V _{CC(B)} = 3.0 V	-	0.7	-	0.7	V
I _I	input leakage current	DIRn, $\overline{\text{OE}}$ input; V _I = 0 V or 3.6 V; V _{CC(A)} = V _{CC(B)} = 0.8 V to 3.6 V	-	±1	-	±5	µA
I _{OZ}	OFF-state output current	A or B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = V _{CC(B)} = 3.6 V [3]	-	±5	-	±30	µA
		suspend mode A port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 3.6 V; V _{CC(B)} = 0 V [3]	-	±5	-	±30	µA
		suspend mode B port; V _O = 0 V or V _{CCO} ; V _{CC(A)} = 0 V; V _{CC(B)} = 3.6 V [3]	-	±5	-	±30	µA
I _{OFF}	power-off leakage current	A port; V _I or V _O = 0 V to 3.6 V; V _{CC(A)} = 0 V; V _{CC(B)} = 0.8 V to 3.6 V	-	±5	-	±30	µA
		B port; V _I or V _O = 0 V to 3.6 V; V _{CC(B)} = 0 V; V _{CC(A)} = 0.8 V to 3.6 V	-	±5	-	±30	µA

Table 8. Static characteristics ...continued^{[1][2]}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	A port; $V_I = 0$ V or V_{CCI} ; $I_O = 0$ A					
		$V_{CC(A)} = 0.8$ V to 3.6 V; $V_{CC(B)} = 0.8$ V to 3.6 V	-	10	-	55	μ A
		$V_{CC(A)} = 1.1$ V to 3.6 V; $V_{CC(B)} = 1.1$ V to 3.6 V	-	8	-	50	μ A
		$V_{CC(A)} = 3.6$ V; $V_{CC(B)} = 0$ V	-	8	-	50	μ A
		$V_{CC(A)} = 0$ V; $V_{CC(B)} = 3.6$ V	-2	-	-12	-	μ A
		B port; $V_I = 0$ V or V_{CCI} ; $I_O = 0$ A					
		$V_{CC(A)} = 0.8$ V to 3.6 V; $V_{CC(B)} = 0.8$ V to 3.6 V	-	10	-	55	μ A
		$V_{CC(A)} = 1.1$ V to 3.6 V; $V_{CC(B)} = 1.1$ V to 3.6 V	-	8	-	50	μ A
		$V_{CC(A)} = 3.6$ V; $V_{CC(B)} = 0$ V	-2	-	-12	-	μ A
		$V_{CC(A)} = 0$ V; $V_{CC(B)} = 3.6$ V	-	8	-	50	μ A
		A plus B port ($I_{CC(A)} + I_{CC(B)}$); $I_O = 0$ A; $V_I = 0$ V or V_{CCI} ; $V_{CC(A)} = 0.8$ V to 3.6 V; $V_{CC(B)} = 0.8$ V to 3.6 V	-	20	-	70	μ A
ΔI_{CC}	additional supply current	A plus B port ($I_{CC(A)} + I_{CC(B)}$); $I_O = 0$ A; $V_I = 0$ V or V_{CCI} ; $V_{CC(A)} = 1.1$ V to 3.6 V; $V_{CC(B)} = 1.1$ V to 3.6 V	-	16	-	65	μ A
		$V_I = 3.0$ V; $V_{CC(A)} = V_{CC(B)} = 3.6$ V	-	500	-	650	μ A

[1] V_{CCO} is the supply voltage associated with the output port.[2] V_{CCI} is the supply voltage associated with the data input port.[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.**Table 9.** Typical total supply current ($I_{CC(A)} + I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μ A
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μ A
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μ A
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μ A
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μ A
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μ A
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μ A

11. Dynamic characteristics

Table 10. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\text{ °C}$ [1][2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction An to Bn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction An to Bn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction Bn to An); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction Bn to An); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction An to Bn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction An to Bn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction Bn to An); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction Bn to An); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] $f_i = 10\text{ MHz}$; $V_i = \text{GND to } V_{CC}$; $t_r = t_f = 1\text{ ns}$; $C_L = 0\text{ pF}$; $R_L = \infty\text{ }\Omega$.

Table 11. Typical dynamic characteristics at $V_{CC(A)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$ [1]Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	An to Bn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		Bn to An	14.5	12.7	12.4	12.3	12.1	12.0	ns
t_{dis}	disable time	\overline{OE} to An	14.3	14.3	14.3	14.3	14.3	14.3	ns
		\overline{OE} to Bn	17.0	9.9	9.0	9.4	9.0	9.7	ns
t_{en}	enable time	\overline{OE} to An	18.2	18.2	18.2	18.2	18.2	18.2	ns
		\overline{OE} to Bn	19.2	10.7	9.8	9.6	9.7	10.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .**Table 12. Typical dynamic characteristics at $V_{CC(B)} = 0.8\text{ V}$ and $T_{amb} = 25\text{ °C}$ [1]**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	An to Bn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		Bn to An	14.5	7.3	6.5	6.2	5.9	6.0	ns
t_{dis}	disable time	\overline{OE} to An	14.3	5.5	4.1	4.0	3.0	3.5	ns
		\overline{OE} to Bn	17.0	13.8	13.4	13.1	12.9	12.7	ns
t_{en}	enable time	\overline{OE} to An	18.2	5.6	4.0	3.2	2.4	2.2	ns
		\overline{OE} to Bn	19.2	14.6	14.1	13.9	13.7	13.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL} ; t_{dis} is the same as t_{PLZ} and t_{PHZ} ; t_{en} is the same as t_{PZL} and t_{PZH} .

Table 13. Dynamic characteristics for temperature range –40 °C to +85 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#).

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	An to Bn	2.0	10.5	1.3	7.8	1.2	6.9	1.0	5.9	0.8	5.7	ns
		Bn to An	2.0	10.5	1.5	9.9	1.5	9.7	1.4	9.4	1.4	9.3	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	2.0	10.0	ns
		$\overline{\text{OE}}$ to Bn	2.0	11.1	2.0	8.6	1.0	8.0	0.7	7.0	1.0	8.0	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	2.0	13.5	ns
		$\overline{\text{OE}}$ to Bn	2.0	15.0	2.0	11.0	2.0	9.4	1.0	7.8	1.0	7.4	ns
V _{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	An to Bn	1.5	9.9	1.0	7.1	1.0	6.0	0.5	4.8	0.5	4.3	ns
		Bn to An	1.3	7.8	1.0	7.1	0.9	6.9	0.8	6.6	0.6	6.5	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	1.0	6.0	ns
		$\overline{\text{OE}}$ to Bn	2.0	10.2	1.5	7.5	0.9	7.2	0.4	6.2	0.4	6.1	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{\text{OE}}$ to Bn	2.0	14.4	1.4	7.9	1.3	7.7	1.1	6.4	1.1	5.6	ns
V _{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	An to Bn	1.5	9.7	0.9	6.9	0.8	5.7	0.5	4.5	0.3	4.0	ns
		Bn to An	1.2	6.9	1.0	6.0	0.8	5.7	0.5	5.5	0.5	5.3	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{\text{OE}}$ to Bn	2.0	9.9	1.5	7.0	0.8	6.9	0.2	5.8	0.2	5.9	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	1.0	6.7	ns
		$\overline{\text{OE}}$ to Bn	1.5	13.9	1.2	7.2	1.2	6.9	0.8	5.4	0.6	5.0	ns
V _{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	An to Bn	1.4	9.4	0.8	6.6	0.5	5.5	0.4	4.2	0.2	3.7	ns
		Bn to An	1.0	5.9	0.5	4.8	0.5	4.5	0.4	4.2	0.3	3.9	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	ns
		$\overline{\text{OE}}$ to Bn	2.0	9.3	1.5	6.7	0.7	6.3	0.2	5.0	0.2	5.7	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	0.6	4.5	ns
		$\overline{\text{OE}}$ to Bn	1.5	13.6	1.0	6.8	1.0	6.0	0.8	4.6	0.6	4.2	ns
V _{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	An to Bn	1.4	9.3	0.6	6.5	0.5	5.3	0.3	3.9	0.2	3.5	ns
		Bn to An	0.8	5.7	0.5	4.3	0.3	4.0	0.2	3.7	0.2	3.5	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	0.2	4.5	ns
		$\overline{\text{OE}}$ to Bn	2.0	9.0	1.5	6.4	0.7	6.1	0.2	4.8	0.2	5.6	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{\text{OE}}$ to Bn	1.5	13.4	1.0	6.7	1.0	5.9	0.7	4.4	0.5	4.0	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

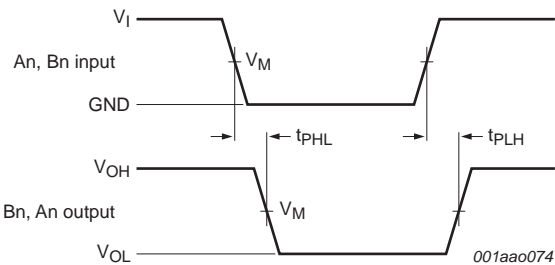
Table 14. Dynamic characteristics for temperature range –40 °C to +125 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 8](#); for wave forms see [Figure 6](#) and [Figure 7](#)

Symbol	Parameter	Conditions	V _{CC(B)}										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V _{CC(A)} = 1.1 V to 1.3 V													
t _{pd}	propagation delay	An to Bn	2.0	12.1	1.3	9.0	1.2	8.0	1.0	6.8	0.8	6.6	ns
		Bn to An	2.0	12.1	1.5	11.4	1.5	11.2	1.4	10.9	1.4	10.7	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	2.0	11.5	ns
		$\overline{\text{OE}}$ to Bn	2.0	12.8	2.0	9.9	1.0	9.2	0.7	8.1	1.0	9.2	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	2.0	15.6	ns
		$\overline{\text{OE}}$ to Bn	2.0	17.3	2.0	12.7	2.0	10.9	1.0	9.0	1.0	8.6	ns
V _{CC(A)} = 1.4 V to 1.6 V													
t _{pd}	propagation delay	An to Bn	1.5	11.4	1.0	8.2	1.0	6.9	0.5	5.6	0.5	5.0	ns
		Bn to An	1.3	9.0	1.0	8.2	0.9	8.0	0.8	7.6	0.6	7.5	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		$\overline{\text{OE}}$ to Bn	2.0	11.8	1.5	8.7	0.9	8.3	0.4	7.2	0.4	7.1	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	1.0	8.7	ns
		$\overline{\text{OE}}$ to Bn	2.0	16.6	1.4	9.1	1.3	8.9	1.1	7.4	1.1	6.5	ns
V _{CC(A)} = 1.65 V to 1.95 V													
t _{pd}	propagation delay	An to Bn	1.5	11.2	0.9	8.0	0.8	6.6	0.5	5.2	0.3	4.6	ns
		Bn to An	1.2	8.0	1.0	6.9	0.8	6.6	0.5	6.4	0.5	6.1	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	0.5	6.6	ns
		$\overline{\text{OE}}$ to Bn	2.0	11.4	1.5	8.1	0.8	8.0	0.2	6.7	0.2	6.8	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	1.0	7.8	ns
		$\overline{\text{OE}}$ to Bn	1.5	16.0	1.2	8.3	1.2	8.0	0.8	6.3	0.6	5.8	ns
V _{CC(A)} = 2.3 V to 2.7 V													
t _{pd}	propagation delay	An to Bn	1.4	10.9	0.8	7.6	0.5	6.4	0.4	4.9	0.2	4.3	ns
		Bn to An	1.0	6.8	0.5	5.6	0.5	5.2	0.4	4.9	0.3	4.5	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	0.2	4.6	ns
		$\overline{\text{OE}}$ to Bn	2.0	10.7	1.5	7.8	0.7	7.3	0.2	5.8	0.2	6.6	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	0.6	5.2	ns
		$\overline{\text{OE}}$ to Bn	1.5	15.7	1.0	7.9	1.0	6.9	0.8	5.3	0.6	4.9	ns
V _{CC(A)} = 3.0 V to 3.6 V													
t _{pd}	propagation delay	An to Bn	1.4	10.7	0.6	7.5	0.5	6.1	0.3	4.5	0.2	4.1	ns
		Bn to An	0.8	6.6	0.5	5.0	0.3	4.6	0.2	4.3	0.2	4.1	ns
t _{dis}	disable time	$\overline{\text{OE}}$ to An	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	0.2	5.2	ns
		$\overline{\text{OE}}$ to Bn	2.0	10.4	1.5	7.4	0.7	7.1	0.2	5.6	0.2	6.5	ns
t _{en}	enable time	$\overline{\text{OE}}$ to An	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	0.5	4.6	ns
		$\overline{\text{OE}}$ to Bn	1.5	15.5	1.0	7.8	1.0	6.8	0.7	5.1	0.5	4.6	ns

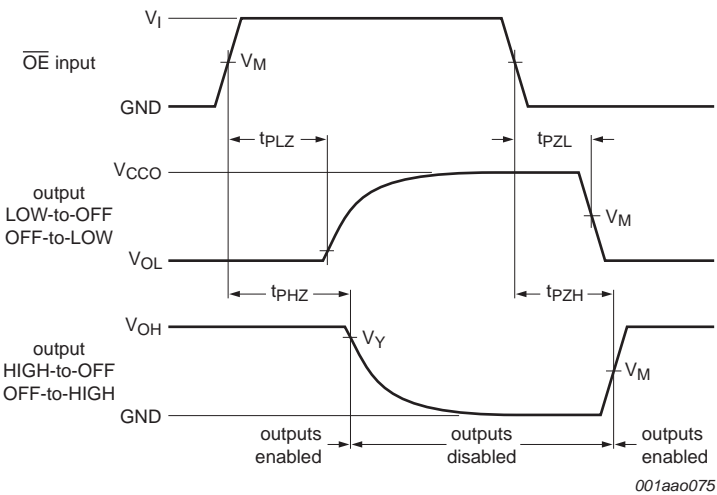
[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

12. Waveforms



Measurement points are given in [Table 15](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The data input (An, Bn) to output (Bn, An) propagation delay times



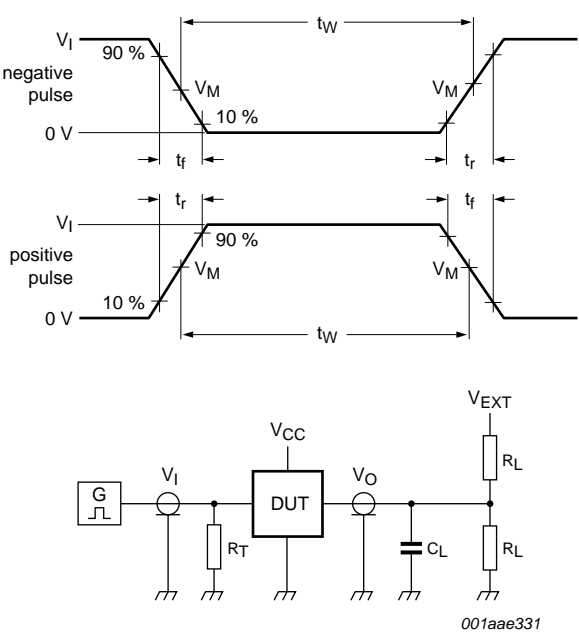
Measurement points are given in [Table 15](#).
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Enable and disable times

Table 15. Measurement points

Supply voltage	Input ^[1]	Output ^[2]		
$V_{CC(A)}, V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1] V_{CCI} is the supply voltage associated with the data input port.
[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in [Table 16](#).
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance.
 V_{EXT} = External voltage for measuring switching times.

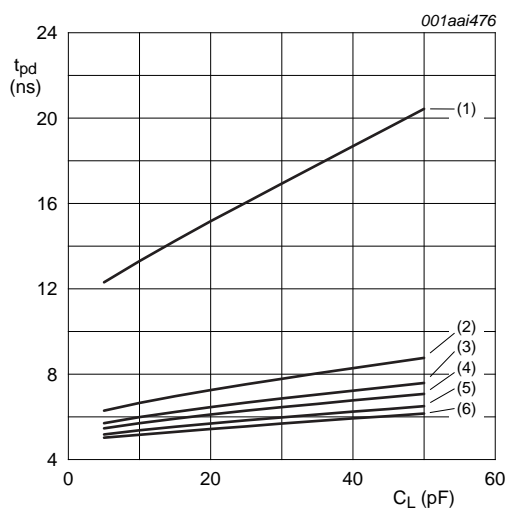
Fig 8. Test circuit for measuring switching times

Table 16. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}, V_{CC(B)}$	V_I ^[1]	$\Delta t/\Delta V$ ^[2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} ^[3]
0.8 V to 1.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	$\leq 1.0 \text{ ns/V}$	15 pF	2 k Ω	open	GND	$2V_{CCO}$

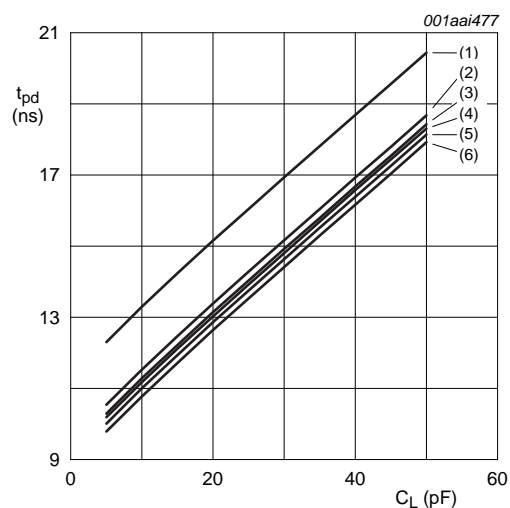
[1] V_{CCI} is the supply voltage associated with the data input port.
[2] $dV/dt \geq 1.0 \text{ V/ns}$
[3] V_{CCO} is the supply voltage associated with the output port.

13. Typical propagation delay characteristics



a. Propagation delay (A to B); $V_{CC(A)} = 0.8 \text{ V}$

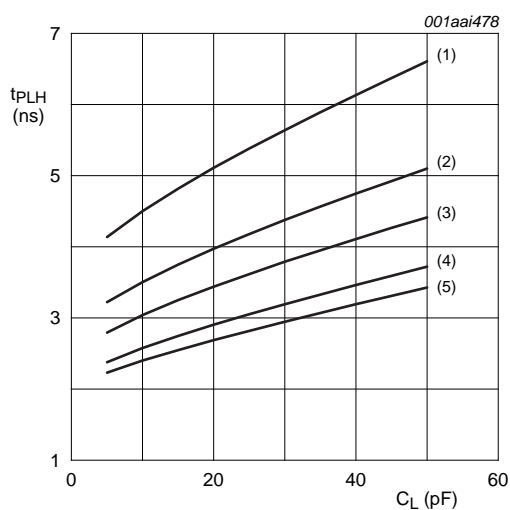
- (1) $V_{CC(B)} = 0.8 \text{ V}$.
- (2) $V_{CC(B)} = 1.2 \text{ V}$.
- (3) $V_{CC(B)} = 1.5 \text{ V}$.
- (4) $V_{CC(B)} = 1.8 \text{ V}$.
- (5) $V_{CC(B)} = 2.5 \text{ V}$.
- (6) $V_{CC(B)} = 3.3 \text{ V}$.



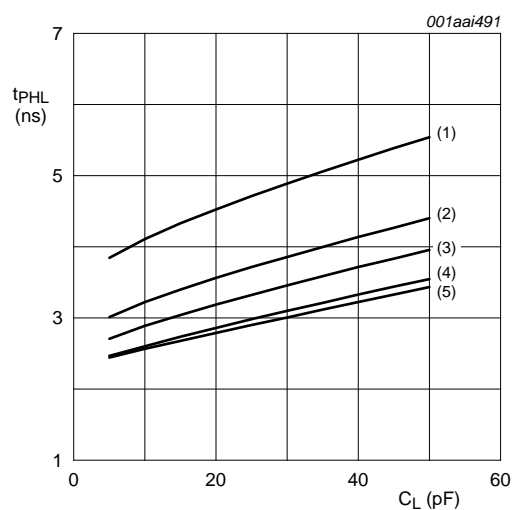
b. Propagation delay (A to B); $V_{CC(B)} = 0.8 \text{ V}$

- (1) $V_{CC(A)} = 0.8 \text{ V}$.
- (2) $V_{CC(A)} = 1.2 \text{ V}$.
- (3) $V_{CC(A)} = 1.5 \text{ V}$.
- (4) $V_{CC(A)} = 1.8 \text{ V}$.
- (5) $V_{CC(A)} = 2.5 \text{ V}$.
- (6) $V_{CC(A)} = 3.3 \text{ V}$.

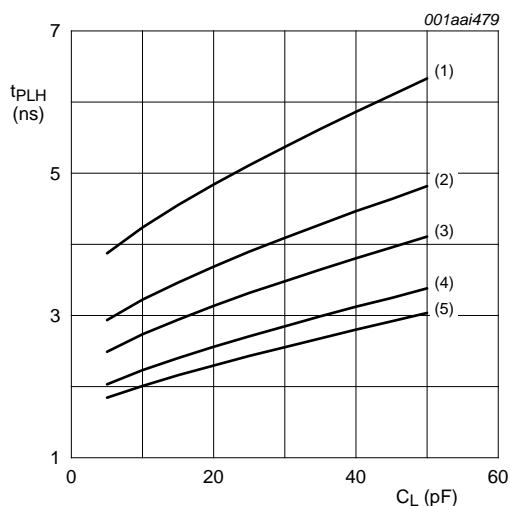
Fig 9. Typical propagation delay versus load capacitance; $T_{amb} = 25 \text{ }^{\circ}\text{C}$



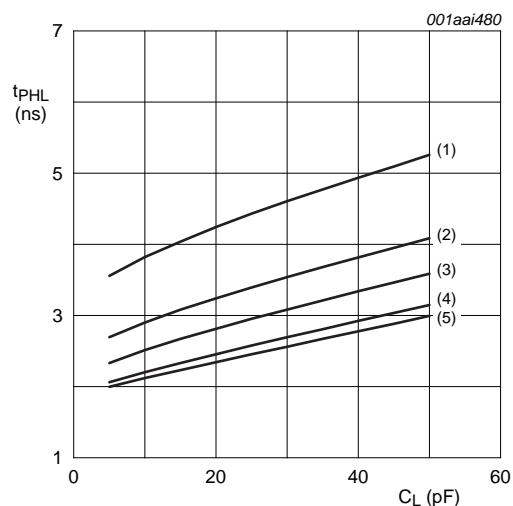
a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.2 \text{ V}$



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.2 \text{ V}$



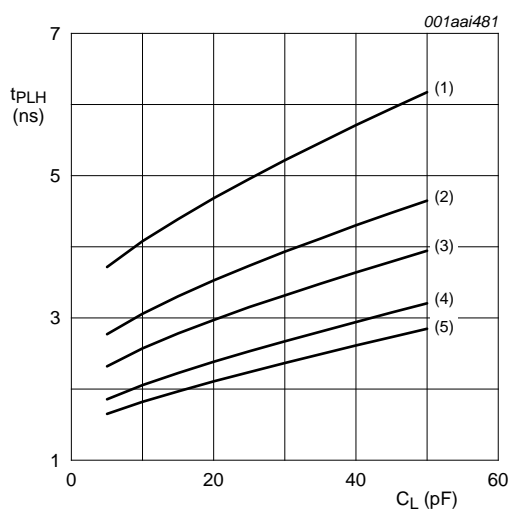
c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.5 \text{ V}$



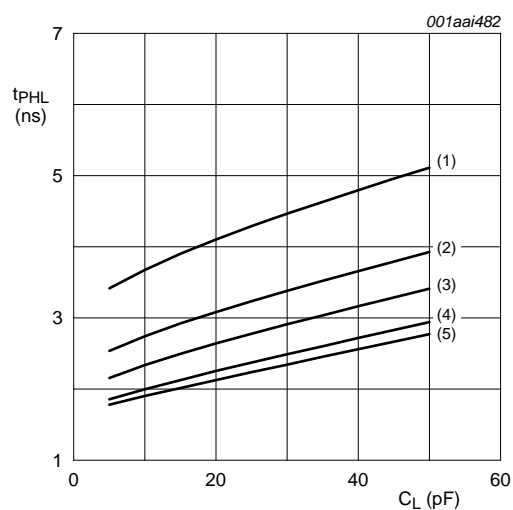
d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.5 \text{ V}$

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.

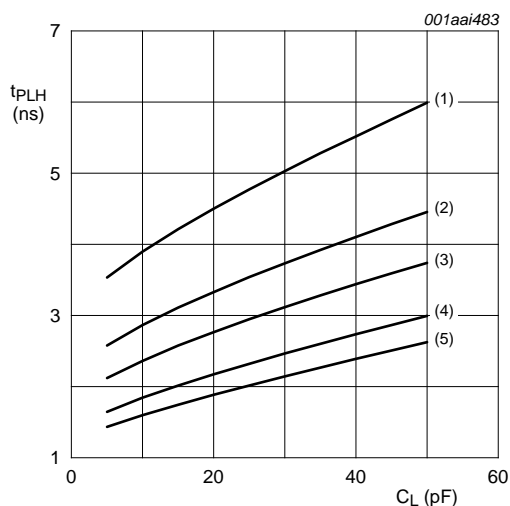
Fig 10. Typical propagation delay versus load capacitance; $T_{amb} = 25 \text{ }^{\circ}\text{C}$



a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 1.8 \text{ V}$

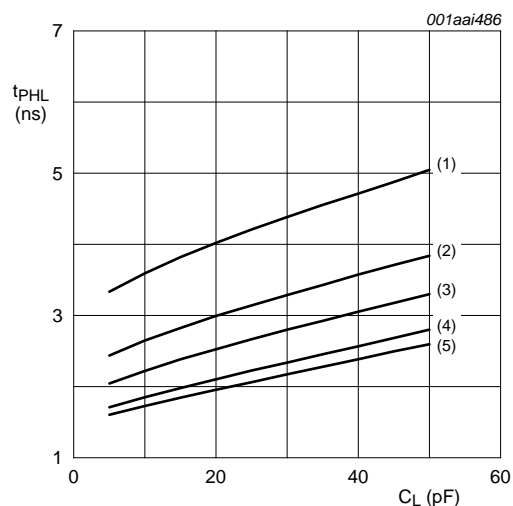


b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 1.8 \text{ V}$



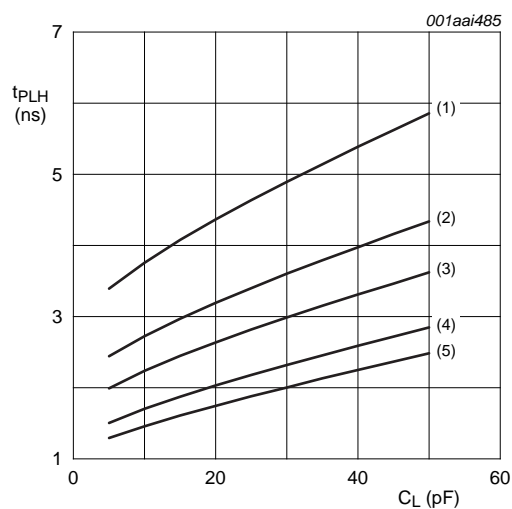
c. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 2.5 \text{ V}$

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.



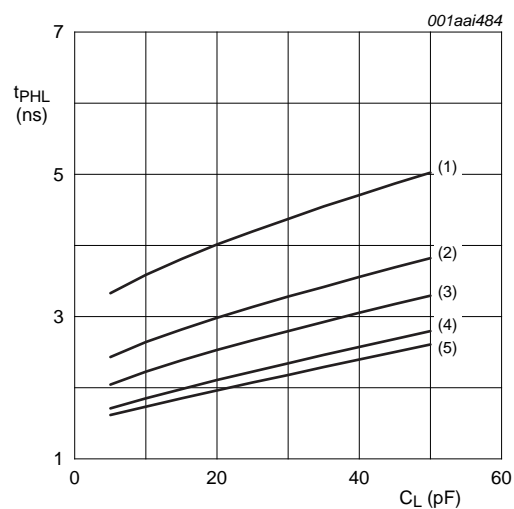
d. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 2.5 \text{ V}$

Fig 11. Typical propagation delay versus load capacitance; $T_{amb} = 25 \text{ }^{\circ}\text{C}$



a. LOW to HIGH propagation delay (A to B);
 $V_{CC(A)} = 3.3 \text{ V}$

- (1) $V_{CC(B)} = 1.2 \text{ V}$.
- (2) $V_{CC(B)} = 1.5 \text{ V}$.
- (3) $V_{CC(B)} = 1.8 \text{ V}$.
- (4) $V_{CC(B)} = 2.5 \text{ V}$.
- (5) $V_{CC(B)} = 3.3 \text{ V}$.



b. HIGH to LOW propagation delay (A to B);
 $V_{CC(A)} = 3.3 \text{ V}$

Fig 12. Typical propagation delay versus load capacitance; $T_{amb} = 25^\circ\text{C}$

14. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

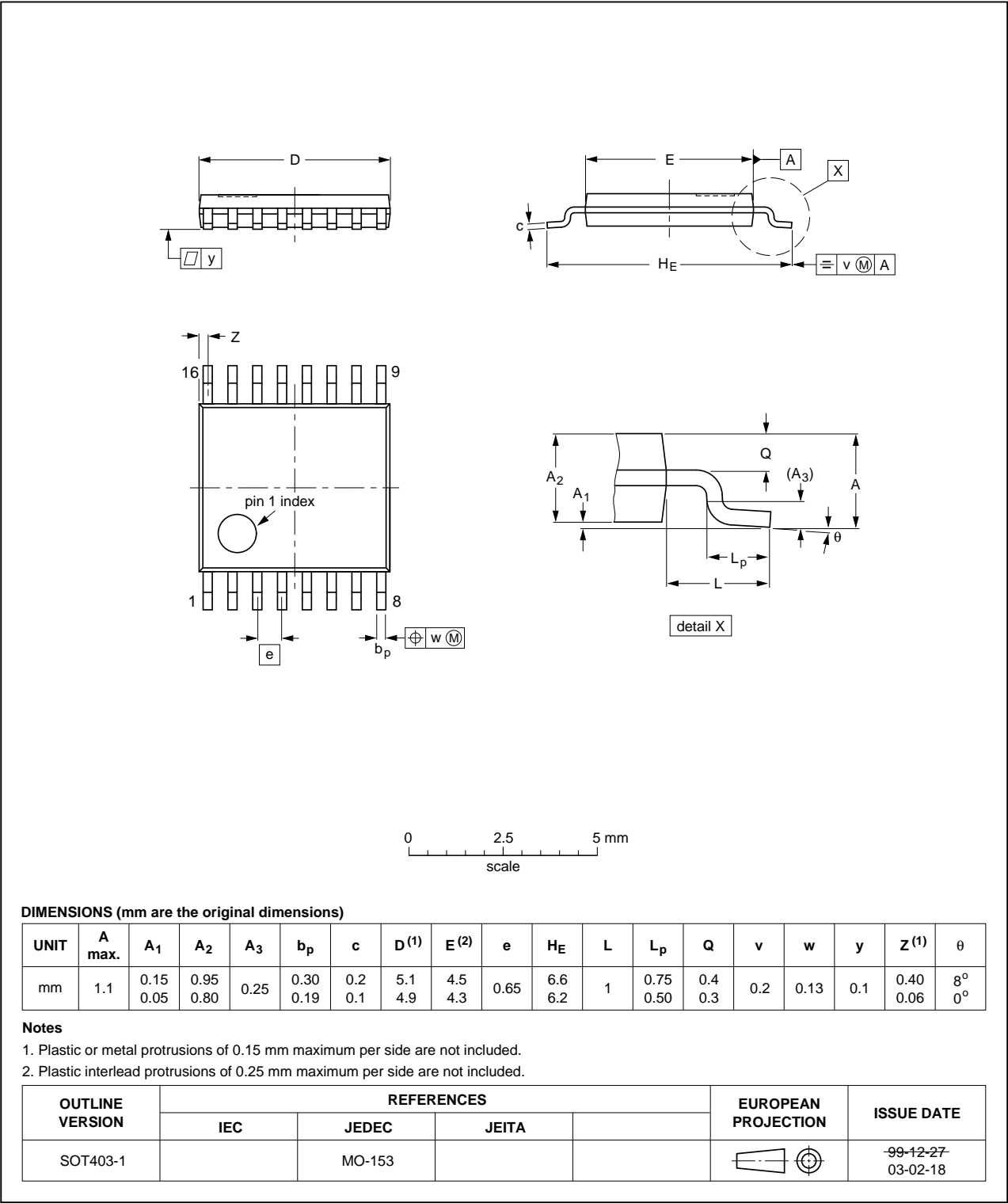


Fig 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

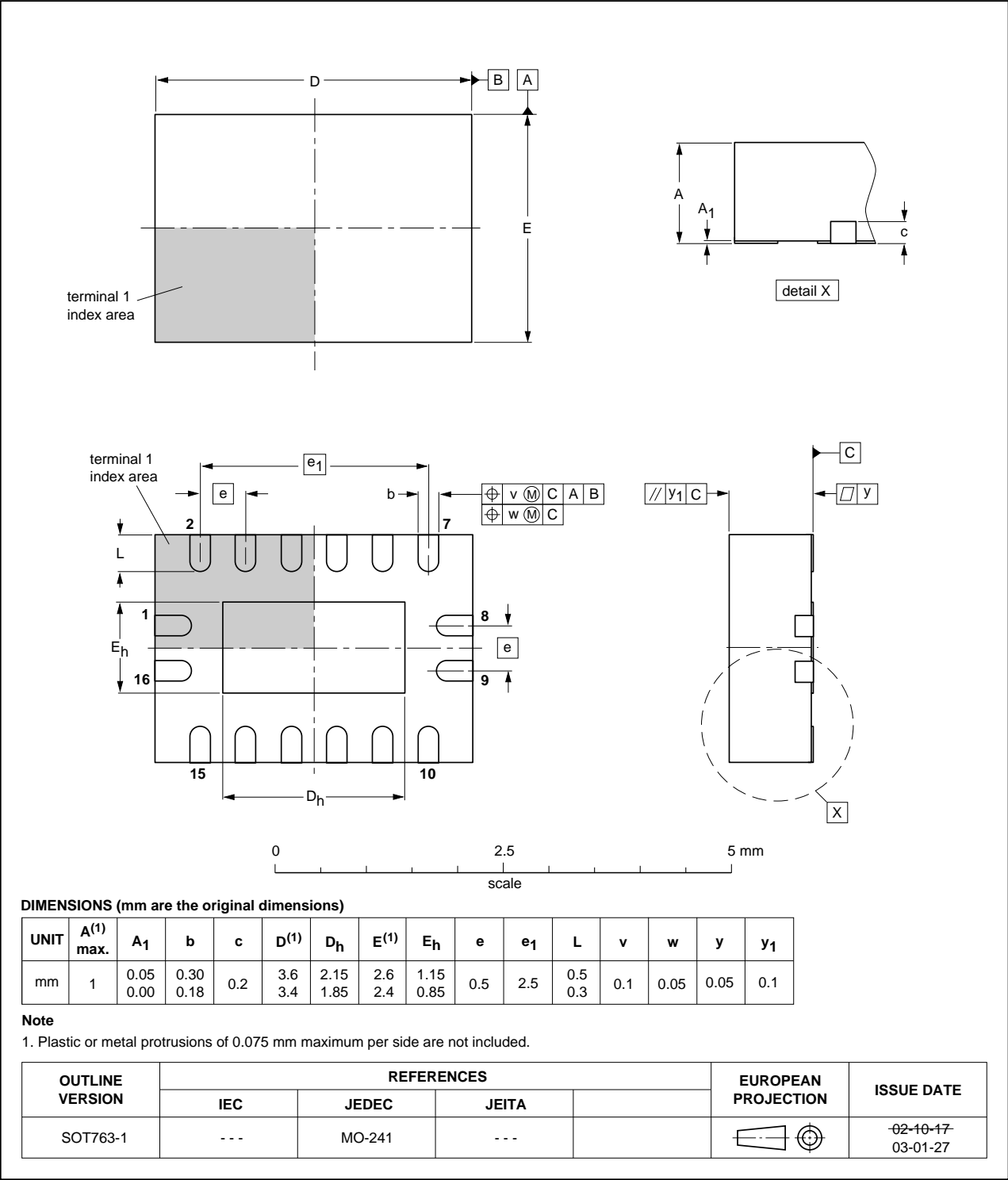


Fig 14. Package outline SOT763-1 (DHVQFN16)

XQFN16: plastic, extremely thin quad flat package; no leads;
16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1

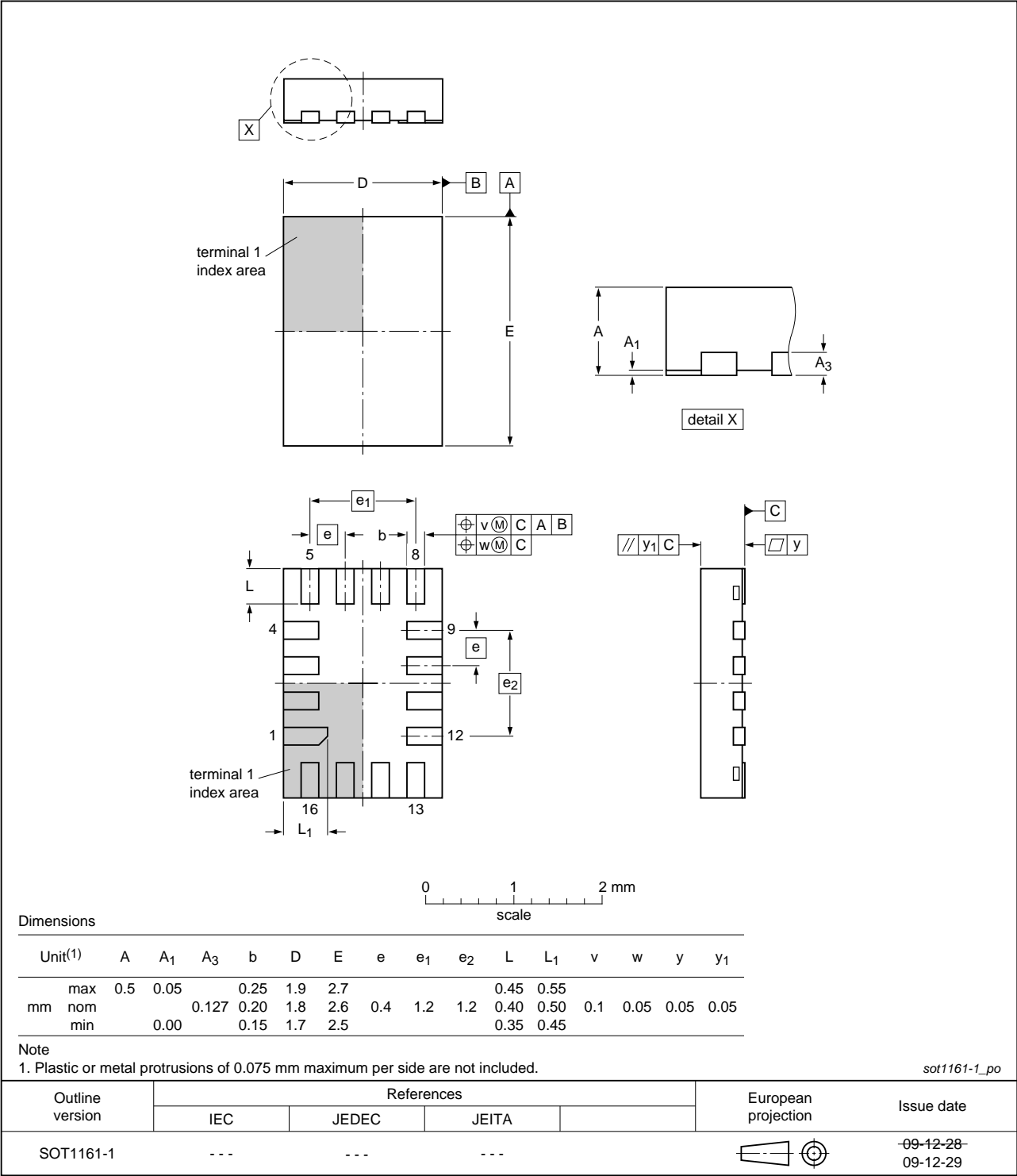


Fig 15. Package outline SOT1161-1 (XQFN16)

15. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC4TD245 v.2	20111209	Product data sheet	-	74AVC4TD245 v.1
Modifications:	• Legal pages updated.			
74AVC4TD245 v.1	20110503	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

19. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Marking	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	4
7	Functional description	5
8	Limiting values	5
9	Recommended operating conditions	6
10	Static characteristics	6
11	Dynamic characteristics	10
12	Waveforms	14
13	Typical propagation delay characteristics ..	16
14	Package outline	20
15	Abbreviations	23
16	Revision history	23
17	Legal information	24
17.1	Data sheet status	24
17.2	Definitions	24
17.3	Disclaimers	24
17.4	Trademarks	25
18	Contact information	25
19	Contents	26

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 December 2011

Document identifier: 74AVC4TD245