BLF2425M7L140; BLF2425M7LS140

Power LDMOS transistor

Rev. 3 — 6 September 2012 Product data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF2425M7L140 and BLF2425M7LS140 are designed for high-power CW applications and are assembled in high performance ceramic packages, available in eared and earless versions

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 1300 mA in a common source class-AB production test circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	28	140	18.5	52

1.2 Features and benefits

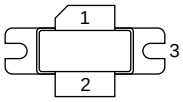
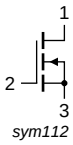
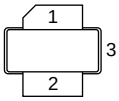
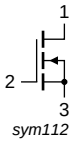
- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications in the frequency range from 2400 MHz to 2500 MHz

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF2425M7L140 (SOT502A)				
1	drain			
2	gate			
3	source	[1]		
BLF2425M7LS140 (SOT502B)				
1	drain			
2	gate			
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF2425M7L140	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF2425M7LS140	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	-	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 125 W	0.28	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.16 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 216 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	41	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	500	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10.8 A	-	16	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.56 A	-	69	-	mΩ

Table 7. RF characteristics

Test signal: CW; f = 2450 MHz; V_{DS} = 28 V; I_{Dq} = 1300 mA; T_{case} = 25 °C unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 140 W	16	18.5	-	dB
RL_{in}	input return loss	P_L = 140 W	-	−16	−8	dB
η_D	drain efficiency	P_L = 140 W	46	52	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF2425M7L140 and BLF2425M7LS140 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1300 mA; P_L = 140 W (CW); f = 2450 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. I_{Dq} = 1300 mA; V_{DS} = 28 V. Z_S and Z_L defined in Figure 1.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
2400	3.7 – 5.4j	1.3 – 1.5j
2450	6.9 – 5.0j	1.5 – 1.6j
2500	8.7 – 2.0j	1.5 – 1.6j

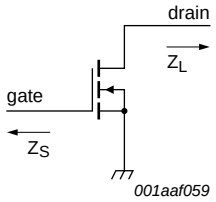
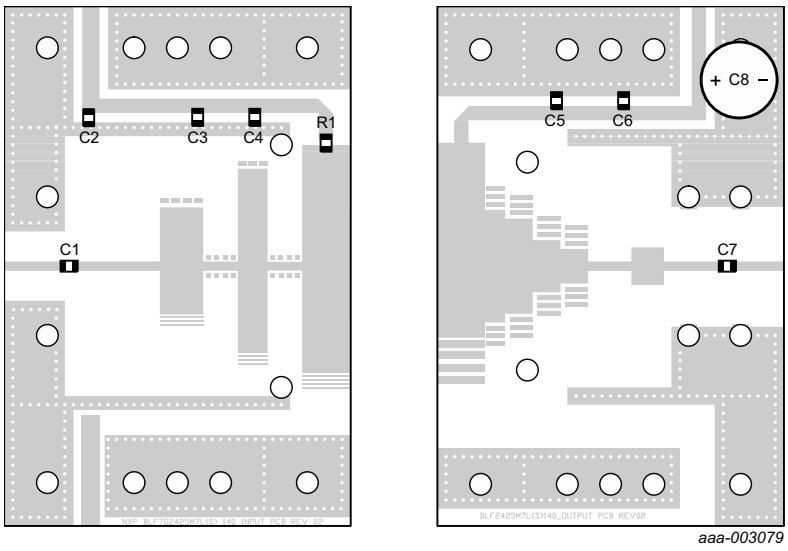


Fig 1. Definition of transistor impedance

7.3 Circuit information



Printed-Circuit Board (PCB): Rogers 4350B; ε_r = 3.5; thickness = 0.508 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

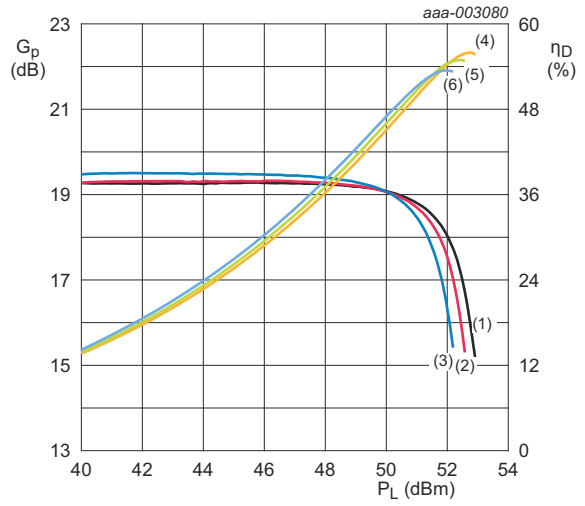
Fig 2. Component layout for application circuit

Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C4, C5	multilayer ceramic chip capacitor	15 pF	ATC100B
C2, C6	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C3	multilayer ceramic chip capacitor	100 nF	Murata
C7	multilayer ceramic chip capacitor	62 pF	ATC100B
C8	electrolytic capacitor	22 μF, 63 V	
R1	resistor	10 Ω	SMD 0805; Bourns

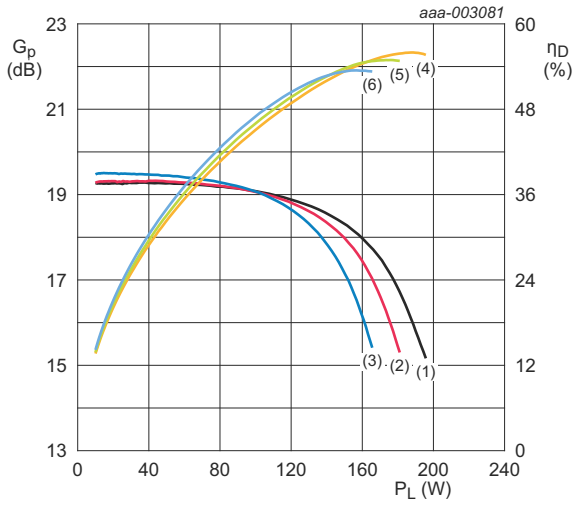
7.4 Graphical data



V_{DS} = 28 V; I_{Dq} = 1300 mA.

(1) G_p at f = 2400 MHz
(2) G_p at f = 2450 MHz
(3) G_p at f = 2500 MHz
(4) η_D at f = 2400 MHz
(5) η_D at f = 2450 MHz
(6) η_D at f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values



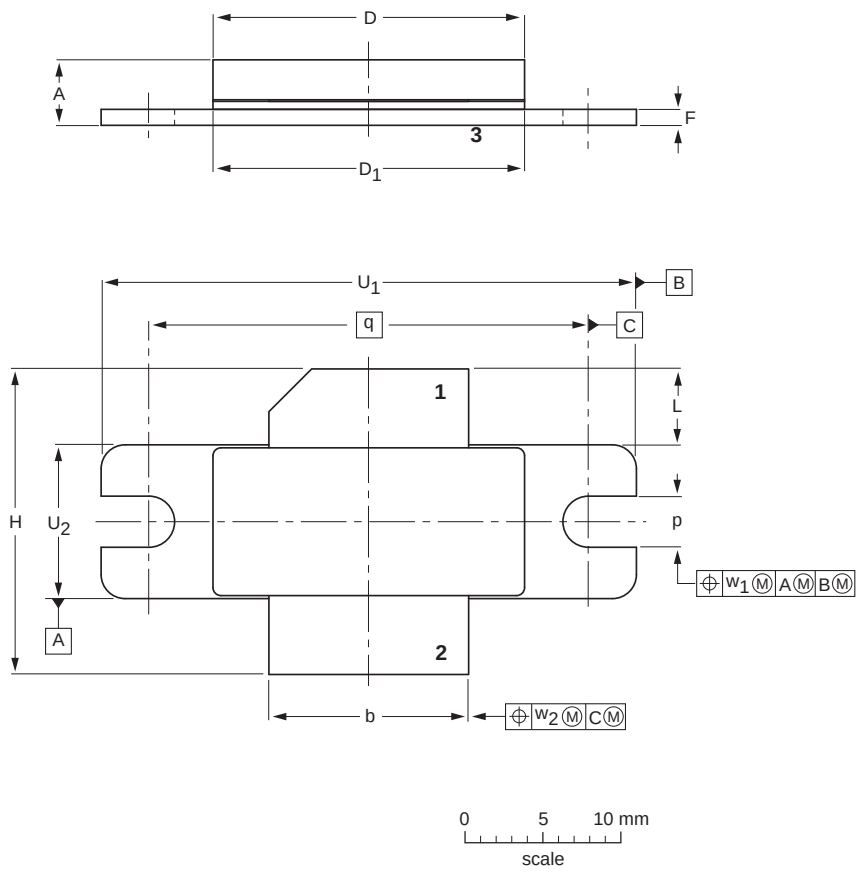
V_{DS} = 28 V; I_{Dq} = 1300 mA.

(1) G_p at f = 2400 MHz
(2) G_p at f = 2450 MHz
(3) G_p at f = 2500 MHz
(4) η_D at f = 2400 MHz
(5) η_D at f = 2450 MHz
(6) η_D at f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of load power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



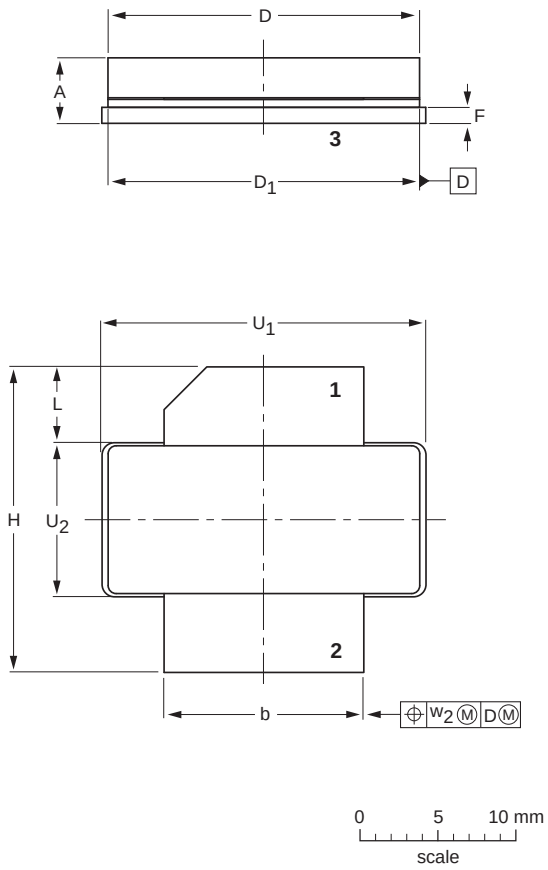
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

Fig 5. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 6. Package outline SOT502B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF2425M7L140_2425M7LS140 v.3	20120906	Product data sheet	-	BLF2425M7L140_2425M7LS140 v.2
Modifications:	• The status of this document has been changed to Product data sheet. • Table 1 on page 1: some changes have been made. • Table 6 on page 3: some changes have been made. • Table 7 on page 3: some changes have been made.			
BLF2425M7L140_2425M7LS140 v.2	20120420	Objective data sheet	-	BLF2425M7L140_2425M7LS140 v.1
BLF2425M7L140_2425M7LS140 v.1	20120130	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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