



BSS138BK

60 V, 360 mA N-channel Trench MOSFET

Rev. 1 — 4 August 2011

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 1.5 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

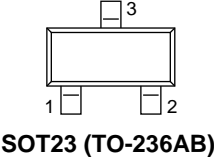
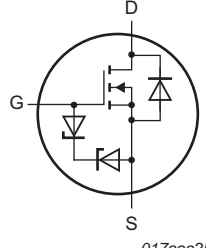
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	[1] -	-	360	mA
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 350\text{ mA}; T_j = 25\text{ }^\circ\text{C}$	-	1	1.6	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT23 (TO-236AB)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BSS138BK	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
BSS138BK	%SB

[1] % = placeholder for manufacturing site code.

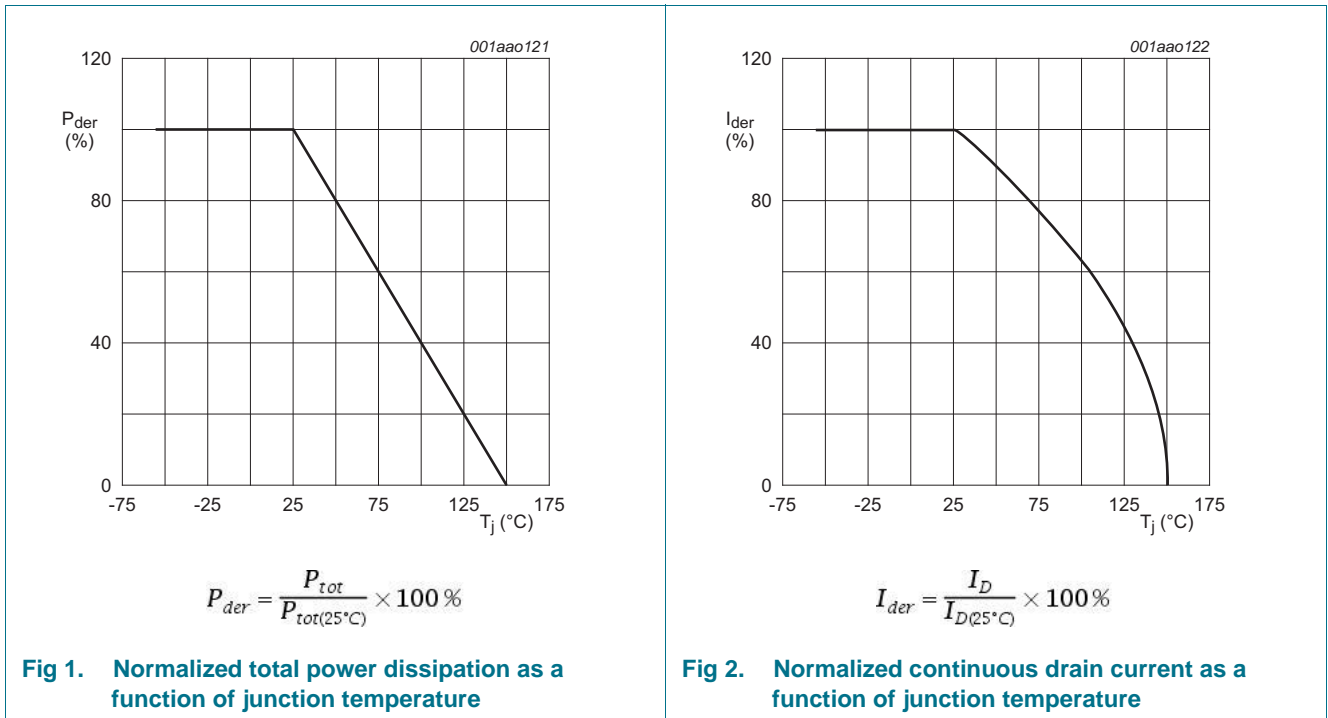
5. Limiting values

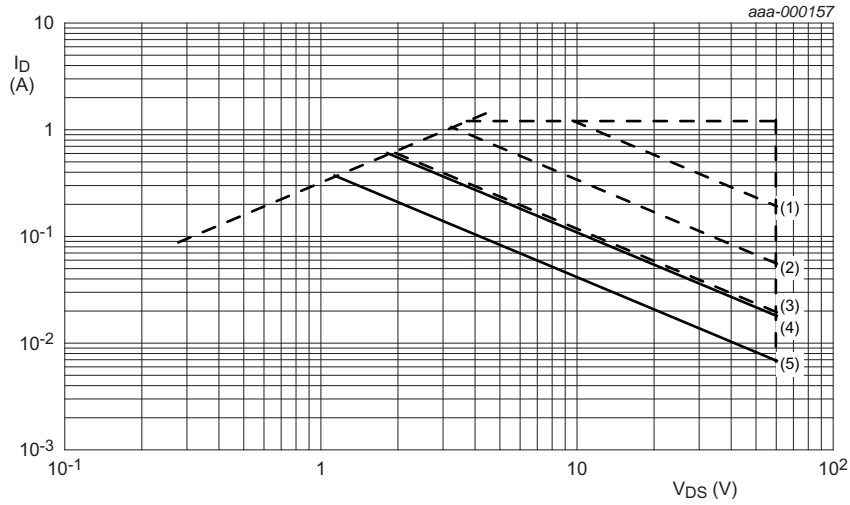
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage	T _j = 25 °C	-	60	V	
V _{GS}	gate-source voltage		-20	20	V	
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	360	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	230	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs	-	1.2	A	
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	350	mW
			[1]	-	420	mW
		T _{sp} = 25 °C	-	-	1140	mW
T _j	junction temperature		-55	150	°C	
T _{amb}	ambient temperature		-55	150	°C	
T _{stg}	storage temperature		-65	150	°C	
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	360	mA
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	1500	V

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





I_{DM} is a single pulse

- (1) $t_p = 1 \text{ ms}$
- (2) $t_p = 10 \text{ ms}$
- (3) $t_p = 100 \text{ ms}$
- (4) DC; $T_{sp} = 25 \text{ }^\circ\text{C}$
- (5) DC; $T_{amb} = 25 \text{ }^\circ\text{C}$; 1 cm^2 drain mounting pad

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

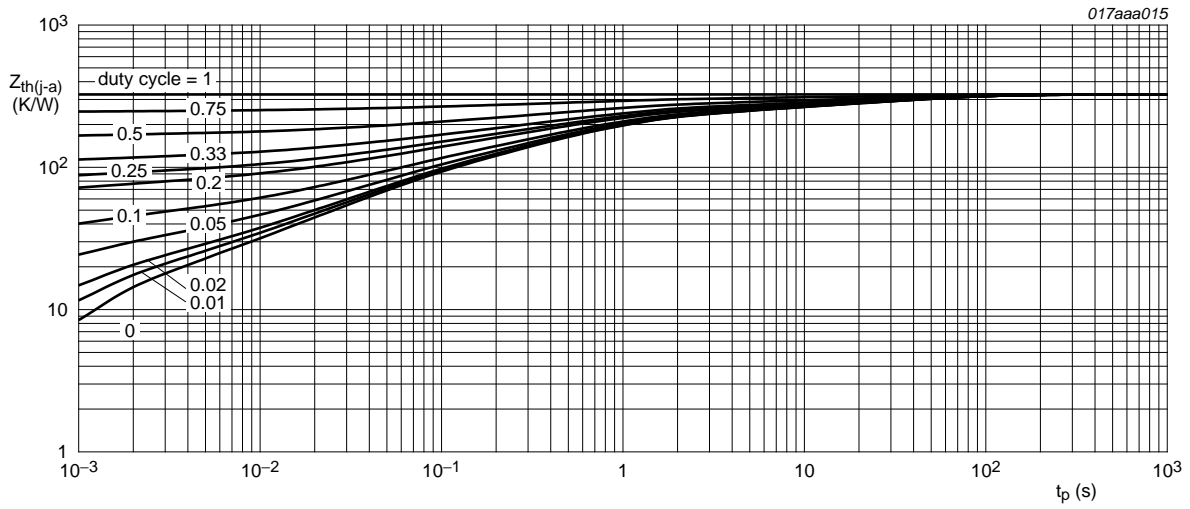
6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	310	370	K/W
			[2]	-	260	300	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	115	K/W	

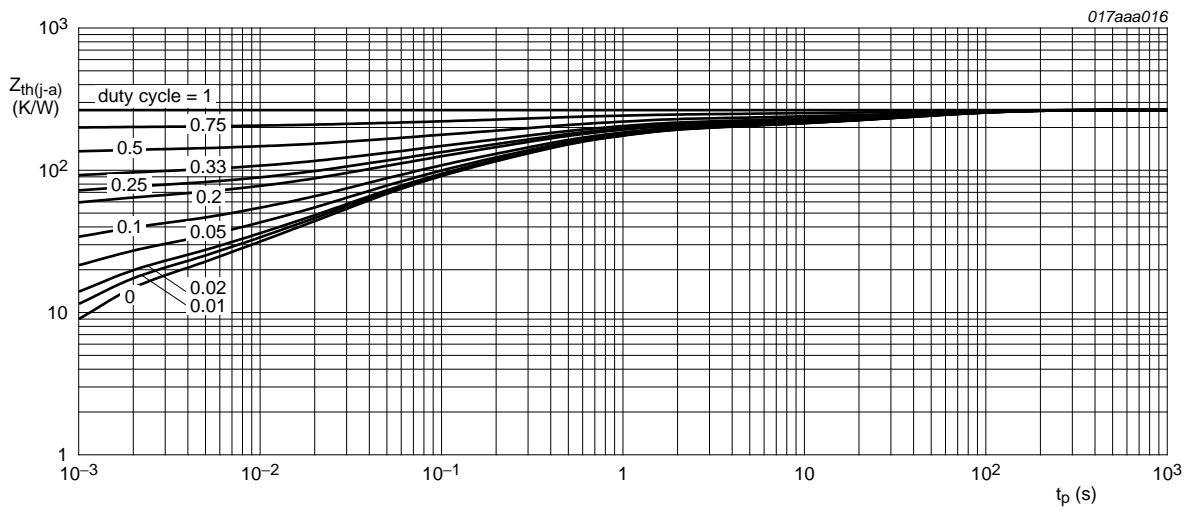
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	0.48	1.1	1.6	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 60 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	10	μA
		$V_{GS} = -20 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	10	μA
		$V_{GS} = 10 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{GS} = -10 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{GS} = 10 \text{ V}$; $I_D = 350 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1	1.6	Ω
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 350 \text{ mA}$; $T_j = 150 \text{ }^\circ\text{C}$	-	2	3.2	Ω
		$V_{GS} = 4.5 \text{ V}$; $I_D = 200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1.1	2.2	Ω
		$V_{GS} = 2.5 \text{ V}$; $I_D = 10 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1.4	6.5	Ω
		$V_{GS} = 10 \text{ V}$; $I_D = 200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	700	-	mS
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}$; $I_D = 200 \text{ mA}$; $T_j = 25 \text{ }^\circ\text{C}$	-	700	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 \text{ V}$; $I_D = 300 \text{ mA}$; $V_{GS} = 4.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.6	0.7	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.2	-	nC
C_{iss}	input capacitance	$V_{DS} = 10 \text{ V}$; $f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	42	56	pF
C_{oss}	output capacitance		-	7	-	pF
C_{rss}	reverse transfer capacitance		-	4	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}$; $R_L = 250 \Omega$; $V_{GS} = 10 \text{ V}$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	5	10	ns
t_r	rise time		-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	38	76	ns
t_f	fall time		-	20	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 300 \text{ mA}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	0.47	0.8	1.2	V

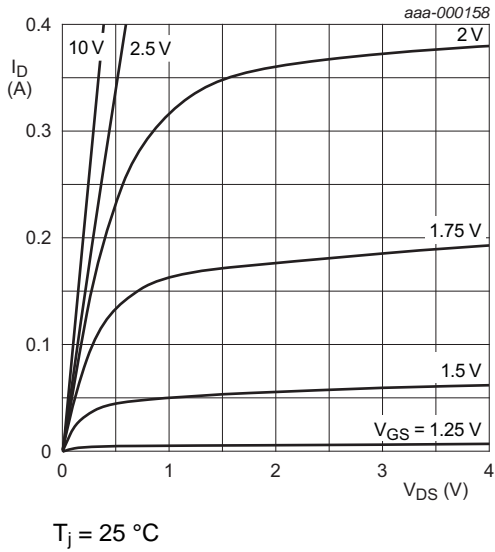


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

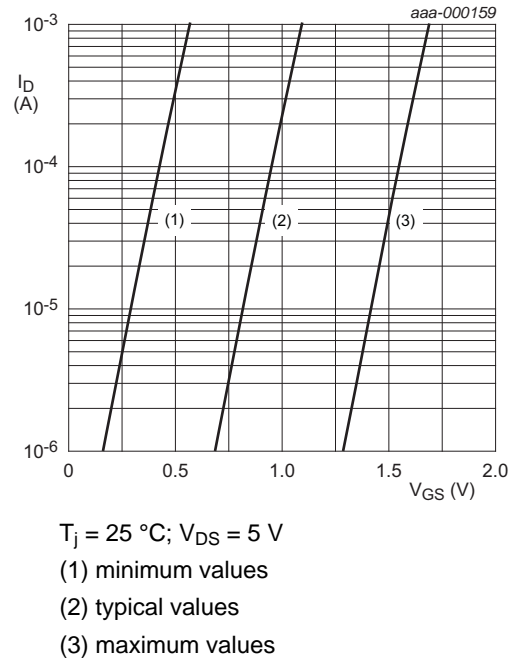
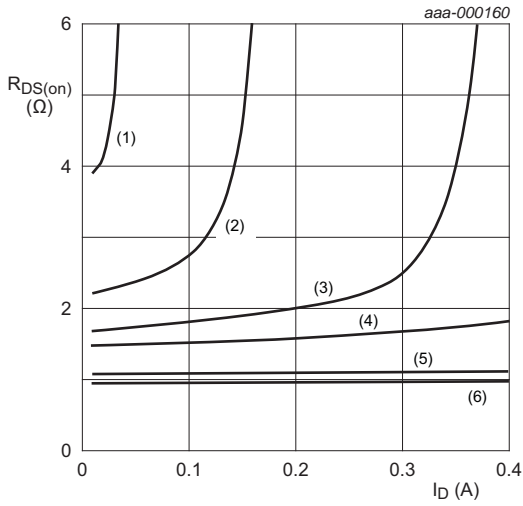
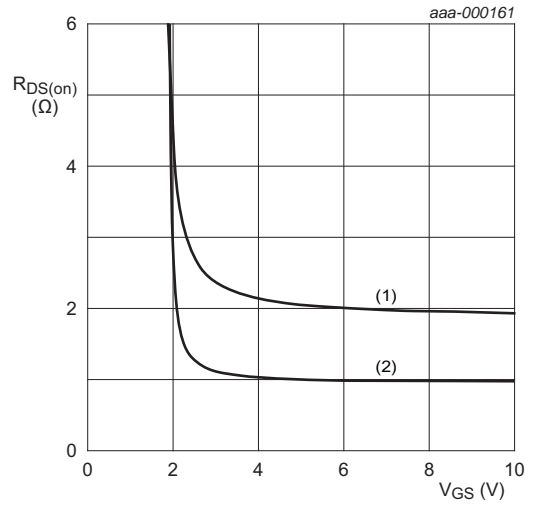


Fig 7. Sub-threshold drain current as a function of gate-source voltage



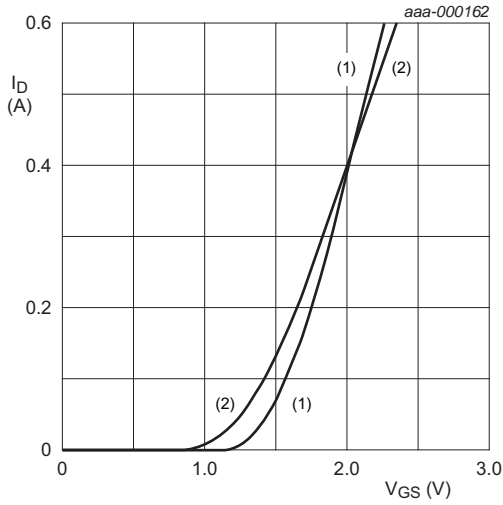
$T_j = 25\text{ }^\circ\text{C}$
 (1) $V_{GS} = 1.5\text{ V}$
 (2) $V_{GS} = 1.75\text{ V}$
 (3) $V_{GS} = 2.0\text{ V}$
 (4) $V_{GS} = 2.25\text{ V}$
 (5) $V_{GS} = 4.5\text{ V}$
 (6) $V_{GS} = 10\text{ V}$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



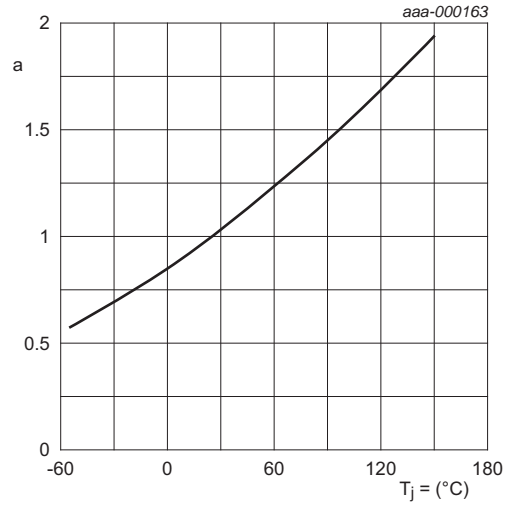
$I_D = 300\text{ mA}$
 (1) $T_j = 150\text{ }^\circ\text{C}$
 (2) $T_j = 25\text{ }^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



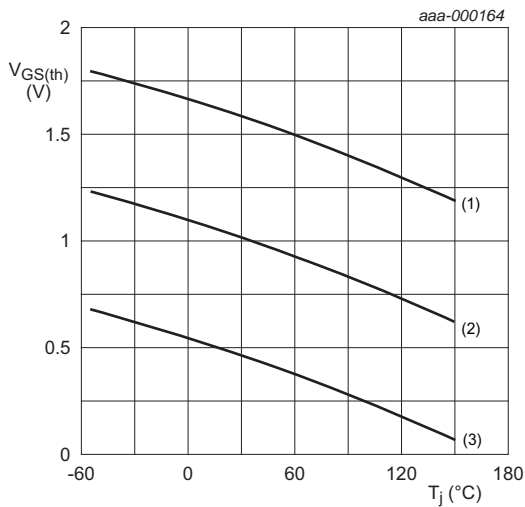
$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ °C}$
 (2) $T_j = 150\text{ °C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



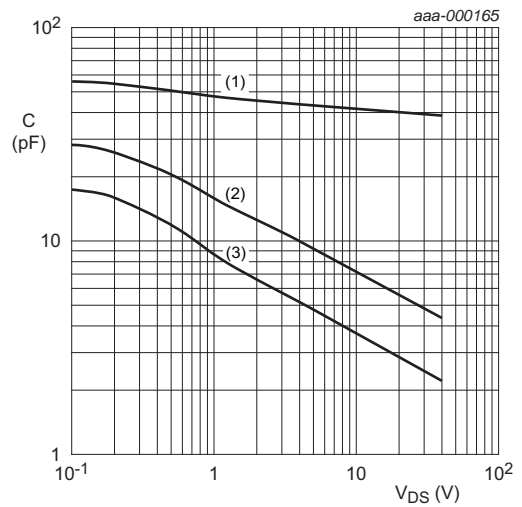
$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



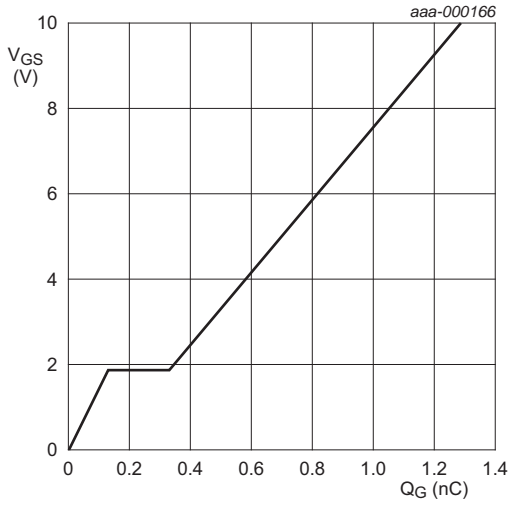
$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.3$ A; $V_{DS} = 30$ V; $T_{amb} = 25$ °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

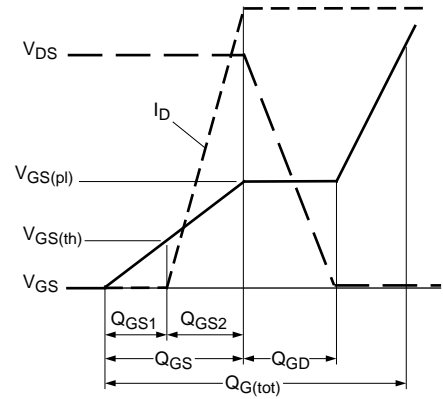
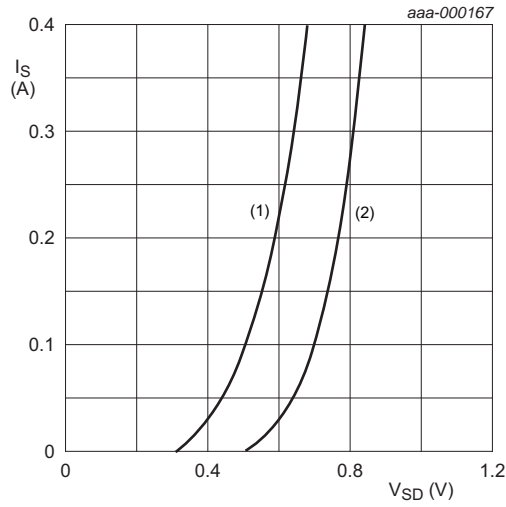


Fig 15. Gate charge waveform definitions



$V_{GS} = 0$ V
 (1) $T_j = 150$ °C
 (2) $T_j = 25$ °C

Fig 16. Source current as a function of source-drain voltage; typical values

8. Test information



Fig 17. Duty cycle definition

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

Plastic surface-mounted package; 3 leads

SOT23

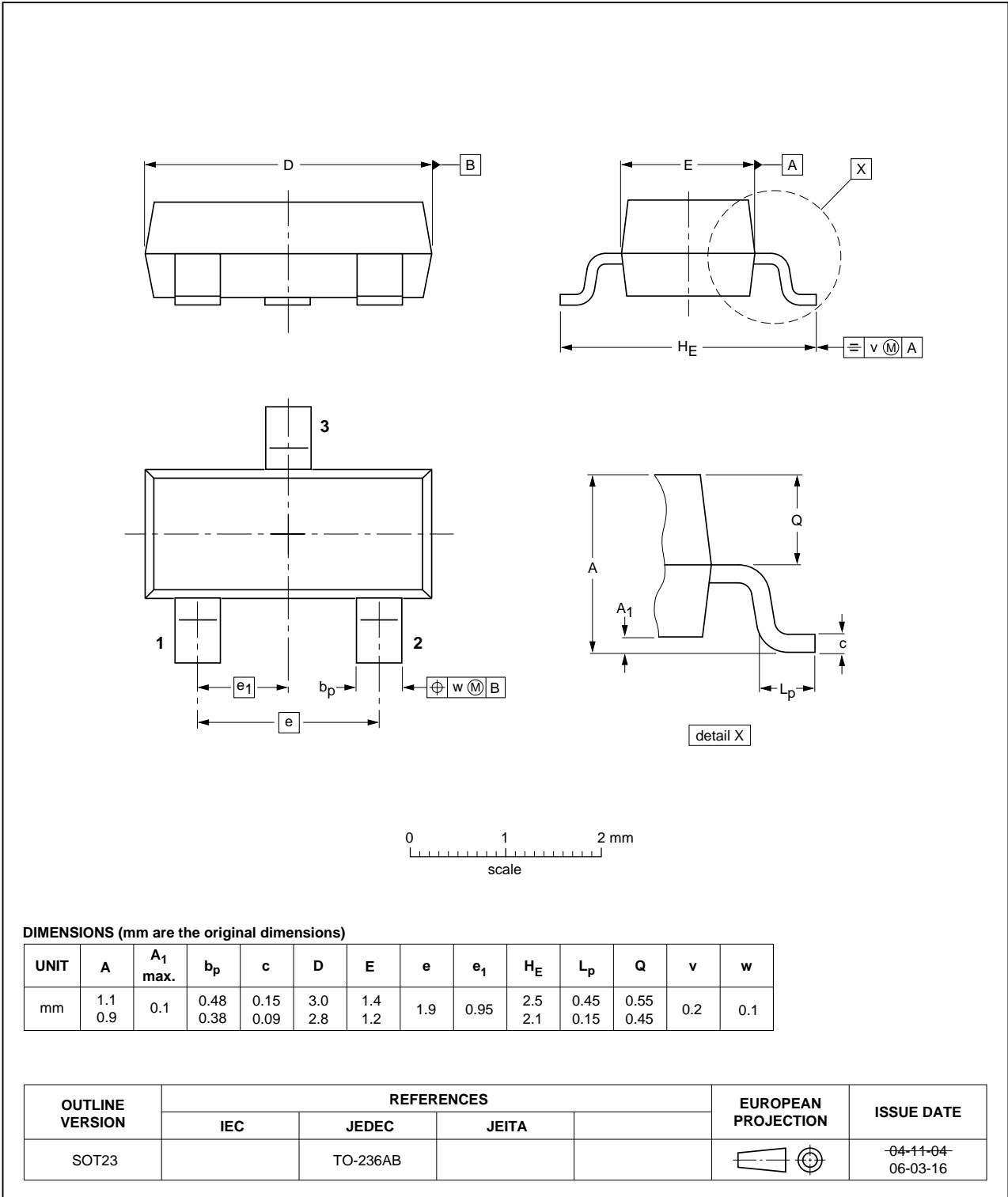


Fig 18. Package outline SOT23 (TO-236AB)

10. Soldering

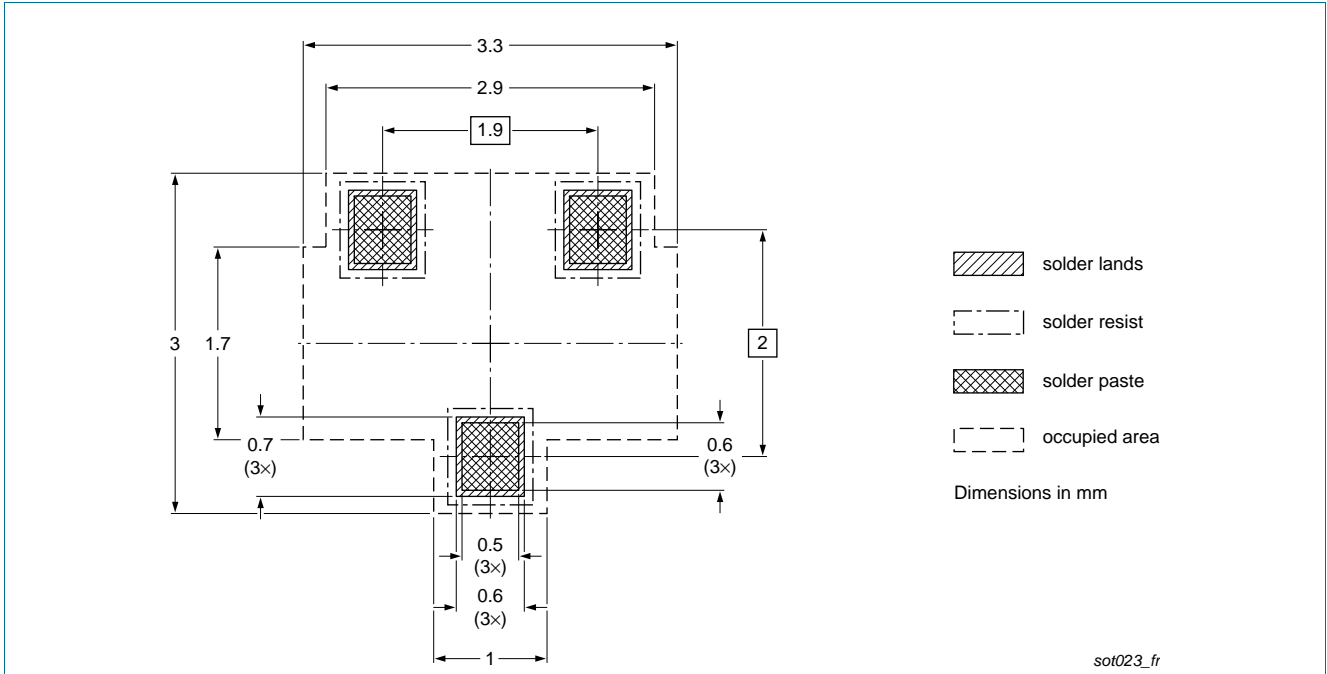


Fig 19. Reflow soldering footprint for SOT23 (TO-236AB)

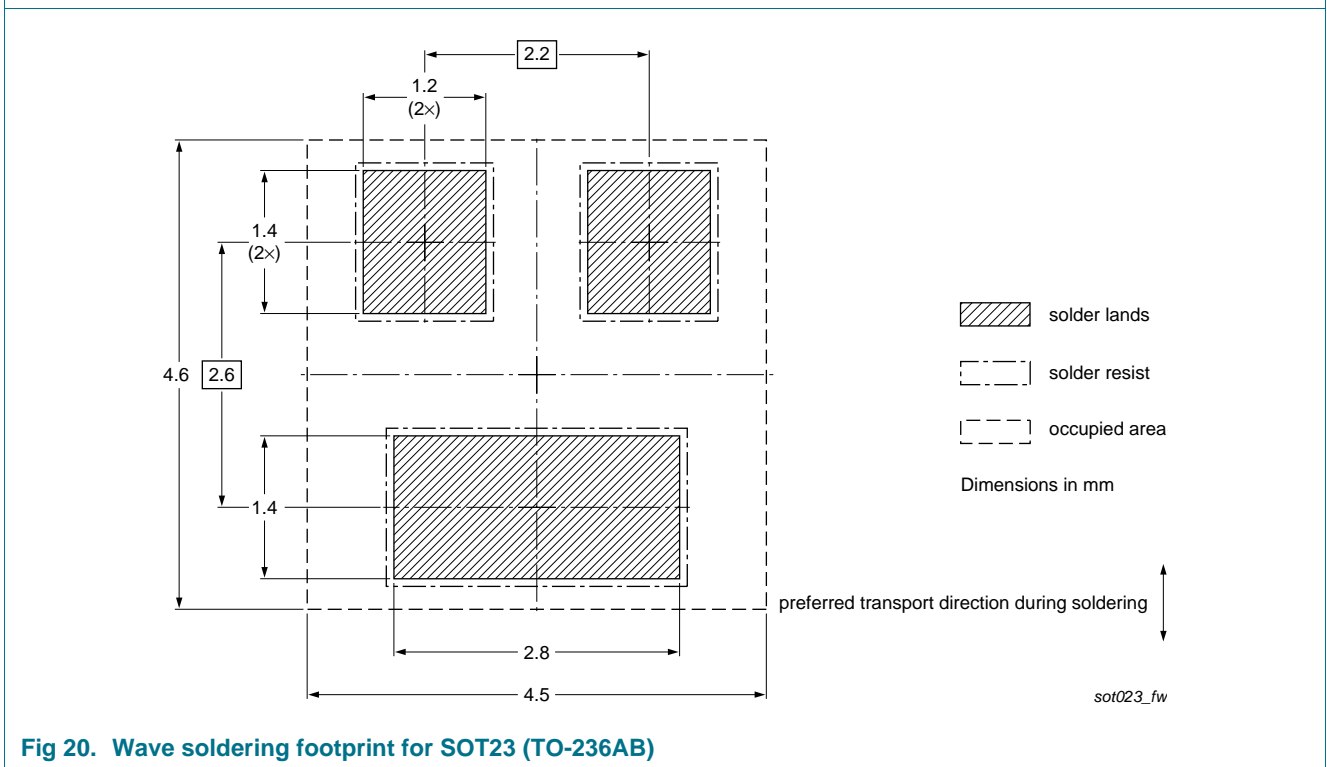


Fig 20. Wave soldering footprint for SOT23 (TO-236AB)

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS138BK v.1	20110804	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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