

# BUK661R6-30C

## N-channel TrenchMOS intermediate level FET

Rev. 01 — 6 September 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Suitable for intermediate level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	-	120	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	306	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 16</a>	-	1.4	1.6	mΩ



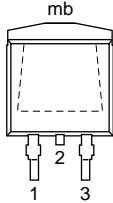
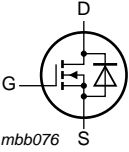
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^\circ\text{C}$ ; unclamped	-	-	1.707	J
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 24\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	63	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT404 (D2PAK)**

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK661R6-30C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	30	V
$V_{GS}$	gate-source voltage	Pulsed [1]	-20	20	V
		DC [2]	-16	16	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$ ; see Figure 1 [3]	-	120	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V}$ ; see Figure 1 [3]	-	120	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see Figure 3	-	1310	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see Figure 2	-	306	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$ [3]	-	120	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	1310	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}$ ; unclamped	-	1.707	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	[4][5][6]	-	-	J

[1] Accumulated pulse duration not to exceed 5mins.

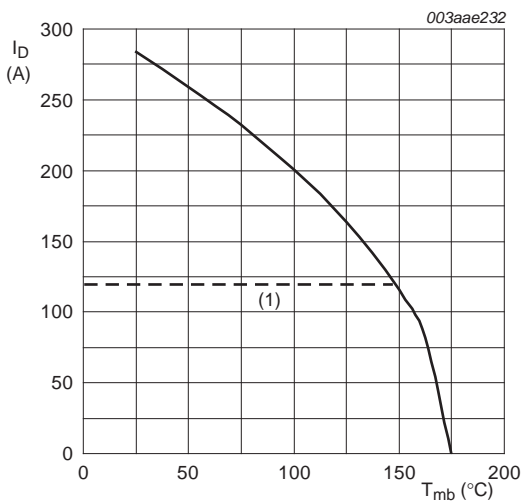
[2] -16V accumulated duration not to exceed 168 hrs.

[3] Continuous current is limited by package.

[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

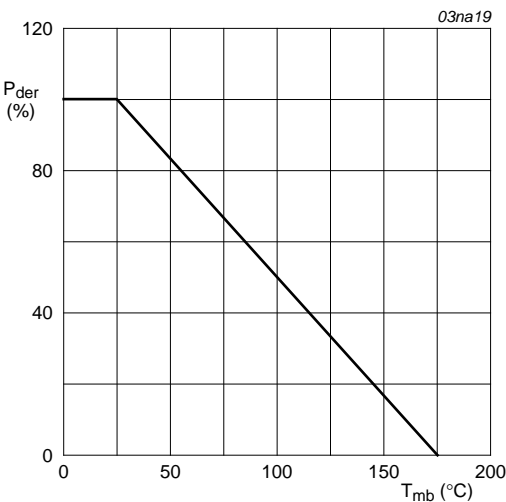
[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[6] Refer to application note AN10273 for further information.



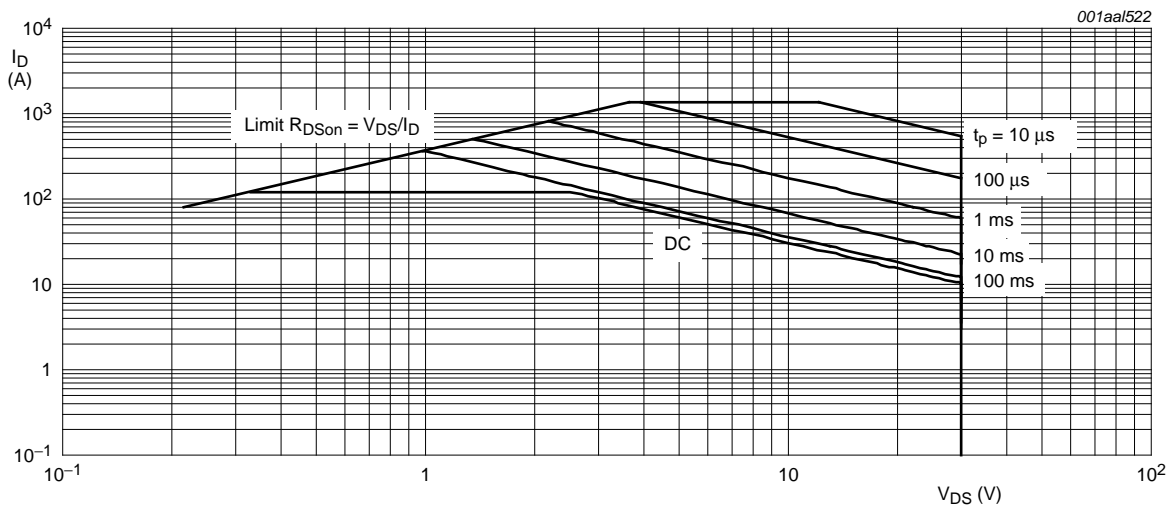
$V_{GS} \geq 10\text{ V}$   
(1) Capped at 120 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



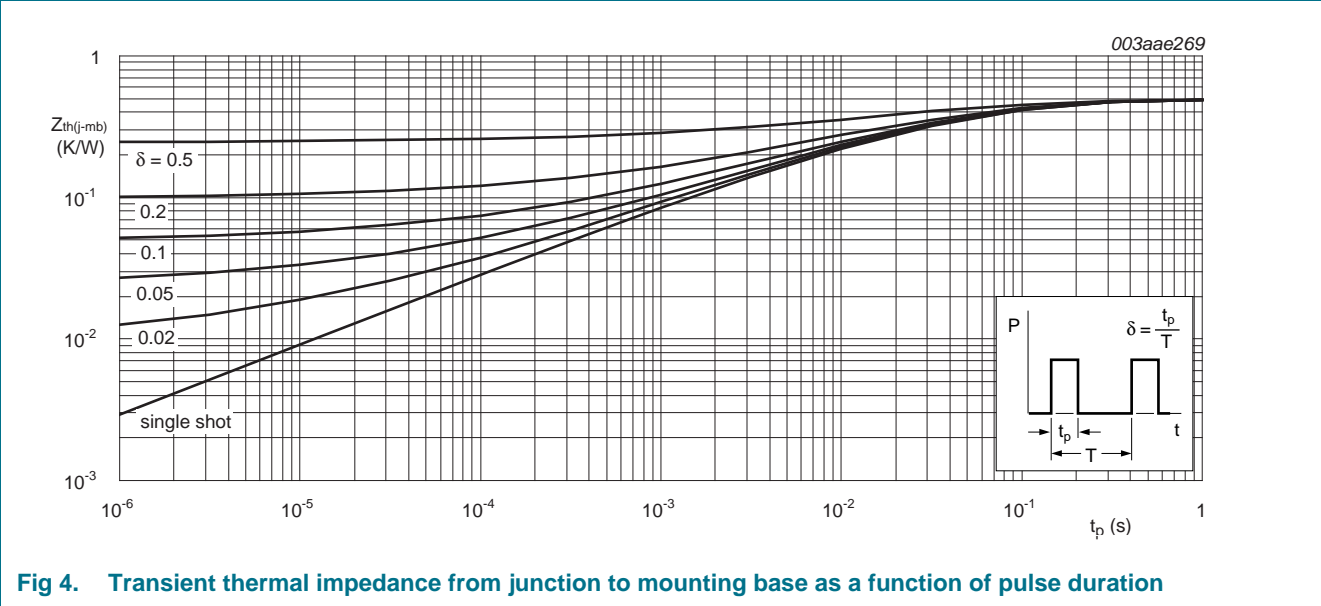
$T_{mb} = 25^\circ\text{C}; I_{DM}$  is single pulse  
(1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.49	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W



## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	30	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	27	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	1.8	2.3	2.8	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; see <a href="#">Figure 10</a>	-	-	3.3	V
		I <sub>D</sub> = 2.5 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; see <a href="#">Figure 10</a>	0.8	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
		V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 20 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>DS</sub> = 0 V; V <sub>GS</sub> = -20 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 16</a>	-	1.4	1.6	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 16</a>	-	2.1	3.3	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 16</a>	-	1.7	2.5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; see <a href="#">Figure 11</a>	-	-	3.2	mΩ
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 10 V; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	229	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 5 V; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	131	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 10 V; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	38	-	nC
Q <sub>GD</sub>	gate-drain charge		-	63	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 14</a>	-	11223	14964	pF
C <sub>oss</sub>	output capacitance		-	1780	2136	pF
C <sub>rss</sub>	reverse transfer capacitance		-	1085	1486	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 25 V; R <sub>L</sub> = 1 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 10 Ω	-	53	-	ns
t <sub>r</sub>	rise time		-	114	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	363	-	ns
t <sub>f</sub>	fall time		-	192	-	ns
L <sub>D</sub>	internal drain inductance	from upper edge of drain mounting base to centre of die ; T <sub>j</sub> = 25 °C	-	3.5	-	nH
L <sub>S</sub>	internal source inductance	from source lead to source bond pad ; T <sub>i</sub> = 25 °C	-	7.5	-	nH

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; see Figure 15	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	70	-	ns
$Q_r$	recovered charge	$V_{DS} = 25\text{ V}$	-	0.138	-	nC

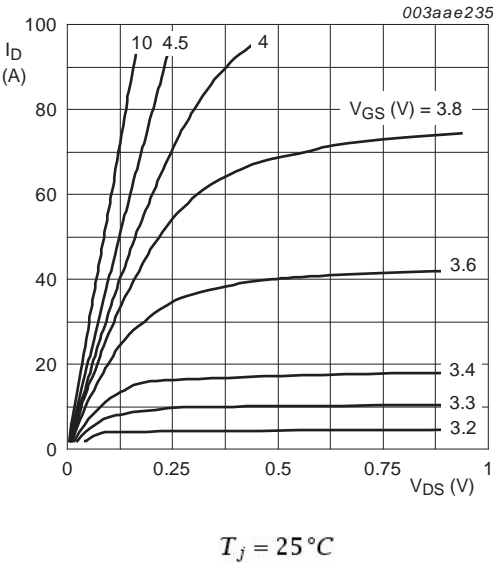


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

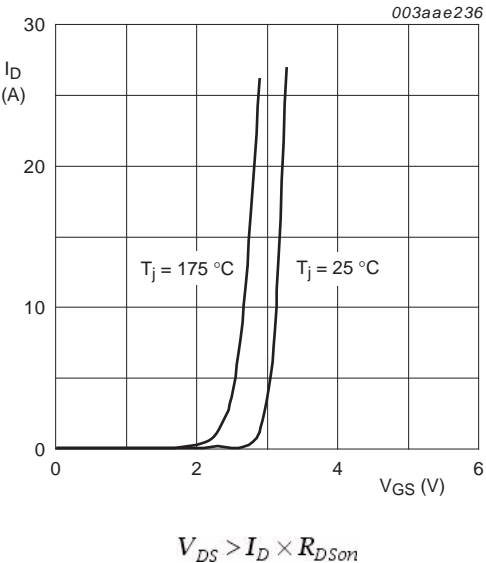


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

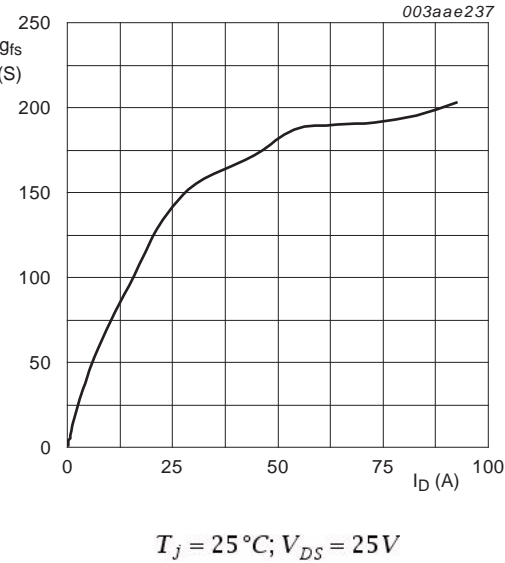


Fig 7. Forward transconductance as a function of drain current; typical values

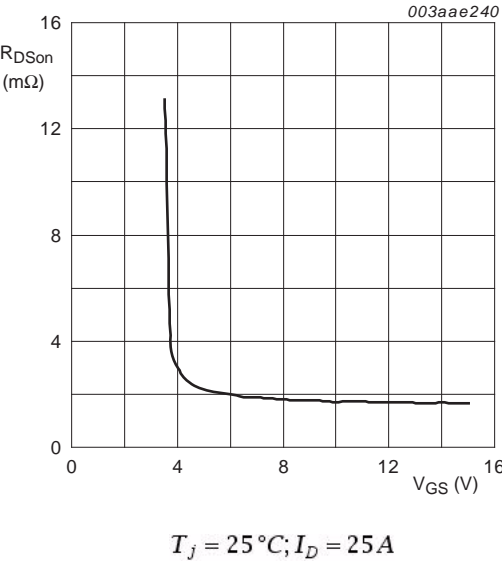
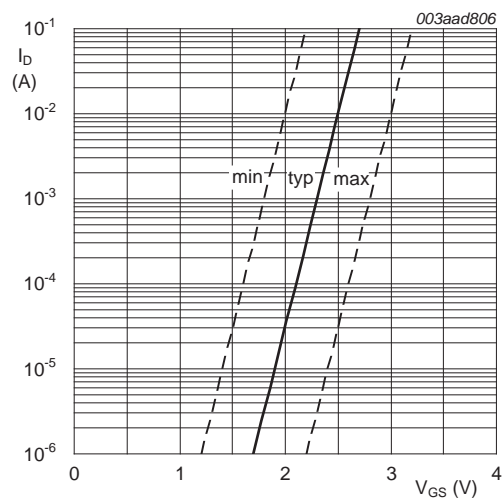
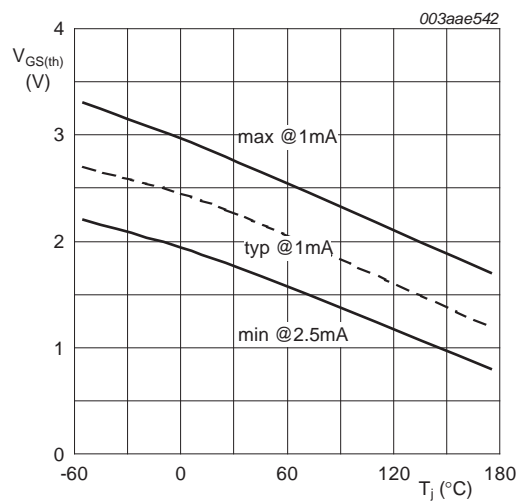


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



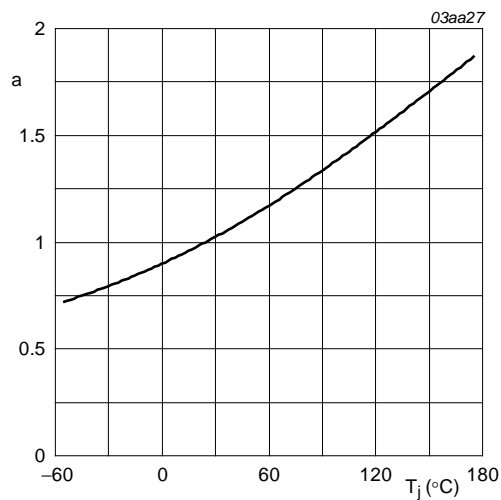
$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature

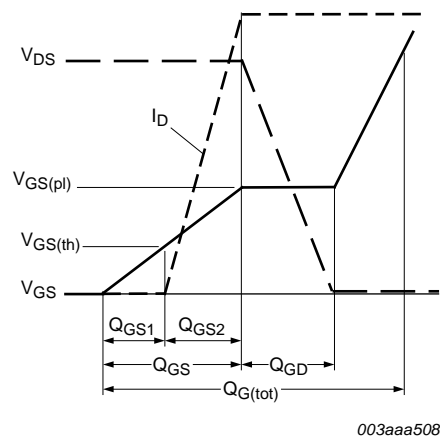
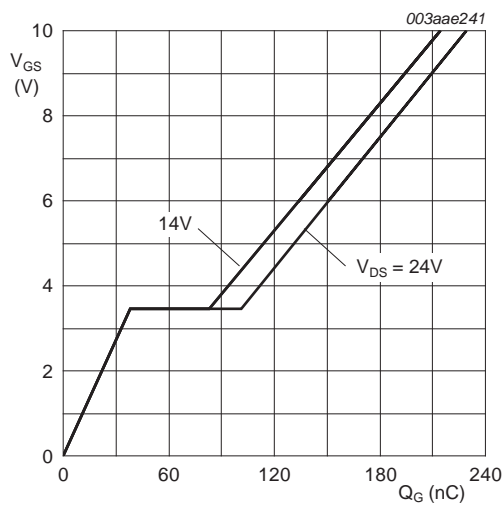


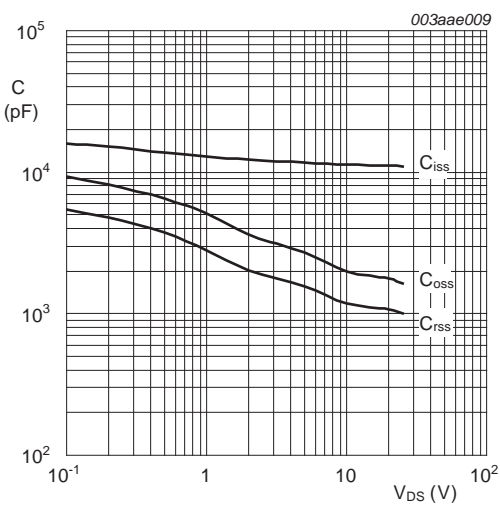
Fig 12. Gate charge waveform definitions





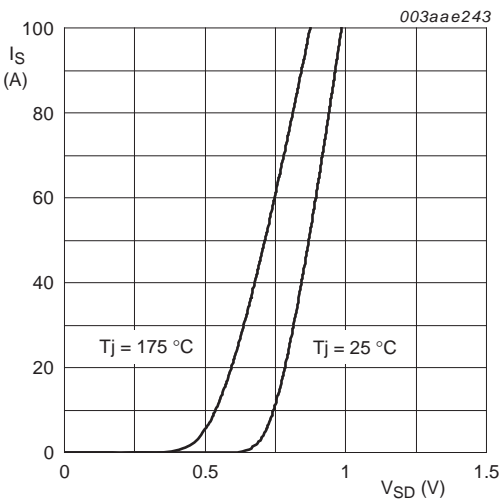
$T_j = 25^\circ C; I_D = 25A$

Fig 13. Gate-source voltage as a function of gate charge; typical values



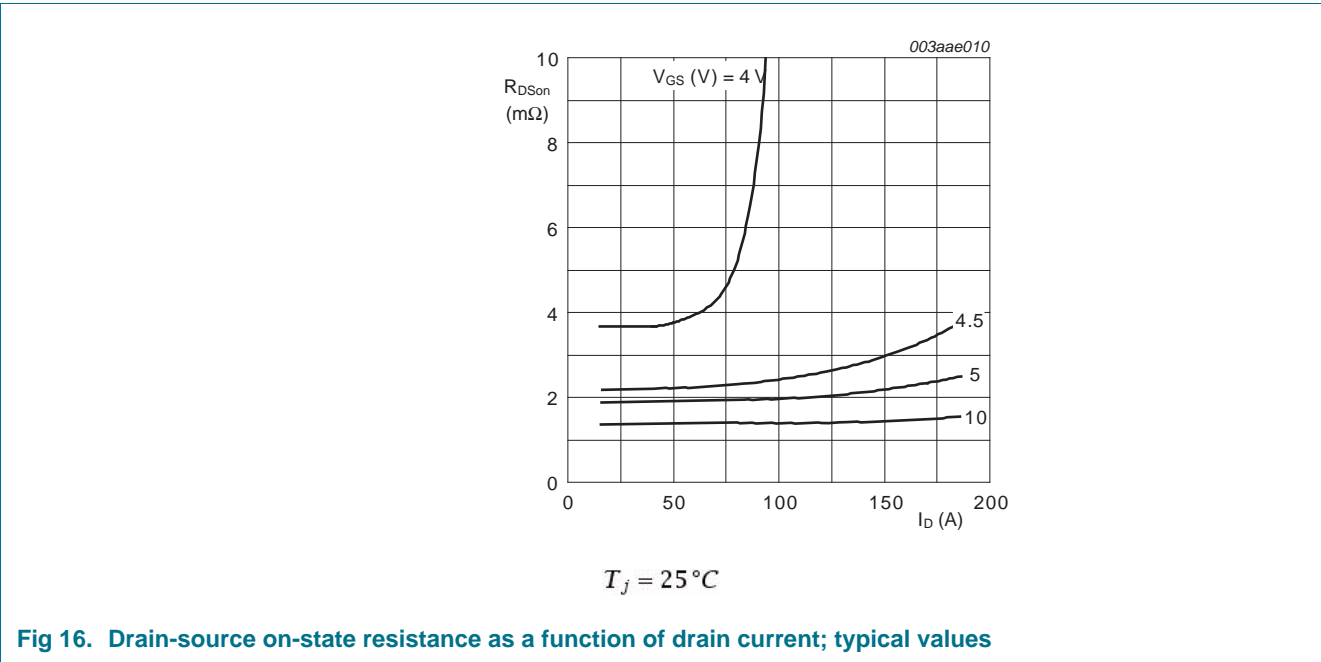
$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitance as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D <sub>max.</sub>	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 17. Package outline SOT404 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK661R6-30C v.1	20100906	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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