

# **BUK6C2R1-55C**

# N-channel TrenchMOS intermediate level FET

Rev. 3 — 18 January 2012

**Product data sheet** 

## 1. Product profile

### 1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high-performance automotive applications.

#### 1.2 Features and benefits

- AEC Q101 compliant
- High current handling capability, up to 320 A
- Low conduction losses due to very low on-state resistance
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoids
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	55	V
I <sub>D</sub>	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C};$ see Figure 1	-	-	228	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	300	W
Static chara	acteristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 90 \text{ A};$ $T_j = 25 \text{ °C};$ see Figure 11	-	1.9	2.3	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic cl	naracteristics					
$Q_{GD}$	gate-drain charge	$I_D$ = 180 A; $V_{DS}$ = 44 V; $V_{GS}$ = 10 V; see <u>Figure 13</u> ; see <u>Figure 14</u>	-	79	-	nC
Avalanche	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D = 120 \text{ A; } V_{sup} \le 55 \text{ V;} \\ R_{GS} = 50 \Omega; V_{GS} = 10 \text{ V;} \\ T_{j(init)} = 25 ^{\circ}\text{C; unclamped}$	-	-	770	mJ

# 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source	mb	D
3	S	source		
4	D	drain[1]		
5	S	source	THE THE PARTY OF T	mbb076 S
6	S	source		
7	S	source	SOT427 (D2PAK)	
mb	D	mounting base; connected to drain		

<sup>[1]</sup> It is not possible to connect to pin 4 of the SOT427 package.

# 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6C2R1-55C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)	SOT427

# 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	55	V
$V_{GS}$	gate-source voltage	Pulsed	<u>[1]</u> -20	20	V
		DC	<u>[2]</u> -16	16	V
I <sub>D</sub>	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u>	-	228	Α
		$T_{amb}$ = 100 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u>	-	162	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; see Figure 3	-	914	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	300	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drain	diode				
Is	source current	T <sub>mb</sub> = 25 °C	-	228	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$	-	914	Α
Avalanche ru	iggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 120 A; $V_{sup} \le 55$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped	-	770	mJ

- [1] Accumulated pulse duration not to exceed 5mins.
- [2] -16V accumulated duration not to exceed 168 hrs.

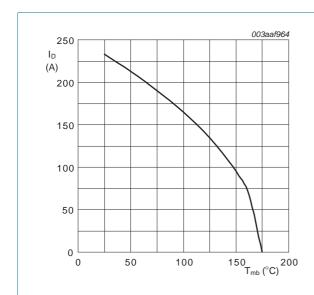


Fig 1. Continuous drain current as a function of mounting base temperature

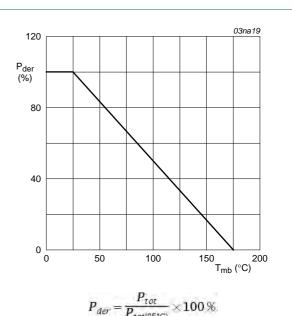
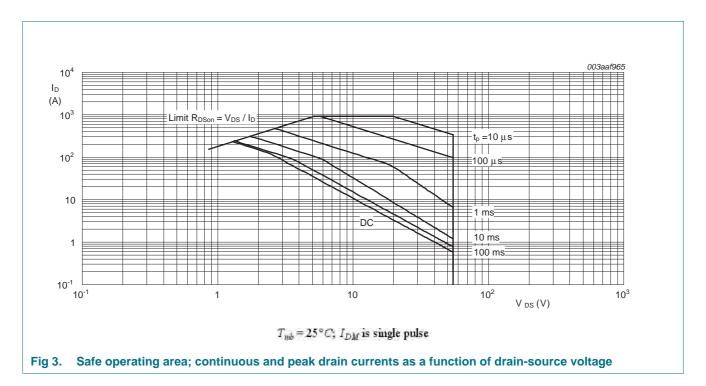


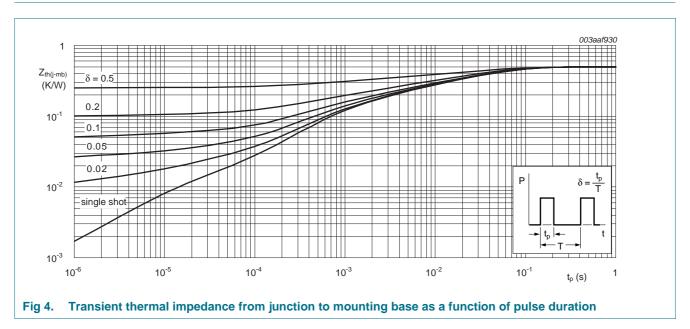
Fig 2. Normalized total power dissipation as a function of mounting base temperature



### 5. Thermal characteristics

#### Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.5	K/W



# 6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
$V_{(BR)DSS}$	drain-source	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	55	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 \ ^{\circ}C$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ °C}$ ; see <u>Figure 9</u> ; see <u>Figure 10</u>	1.8	2.3	2.8	V
$V_{GSth}$	gate-source threshold voltage	$I_D$ = 2.5 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 175 °C; see <u>Figure 10</u>	8.0	-	-	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = -55 °C; see <u>Figure 10</u>	-	-	3.3	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.04	1	μΑ
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 ^{\circ}\text{C}$	-	-	500	μΑ
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_{D}$ = 90 A; $T_{j}$ = 25 °C; see <u>Figure 11</u>	-	1.9	2.3	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 90 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 11</u>	-	2.4	3.1	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 90 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 11	-	2.6	3.7	mΩ
		$V_{GS}$ 10 V; $I_D$ = 90 A; $T_j$ = 175 °C; see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	5.7	mΩ
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D$ = 180 A; $V_{DS}$ = 44 V; $V_{GS}$ = 10 V; see <u>Figure 13</u> ; see <u>Figure 14</u>	-	253	-	nC
		$I_D$ = 180 A; $V_{DS}$ = 44 V; $V_{GS}$ = 5 V; see <u>Figure 13</u> ; see <u>Figure 14</u>	-	140	-	nC
Q <sub>GS</sub>	gate-source charge	$I_D = 180 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 10 \text{ V};$	-	40	-	nC
$Q_{GD}$	gate-drain charge	see Figure 13; see Figure 14	-	79	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	12000	16000	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 15</u>	-	1075	1290	pF
C <sub>rss</sub>	reverse transfer capacitance		-	730	1000	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 0.3 \Omega; V_{GS} = 10 \text{ V};$	-	43	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega$	-	206	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	412	-	ns
t <sub>f</sub>	fall time		-	190	-	ns
Source-d	rain diode					
V <sub>SD</sub>	source-drain voltage	$I_S = 80 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 16</u>	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 50 \text{ A}$ ; $dI_S/dt = -100 \text{ A/}\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ;	-	56	-	ns
Q <sub>r</sub>	recovered charge	$V_{DS} = 30 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	115	-	nC

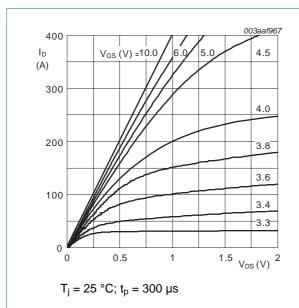


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

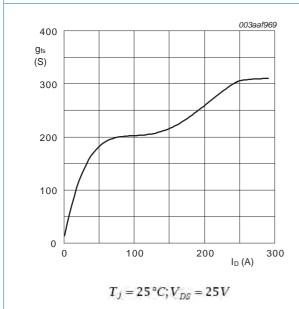


Fig 7. Forward transconductance as a function of drain current; typical values

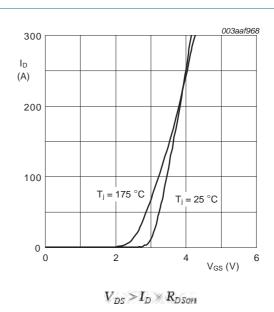
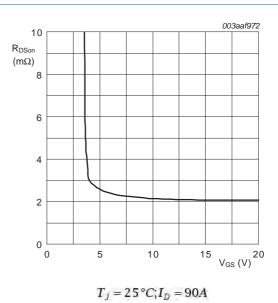


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



ig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

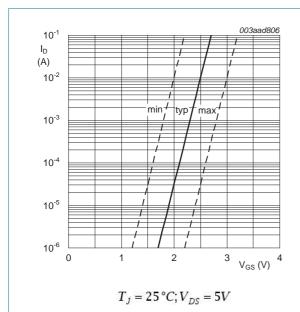


Fig 9. Sub-threshold drain current as a function of gate-source voltage

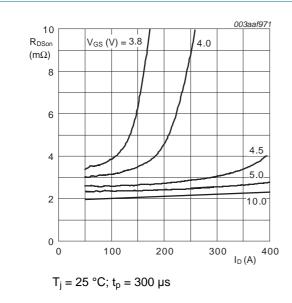


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

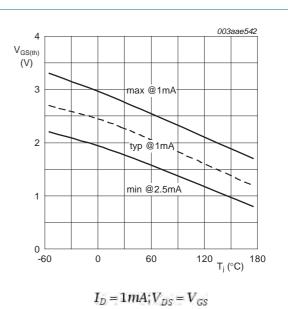


Fig 10. Gate-source threshold voltage as a function of junction temperature

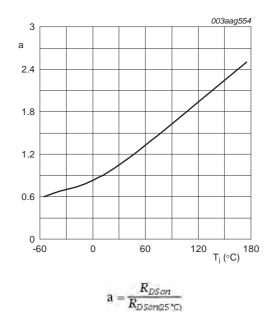


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

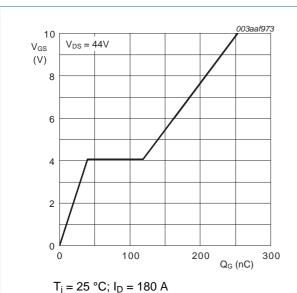


Fig 13. Gate-source voltage as a function of gate charge; typical values

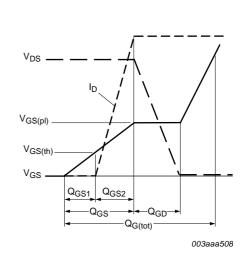


Fig 14. Gate charge waveform definitions

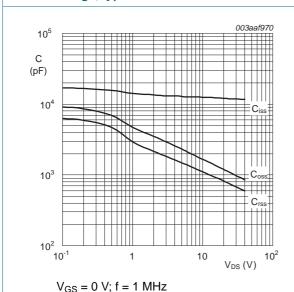
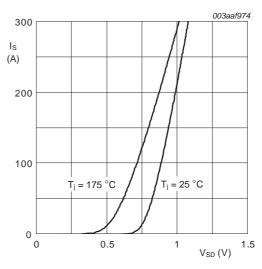


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{GS} = 0 V$ 

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

# 7. Package outline

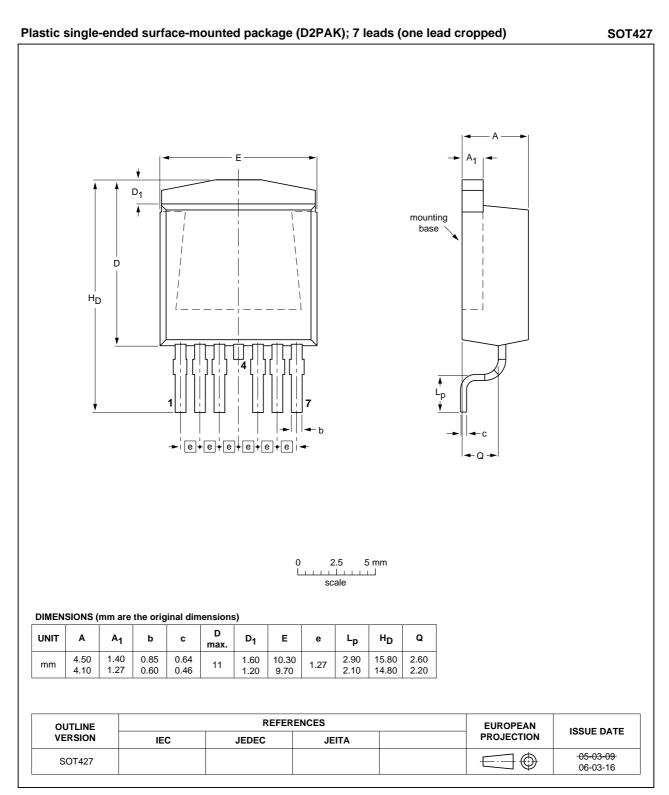


Fig 17. Package outline SOT427 (D2PAK)

# 8. Revision history

#### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6C2R1-55C v.3	20120118	Product data sheet	-	BUK6C2R1-55C v.2
Modifications:	<ul> <li>Status change</li> </ul>	ed from preliminary to produc	et.	
BUK6C2R1-55C v.2	20111221	Preliminary data shee	t -	BUK6C2R1-55C v.1

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#### 9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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# **BUK6C2R1-55C**

#### N-channel TrenchMOS intermediate level FET

## 11. Contents

1	Product profile
1.1	General description
1.2	Features and benefits1
1.3	Applications
1.4	Quick reference data1
2	Pinning information2
3	Ordering information
4	Limiting values
5	Thermal characteristics4
6	Characteristics5
7	Package outline
8	Revision history10
9	Legal information11
9.1	Data sheet status
9.2	Definitions11
9.3	Disclaimers
9.4	Trademarks12
10	Contact information

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