

BUK754R0-55B; BUK764R0-55B

N-channel TrenchMOS standard level FET

Rev. 04 — 4 October 2007

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology.

1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

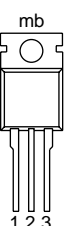
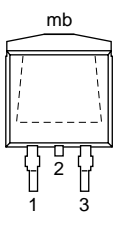
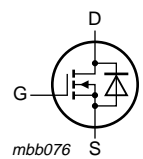
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V and 24 V loads

1.4 Quick reference data

- $E_{DS(AL)S} \leq 1.2 \text{ J}$
- $I_D \leq 75 \text{ A}$
- $R_{DS(on)} = 3.4 \text{ m}\Omega \text{ (typ)}$
- $P_{tot} \leq 300 \text{ W}$

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline		Symbol
1	gate (G)	 03ab54 SOT78A (TO-220AB)	 SOT404 (D2PAK)	 mbb076
2	drain (D)			
3	source (S)			
mb	mounting base; connected to drain (D)			

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUK754R0-55B	SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A
BUK764R0-55B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{DS}	drain-source voltage		-	55	V	
V _{DGR}	drain-gate voltage (DC)	R _{GS} = 20 kΩ	-	55	V	
V _{GS}	gate-source voltage		-	±20	V	
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 2 and 3	[1][3]	-	193	A
			[2]	-	75	A
		T _{mb} = 100 °C; V _{GS} = 10 V; see Figure 2	[2]	-	75	A
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs; see Figure 3	-	774	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 1	-	300	W	
T _{stg}	storage temperature		-55	+175	°C	
T _j	junction temperature		-55	+175	°C	
Source-drain diode						
I _{DR}	reverse drain current	T _{mb} = 25 °C	[1][2]	-	193	A
			[2]	-	75	A
I _{DRM}	peak reverse drain current	T _{mb} = 25 °C; pulsed; t _p ≤ 10 μs	-	774	A	
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	unclamped inductive load; I _D = 75 A; V _{DS} ≤ 55 V; R _{GS} = 50 Ω; V _{GS} = 10 V; starting at T _j = 25 °C	-	1.2	J	
E _{DS(AL)R}	repetitive drain-source avalanche energy		[4]	-	-	J

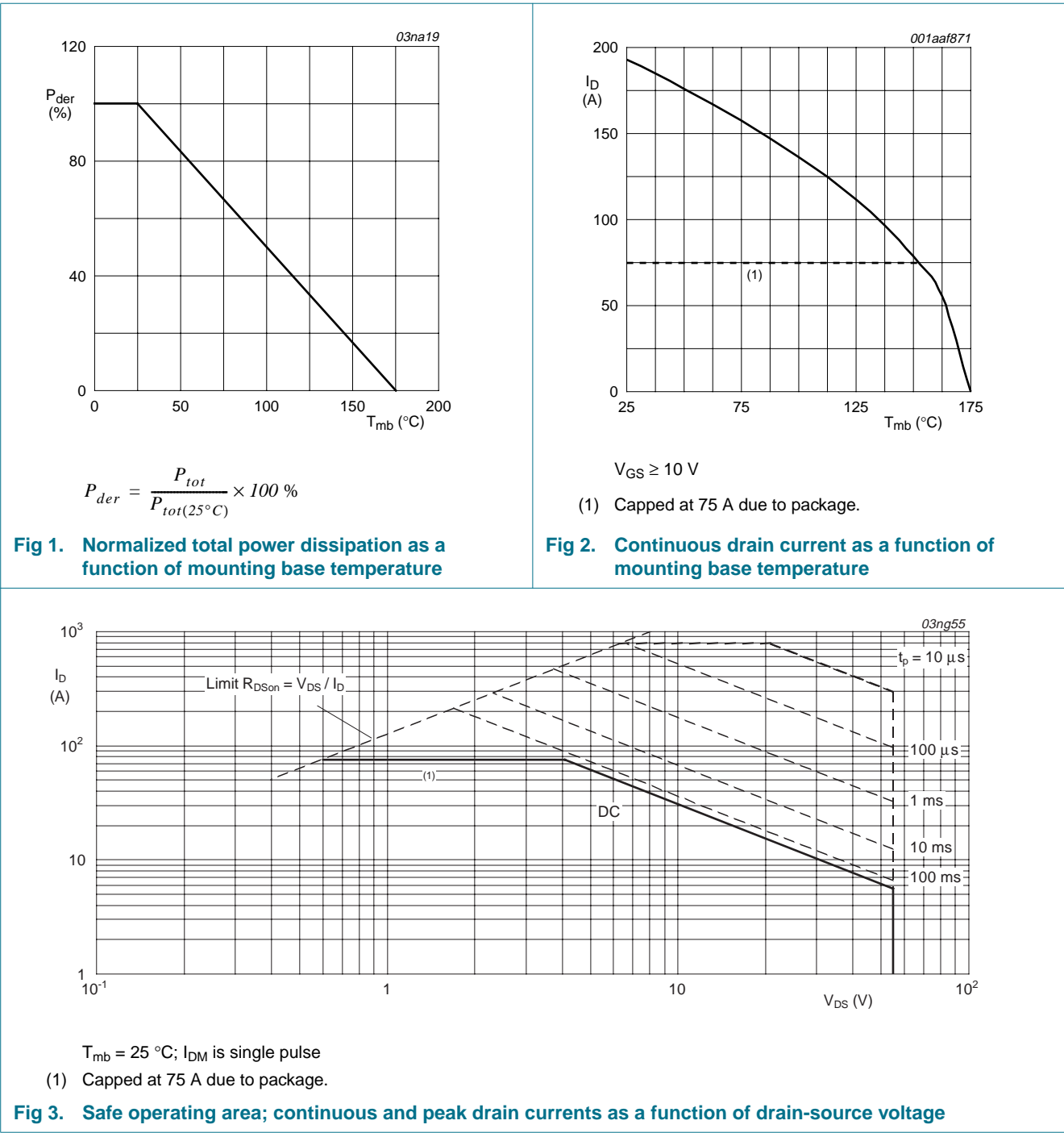
[1] Current is limited by chip power dissipation rating.

[2] Continuous current is limited by package.

[3] Refer to document 9397 750 12572 for further information.

[4] Conditions:

- Maximum value not quoted. Repetitive rating defined in [Figure 16](#).
- Single-pulse avalanche rating limited by $T_{j(max)}$ of $175\text{ }^\circ\text{C}$.
- Repetitive avalanche rating limited by an average junction temperature of $170\text{ }^\circ\text{C}$.
- Refer to application note AN10273 for further information.



5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78A (TO-220AB)	vertical in free air	-	60	-	K/W
	SOT404 (D2PAK)	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W

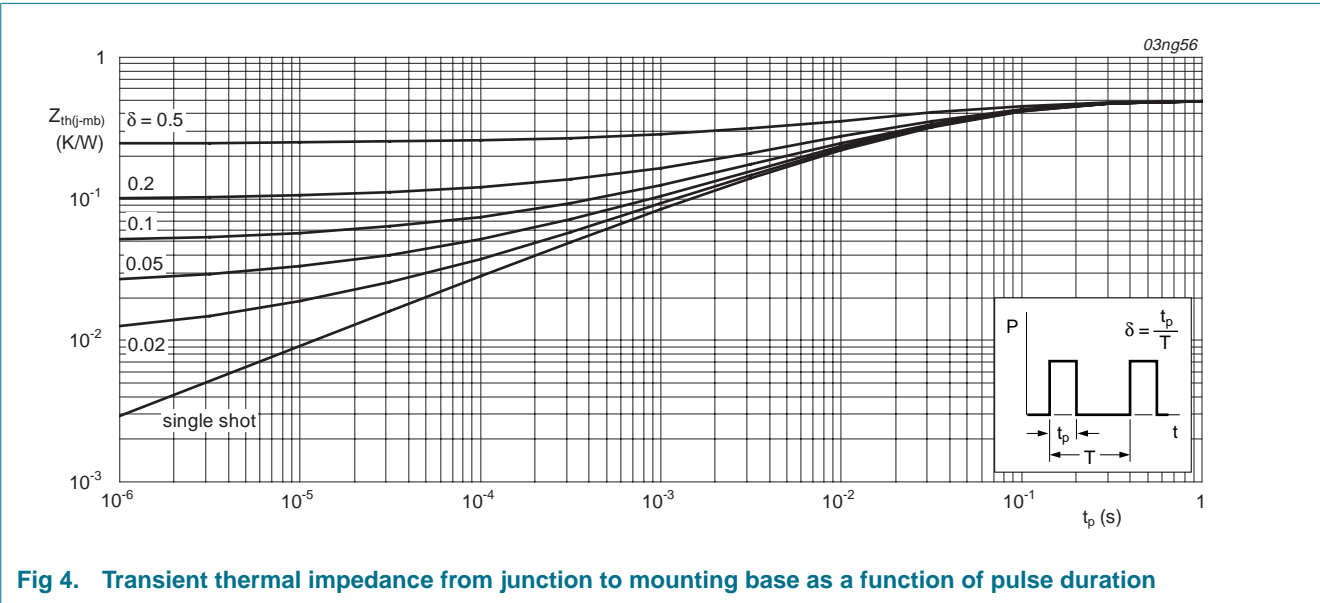


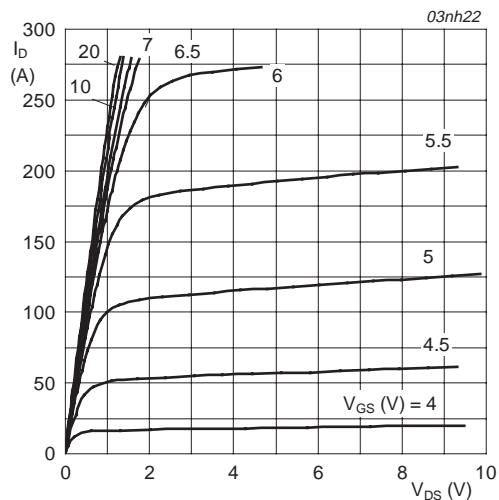
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

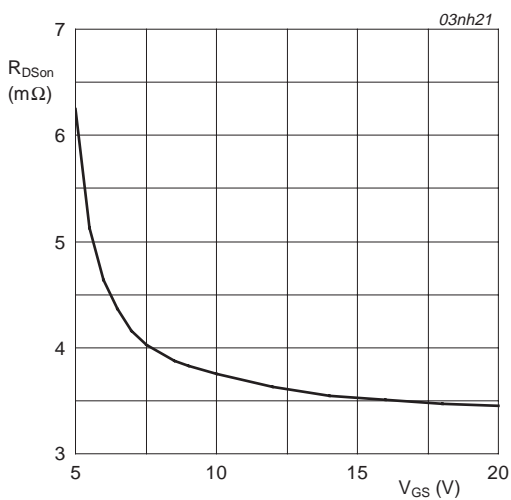
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	55	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9				
		$T_j = 25\text{ }^{\circ}\text{C}$	2	3	4	V
		$T_j = 175\text{ }^{\circ}\text{C}$	1	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 55\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	0.02	1	μA
		$T_j = 175\text{ }^{\circ}\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	3.4	4.0	m Ω
		$T_j = 175\text{ }^{\circ}\text{C}$	-	-	8	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DD} = 44\text{ V}$; $V_{GS} = 10\text{ V}$; see Figure 14	-	86	-	nC
Q_{GS}	gate-source charge		-	18	-	nC
Q_{GD}	gate-drain charge		-	25	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; see Figure 12	-	5082	6776	pF
C_{oss}	output capacitance		-	1054	1265	pF
C_{rss}	reverse transfer capacitance		-	450	617	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}$; $R_L = 1.2\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_G = 10\text{ }\Omega$	-	23	-	ns
t_r	rise time		-	51	-	ns
$t_{d(off)}$	turn-off delay time		-	71	-	ns
t_f	fall time		-	41	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nH
		from contact screw on mounting base to center of die SOT78A	-	3.5	-	nH
		from upper edge of drain mounting base to center of die SOT404	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 40\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = -10\text{ V}$; $V_R = 30\text{ V}$	-	95	-	ns
Q_r	recovered charge		-	251	-	nC



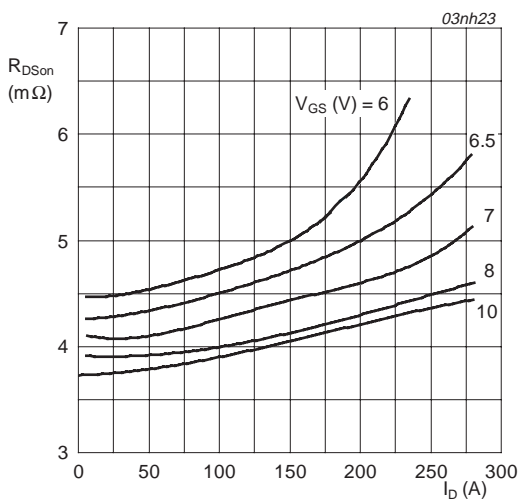
Tj = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



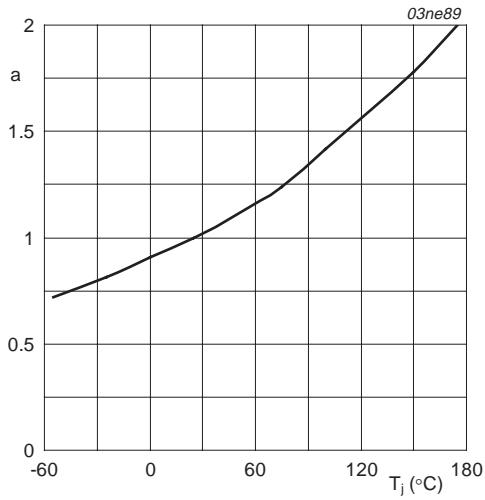
Tj = 25 °C; ID = 25 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



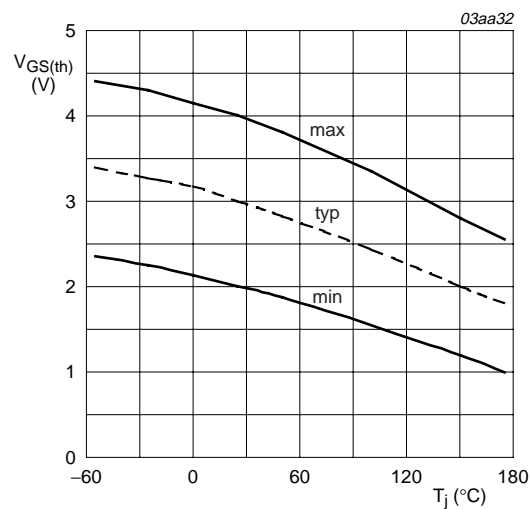
Tj = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



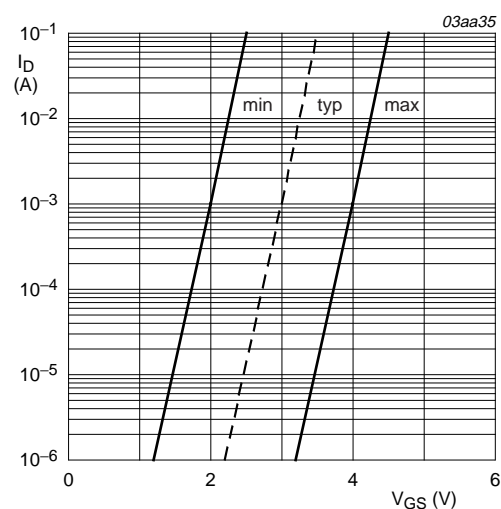
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



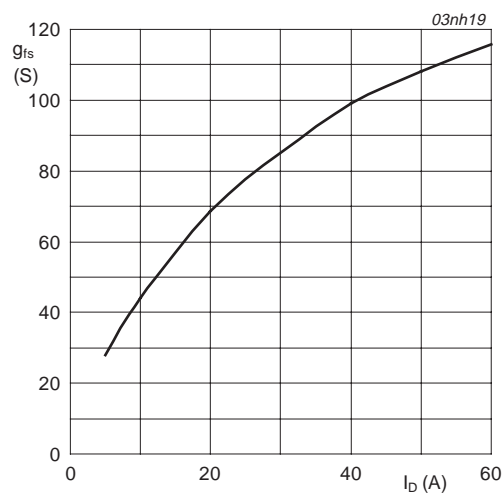
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



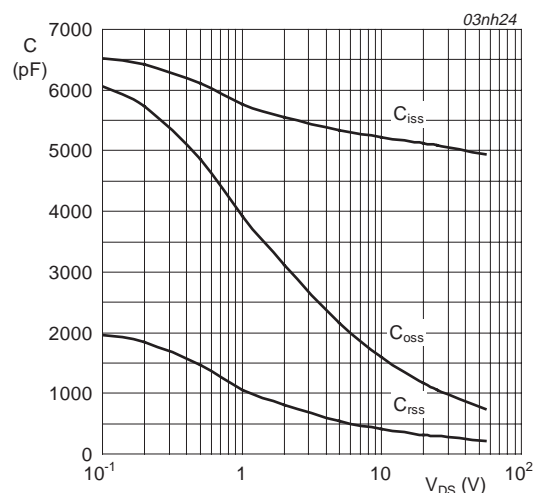
$T_j = 25\text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^{\circ}C; V_{DS} = 25\text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

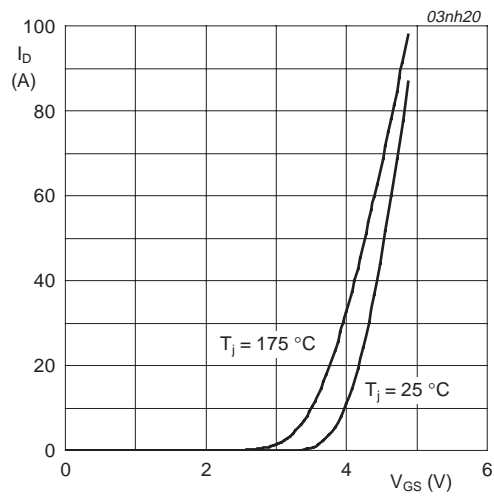


Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values

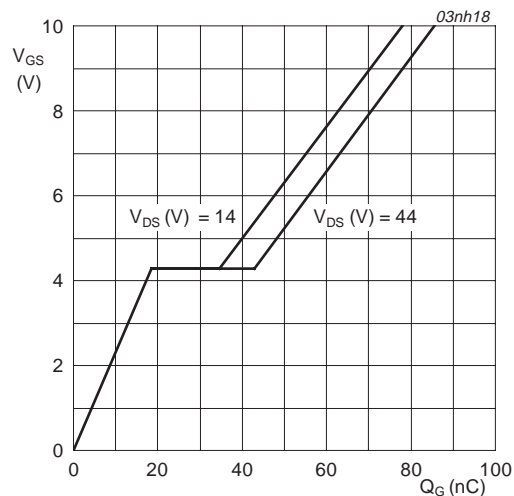


Fig 14. Gate-source voltage as a function of gate charge; typical values

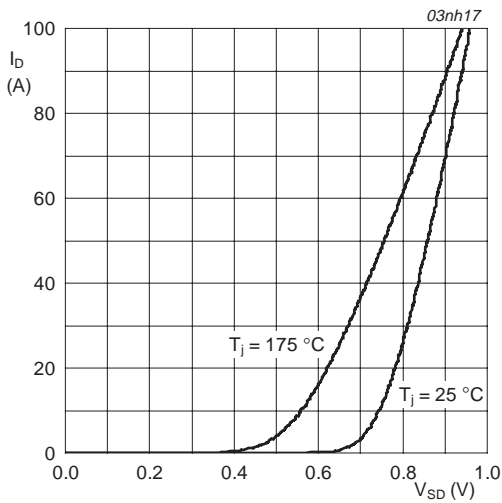
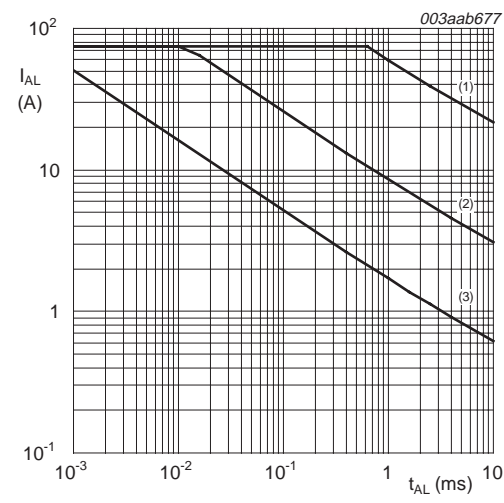


Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



See Table note 4 of Table 3 Limiting values.
 (1) Single-pulse; $T_j = 25\text{ }^{\circ}\text{C}$.
 (2) Single-pulse; $T_j = 150\text{ }^{\circ}\text{C}$.
 (3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78A

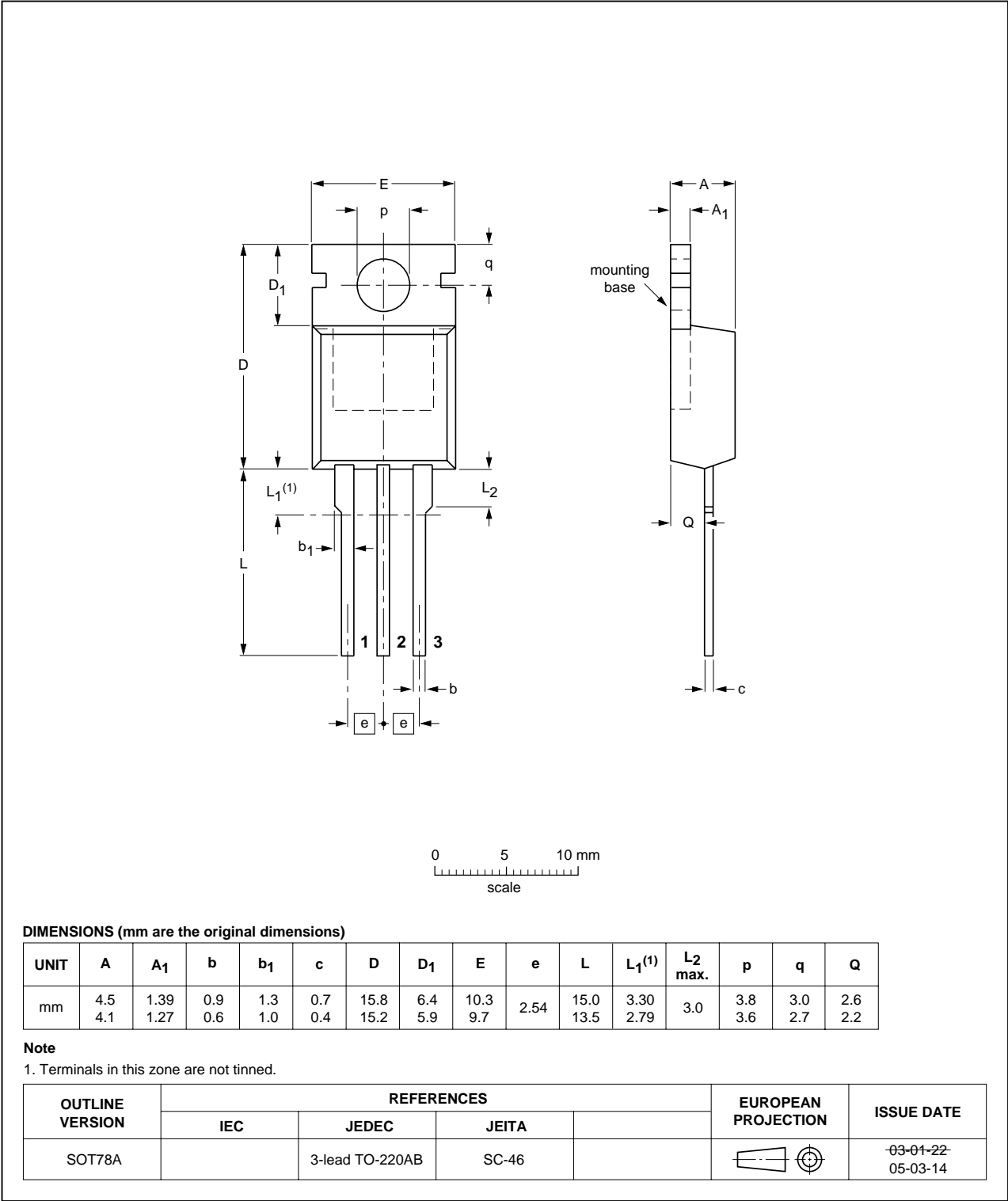
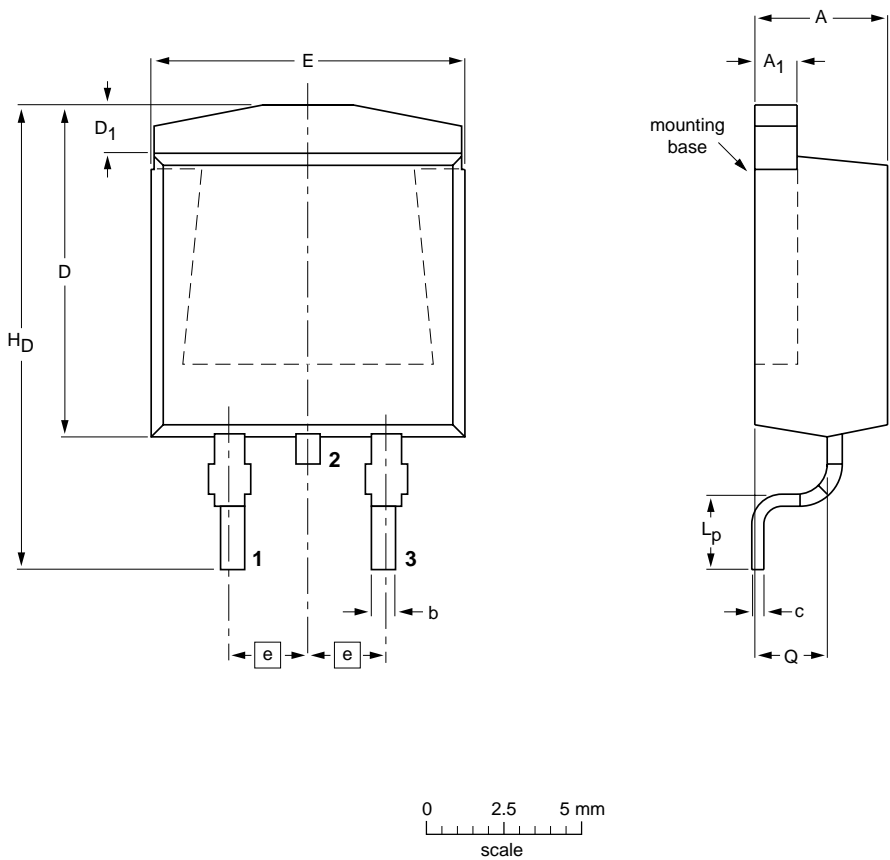


Fig 17. Package outline SOT78A (TO-220AB)

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20


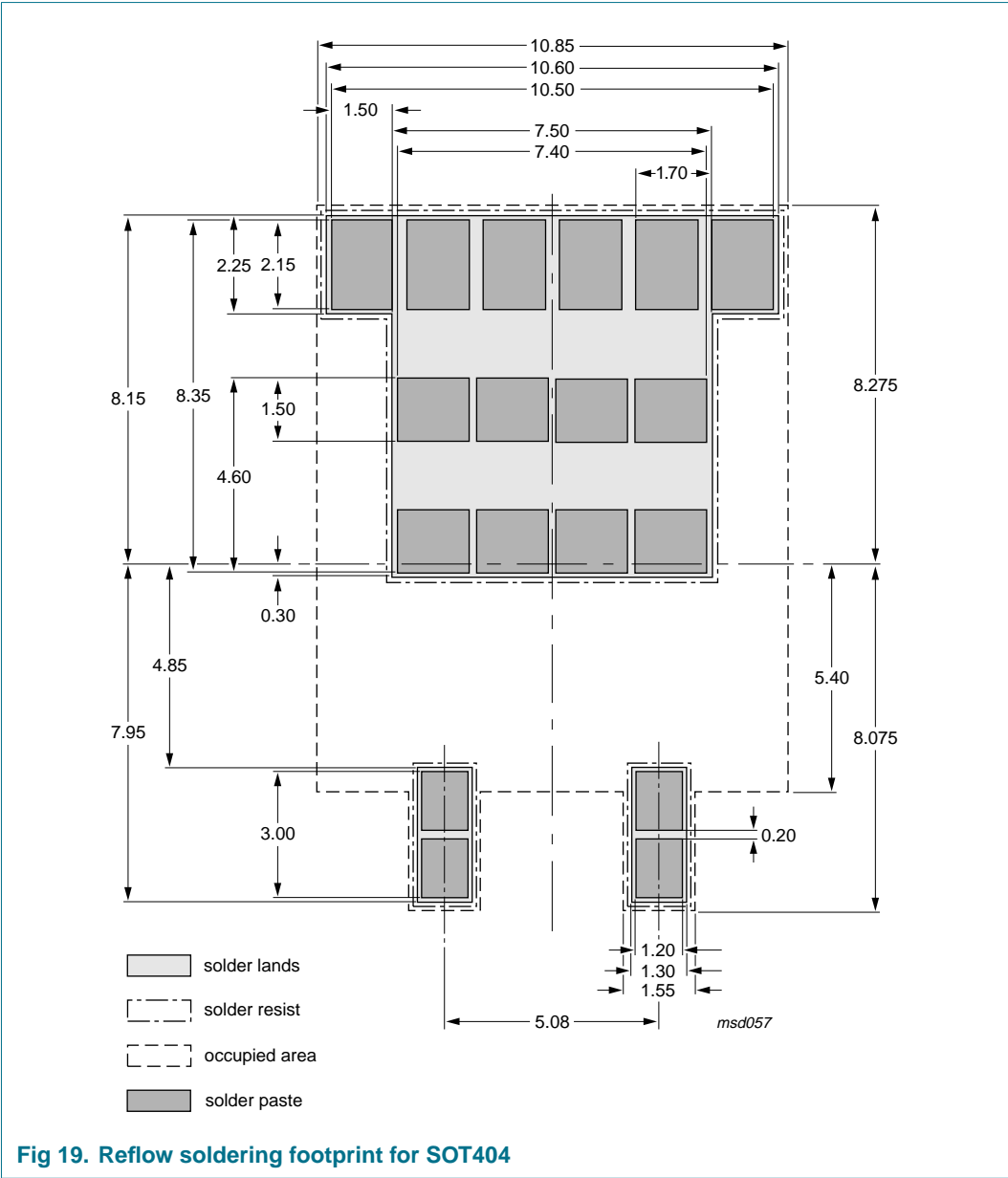
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

8. Soldering



9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK75_764R0-55B_4	20071004	Product data sheet	-	BUK75_764R0-55B_3
Modifications:	<ul style="list-style-type: none">• Figure 7 updated.			
BUK75_764R0-55B_3	20070124	Product data sheet	-	BUK75_764R0_55B-02
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• C_{rss} (typ) and (max) value in Section 6 “Characteristics” changed from 289 (typ) and 396 (max) to 450 (typ) and 617 (max).			
BUK75_764R0_55B-02	20020930	Product data sheet	-	BUK75_764R0_55B-01
BUK75_764R0_55B-01	20020328	Product data sheet	-	-

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10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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