BUK754R0-40C

N-channel TrenchMOS standard level FET

Rev. 02 — 20 July 2010 **Product data sheet**

1. Product profile

1.1 General description

Standard level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Avalanche robust
- Suitable for standard level gate drive
- Suitable for thermally demanding environment up to 175°C rating

1.3 Applications

- 12V Motor, lamp and solenoid loads
- High performance automotive power systems
- High performance Pulse Width Modulation (PWM) applications

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1; see Figure 3	[1]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	-	203	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 11; see Figure 12		-	3.4	4	mΩ

Table 1. Quick reference data *...continued*

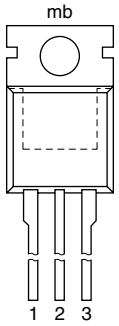
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	292	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 32 V; T_j = 25 °C; see Figure 14; see Figure 13	-	35	-	nC

[1] Continuous current is limited by package.

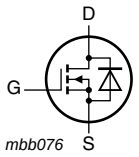
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		



SOT78 (TO-220AB)



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK754R0-40C	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 4. Limiting values

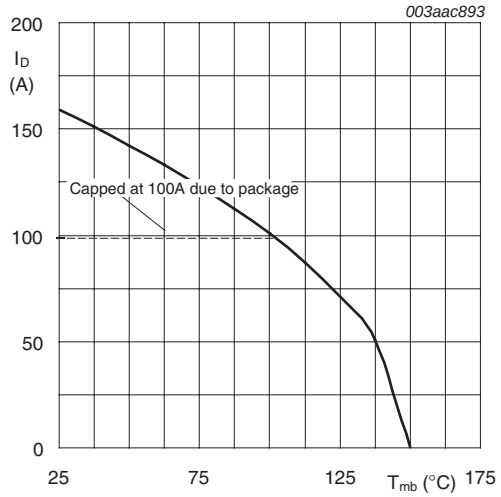
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage		[1]	-20	20	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	[2]	-	159	A
		T_{mb} = 100 °C; V_{GS} = 10 V; see Figure 1	[3]	-	100	A
		T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	[3]	-	100	A
I_{DM}	peak drain current	T_{mb} = 25 °C; $t_p \leq 10$ µs; pulsed; see Figure 3		-	636	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	203	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[3]	-	100	A
			[2]	-	159	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; T_{mb} = 25 °C		-	636	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	292	mJ

[1] -20V accumulated duration not to exceed 168 hrs

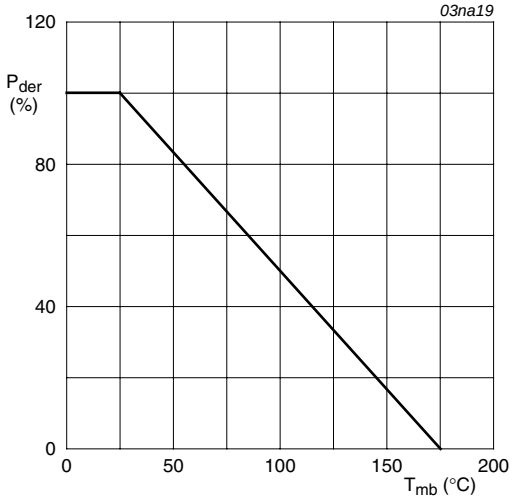
[2] Current is limited by power dissipation chip rating.

[3] Continuous current is limited by package.



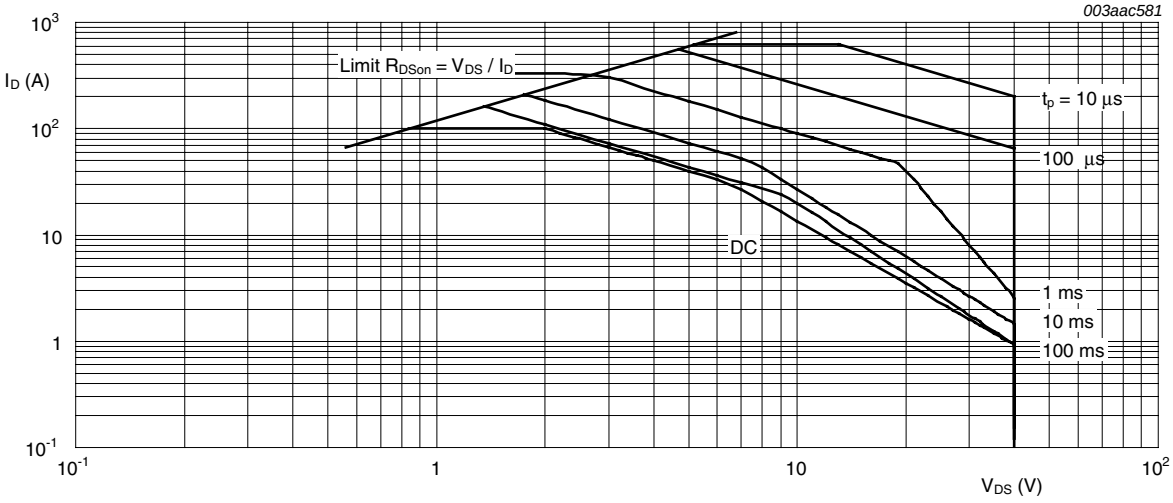
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25°C; I_{DM} \text{is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.74	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	vertical in still air	-	-	60	K/W

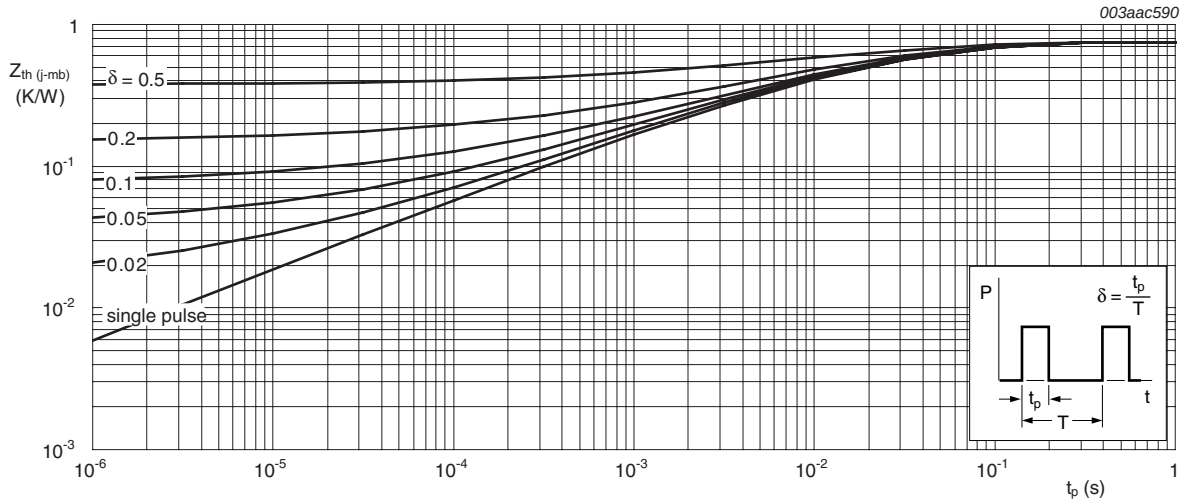
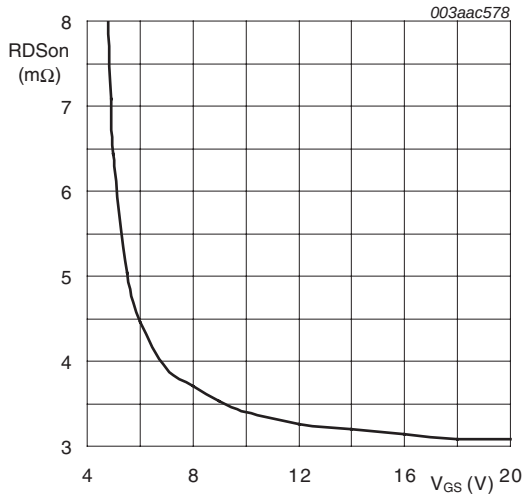


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

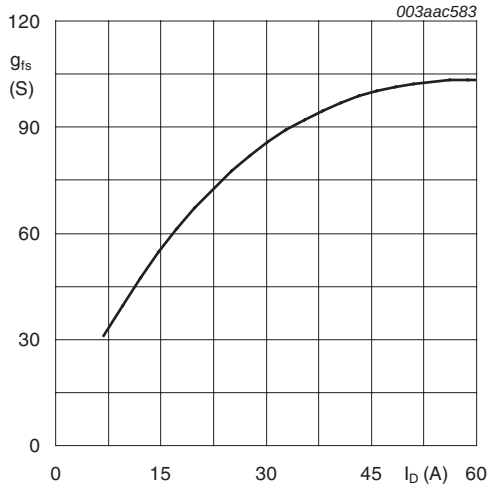
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 11	-	-	8	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 11; see Figure 12	-	3.4	4	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 13; see Figure 14	-	97	-	nC
Q_{GS}	gate-source charge		-	21	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 14; see Figure 13	-	35	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	4391	5708	pF
C_{oss}	output capacitance		-	800	1040	pF
C_{rss}	reverse transfer capacitance		-	535	696	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	40	-	ns
t_r	rise time		-	95	-	ns
$t_{d(off)}$	turn-off delay time		-	129	-	ns
t_f	fall time		-	92	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to centre of die ; T_j = 25 °C	-	4.5	-	nH
		from contact screw on mounting base to centre of die ; T_j = 25 °C	-	3.5	-	nH
L_S	internal source inductance	from source lead to source bond pad ; T_j = 25 °C	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.83	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	44	-	ns
Q_r	recovered charge		-	57	-	nC



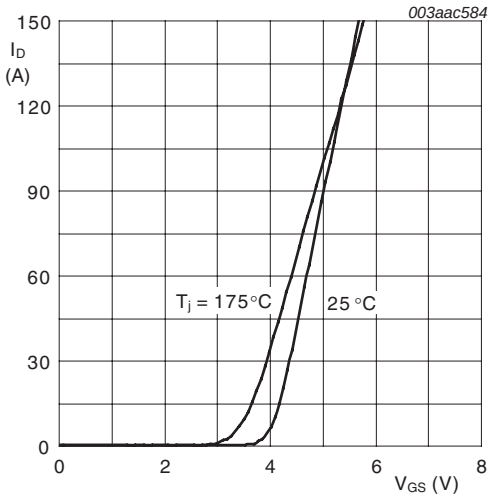
$T_j = 25\,°C; I_D = 25A$

Fig 5. Drain-source on-state resistance as a function of gate voltage; typical values



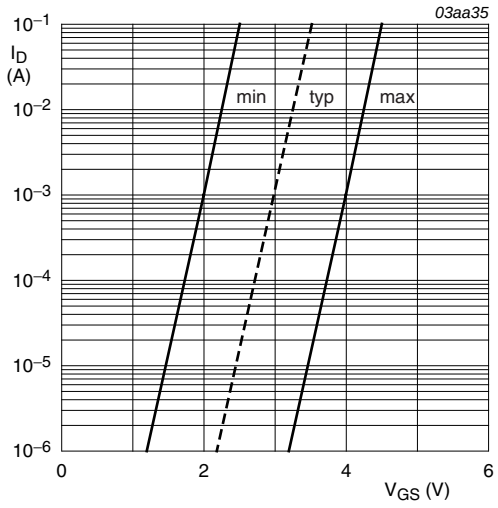
$T_j = 25\,°C; V_{DS} = 25V$

Fig 6. Forward transconductance as a function of drain current; typical values



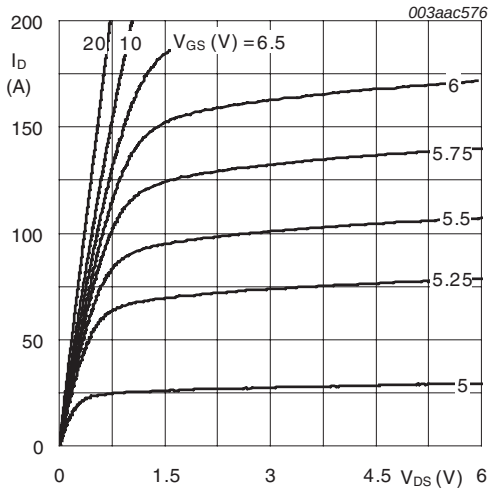
$V_{DS} = 25V$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



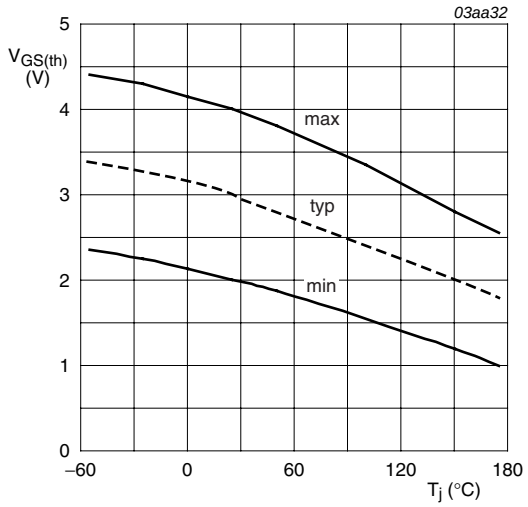
$T_j = 25\,°C; V_{DS} = 5V$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



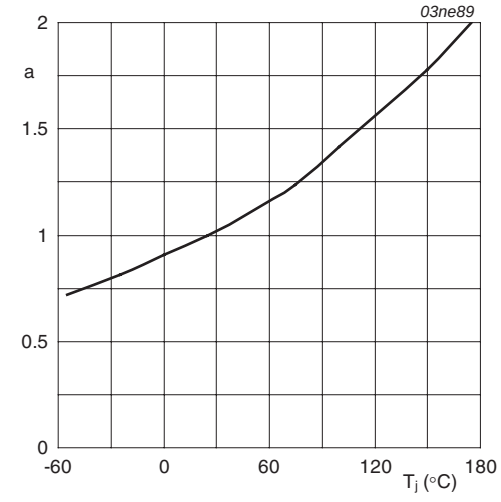
$T_j = 25\,°C$

Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values



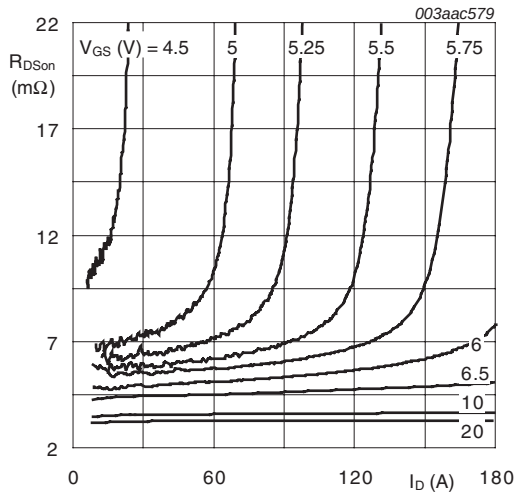
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25\,°C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values

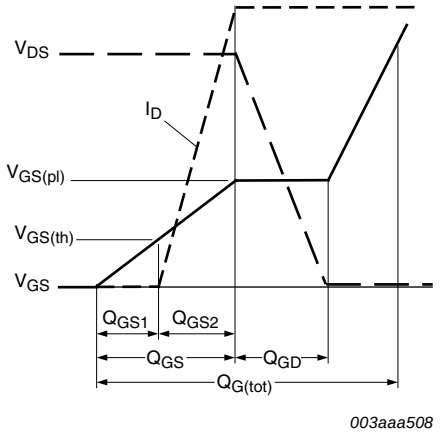
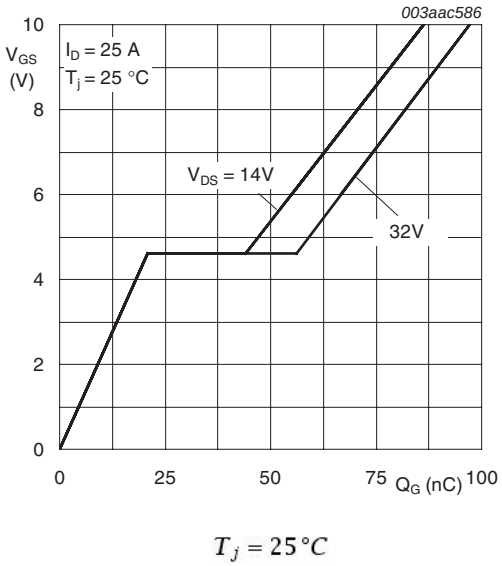
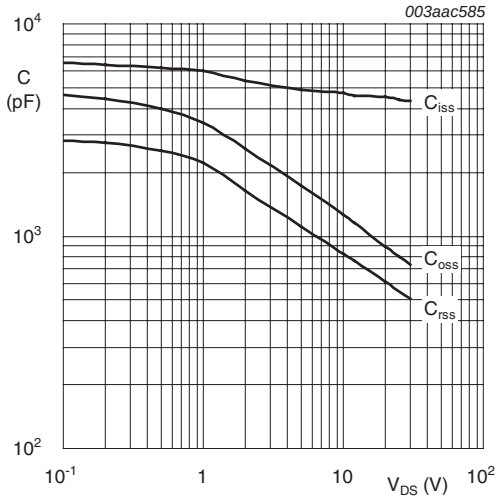


Fig 13. Gate charge waveform definitions



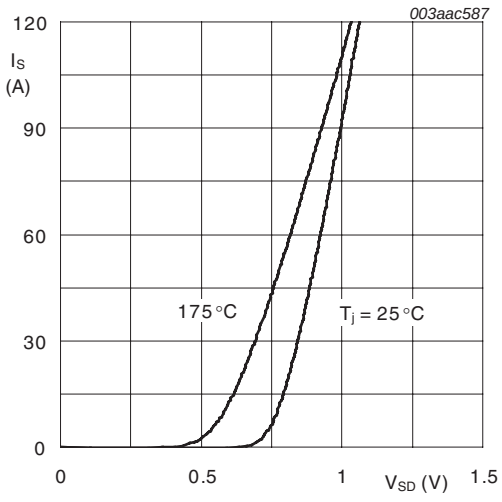
$T_j = 25\,°C$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\,V; f = 1\,MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

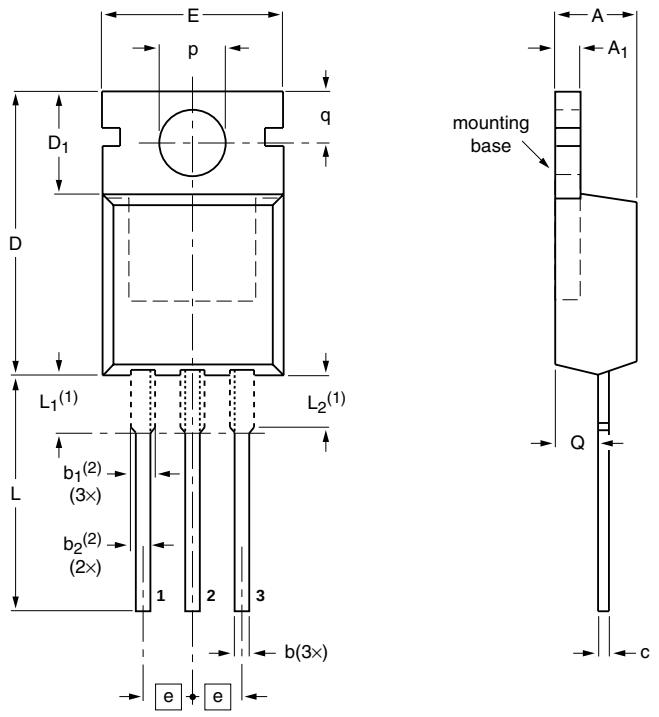


$V_{GS} = 0\,V$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

Fig 17. Package outline SOT78 (TO-220AB)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK754R0-40C v.2	20100720	Product data sheet	-	BUK754R0-40C v.1
Modifications:	• Status changed from preliminary to product. • Various changes to content.			
BUK754R0-40C v.1	20090114	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

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Date of release: 20 July 2010
Document identifier: BUK754R0-40C