

BUK763R6-40C

N-channel TrenchMOS standard level FET

Rev. 04 — 16 June 2010

Product data sheet

1. Product profile

1.1 General description

Standard level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Avalanche robust
- Suitable for standard level gate drive
- Suitable for thermally demanding environment up to 175°C rating

1.3 Applications

- 12V Motor, lamp and solenoid loads
- High performance automotive power systems
- High performance Pulse Width Modulation (PWM) applications



1.4 Quick reference data

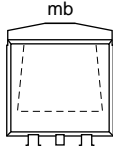
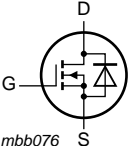
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 1 ; see Figure 3	[1]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	-	203	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 11 ; see Figure 12	-	3	3.6	m Ω
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; unclamped	-	-	292	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 32\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 14 ; see Figure 13	-	35	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK763R6-40C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

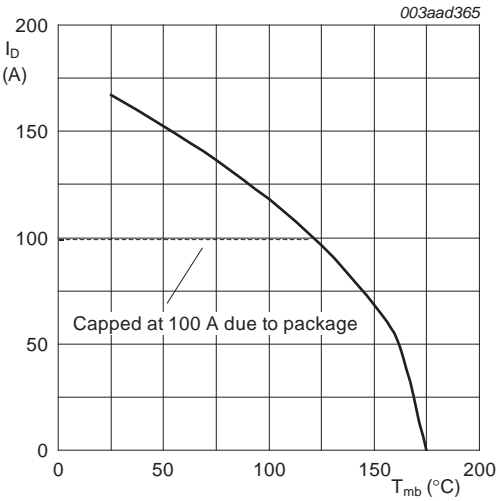
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	40	V	
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	-	40	V	
V _{GS}	gate-source voltage	[1]	-20	-	20	V	
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 ; [2] see Figure 3	-	-	167	A	
		T _{mb} = 100 °C; V _{GS} = 10 V; see Figure 1 [3]	-	-	100	A	
		T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 ; [3] see Figure 3	-	-	100	A	
I _{DM}	peak drain current	T _{mb} = 25 °C; t _p ≤ 10 μs; pulsed; see Figure 3	-	-	668	A	
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	203	W	
T _{stg}	storage temperature		-55	-	175	°C	
T _j	junction temperature		-55	-	175	°C	
Source-drain diode							
I _S	source current	T _{mb} = 25 °C	[3]	-	-	100	A
			[2]	-	-	167	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	-	668	A	
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 100 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	-	-	292	mJ	

[1] -20V accumulated duration not to exceed 168 hrs.

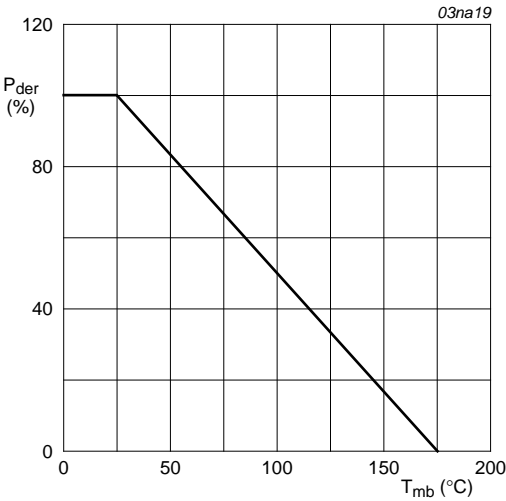
[2] Current is limited by power dissipation chip rating.

[3] Continuous current is limited by package.



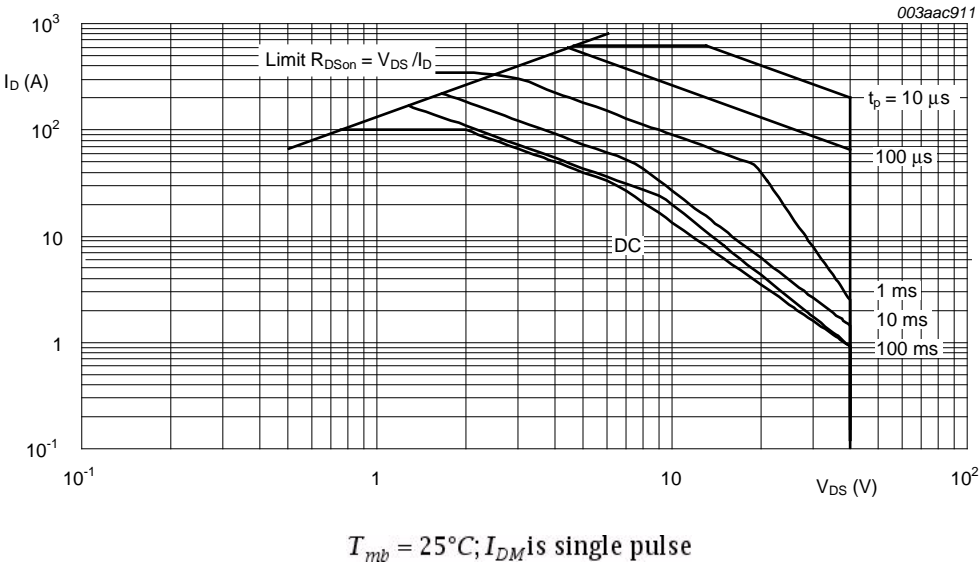
$V_{GS} \geq 10V(1)$ Capped at 100A due to package

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.74	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed circuit board; minimum footprint; SOT404 package	-	-	50	K/W

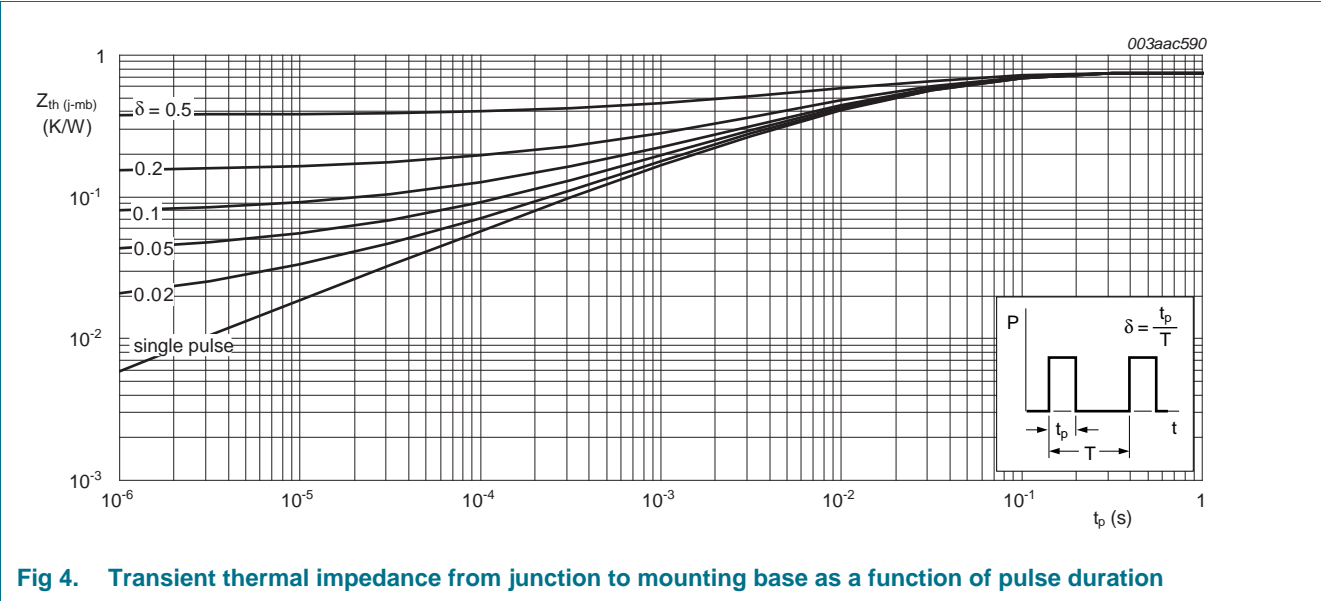
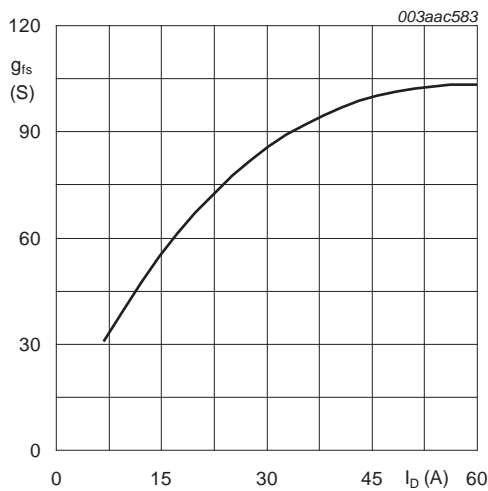


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

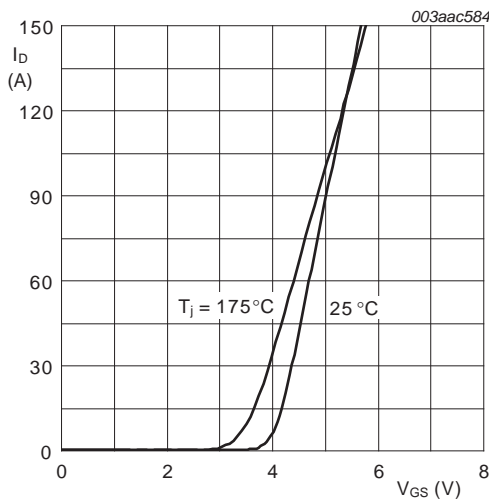
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	40	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10	2	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10	-	-	4.4	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = 20 V; T _j = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = -20 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 11	-	-	7.2	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	3	3.6	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; T _j = 25 °C; see Figure 13 ; see Figure 14	-	97	-	nC
Q _{GS}	gate-source charge		-	21	-	nC
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; T _j = 25 °C; see Figure 14 ; see Figure 13	-	35	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 15	-	4391	5708	pF
C _{oss}	output capacitance		-	800	1040	pF
C _{rss}	reverse transfer capacitance		-	535	696	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	40	-	ns
t _r	rise time		-	95	-	ns
t _{d(off)}	turn-off delay time		-	129	-	ns
t _f	fall time		-	92	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die ; T _j = 25 °C	-	4.5	-	nH
		from contact screw on mounting base to centre of die ; T _j = 25 °C	-	3.5	-	nH
L _S	internal source inductance	from source lead to source bond pad ; T _j = 25 °C	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 16	-	0.83	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = -10 V; V _{DS} = 30 V; T _j = 25 °C	-	44	-	ns
Q _r	recovered charge		-	57	-	nC



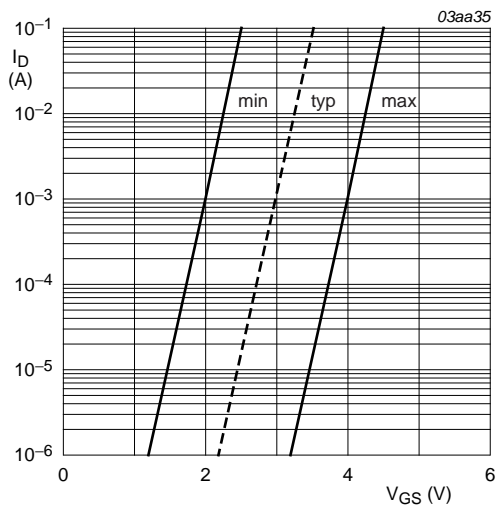
$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 25\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



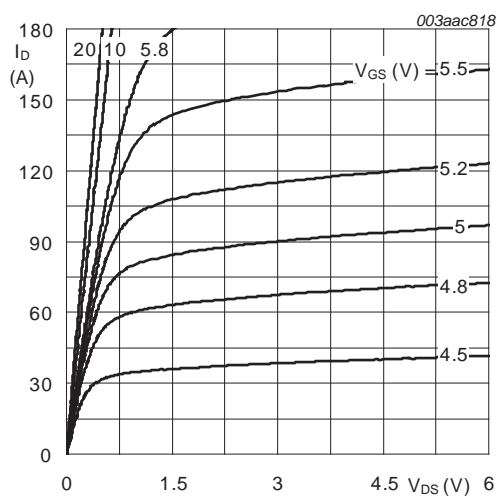
$V_{DS} = 25\text{ V}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



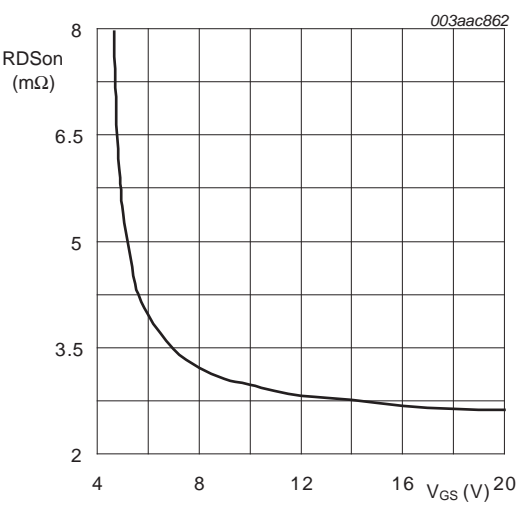
$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



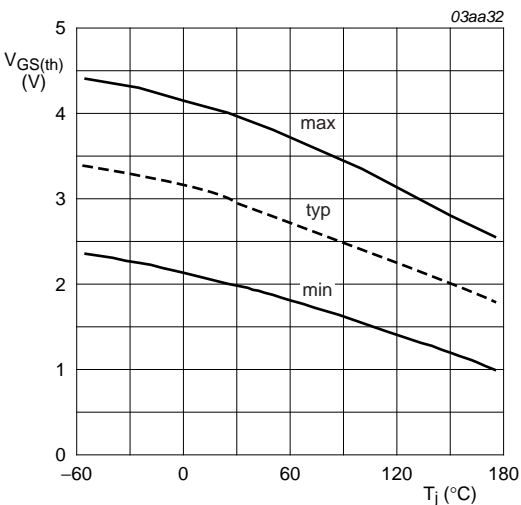
$T_j = 25\text{ }^{\circ}\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



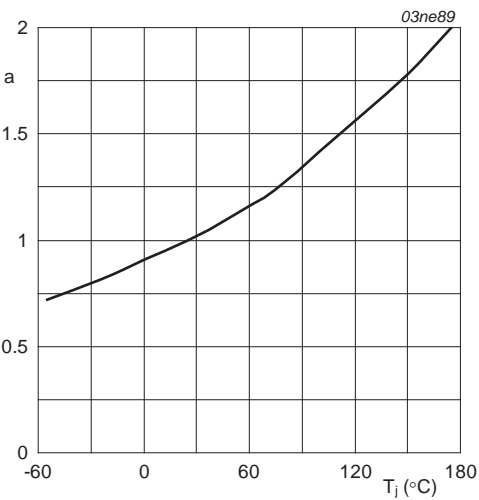
$$T_j = 25^{\circ}\text{C}; I_D = 25\text{A}$$

Fig 9. Drain-source on-state resistance as a function of gate voltage; typical values



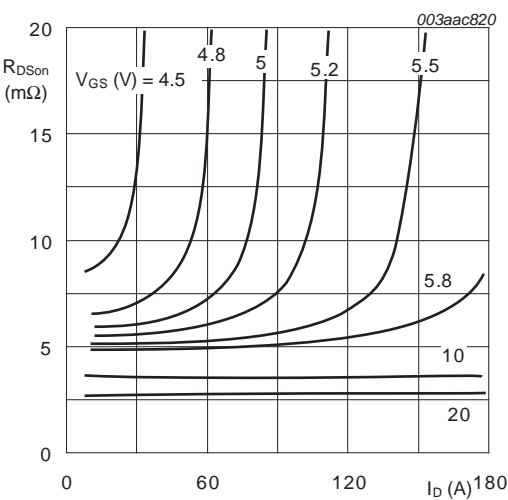
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$$T_j = 25^{\circ}\text{C}$$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values

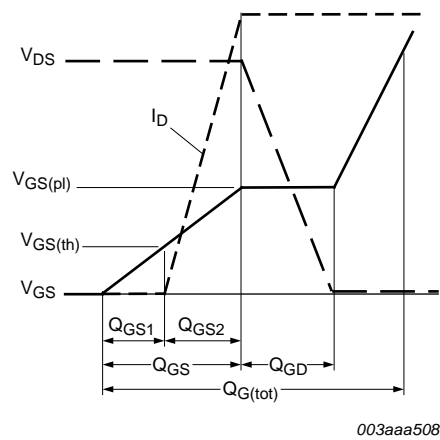


Fig 13. Gate charge waveform definitions

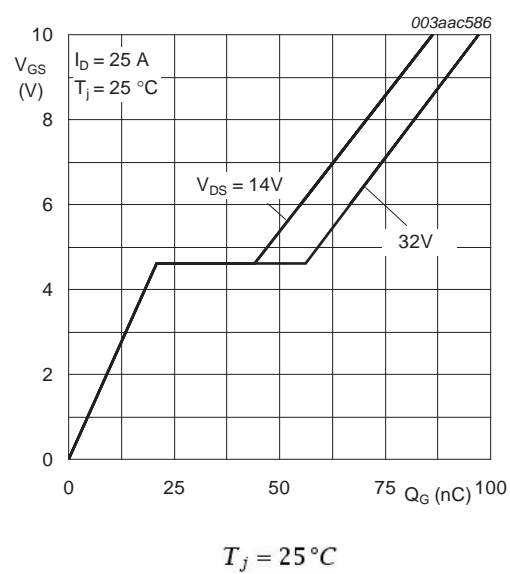


Fig 14. Gate-source voltage as a function of gate charge; typical values

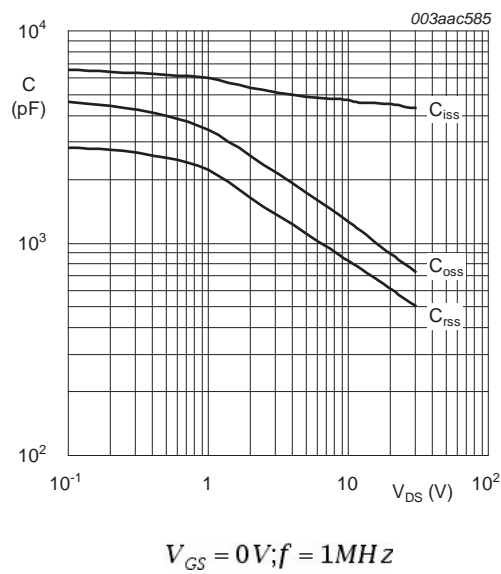


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

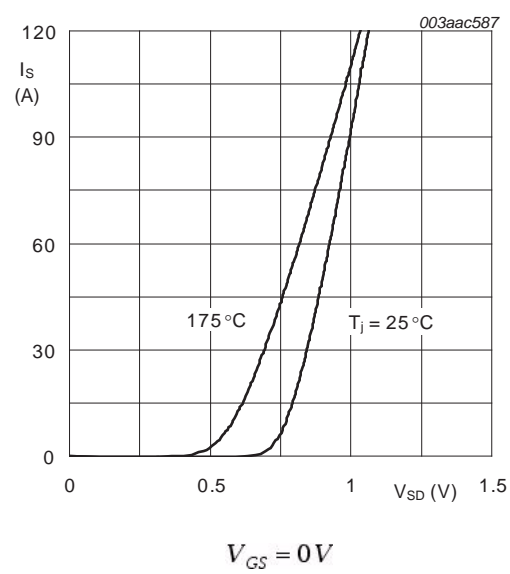


Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

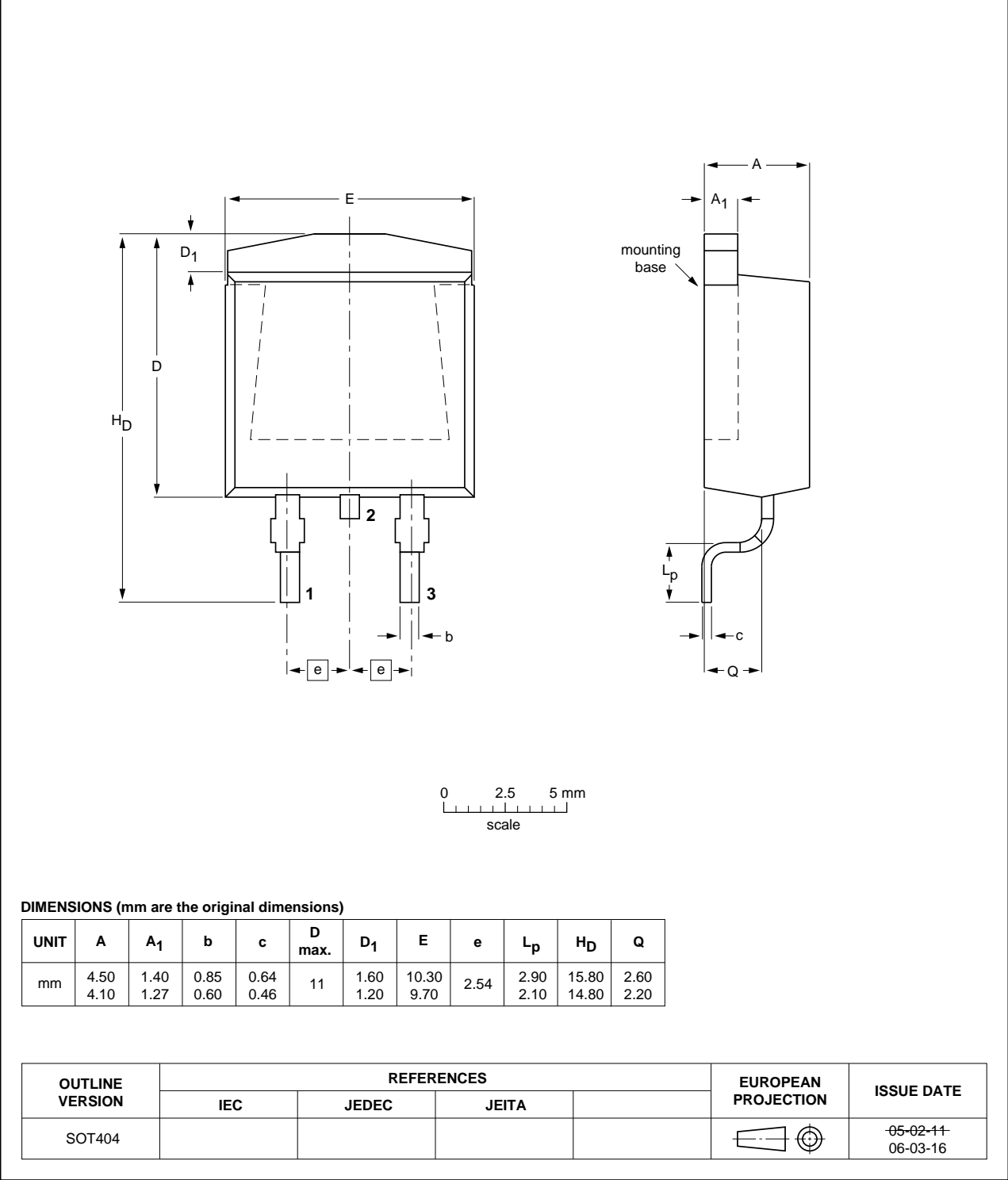


Fig 17. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK763R6-40C v.4	20100616	Product data sheet	-	BUK763R6-40C v.3
Modifications:	• Various changes to content.			
BUK763R6-40C v.3	20100602	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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