

GTL2018

8-bit LVTTTL to GTL transceiver

Rev. 2 — 29 August 2011

Product data sheet

1. General description

The GTL2018 is an octal translating transceiver designed for 3.3 V LVTTTL system interface with a GTL-/GTL/GTL+ bus.

The direction pin (DIR) allows the part to function as either a GTL-to-LVTTTL sampling receiver or as an LVTTTL-to-GTL interface.

The GTL2018 LVTTTL inputs (only) are tolerant up to 5.5 V, allowing direct access to TTL or 5 V CMOS inputs.

2. Features and benefits

- Operates as an octal GTL-/GTL/GTL+ sampling receiver or as an LVTTTL to GTL-/GTL/GTL+ driver
- 3.0 V to 3.6 V operation with 5 V tolerant LVTTTL input
- GTL input and output 3.6 V tolerant
- V_{ref} adjustable from 0.5 V to $0.5V_{CC}$
- Partial power-down permitted
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-CC101
- AEC-Q100 compliance available
- Package offered: TSSOP24

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _i	input capacitance	control inputs; V _I = 3.0 V or 0 V	-	2	2.5	pF
C _{io}	input/output capacitance	A port; V _O = 3.0 V or 0 V	-	4.6	6	pF
		B port; V _O = V _{TT} or 0 V	-	3.4	4.3	pF
GTL; V _{ref} = 0.8 V; V _{TT} = 1.2 V						
t _{PLH}	LOW to HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t _{PHL}	HIGH to LOW propagation delay	An to Bn; see Figure 3	-	3.4	7	ns
t _{PLH}	LOW to HIGH propagation delay	Bn to An; see Figure 4	-	5.2	8	ns
t _{PHL}	HIGH to LOW propagation delay	Bn to An; see Figure 4	-	4.9	7	ns



4. Ordering information

Table 2. Ordering information
 $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Topside mark	Package		
		Name	Description	Version
GTL2018PW	GTL2018PW	TSSOP24	plastic thin shrink small outline package; 24 leads;	SOT355-1
GTL2018PW/Q900			body width 4.4 mm	

[1] GTL2018PW/Q900 is AEC-Q100 compliant. Contact i2c.support@nxp.com for PPAP.

5. Functional diagram

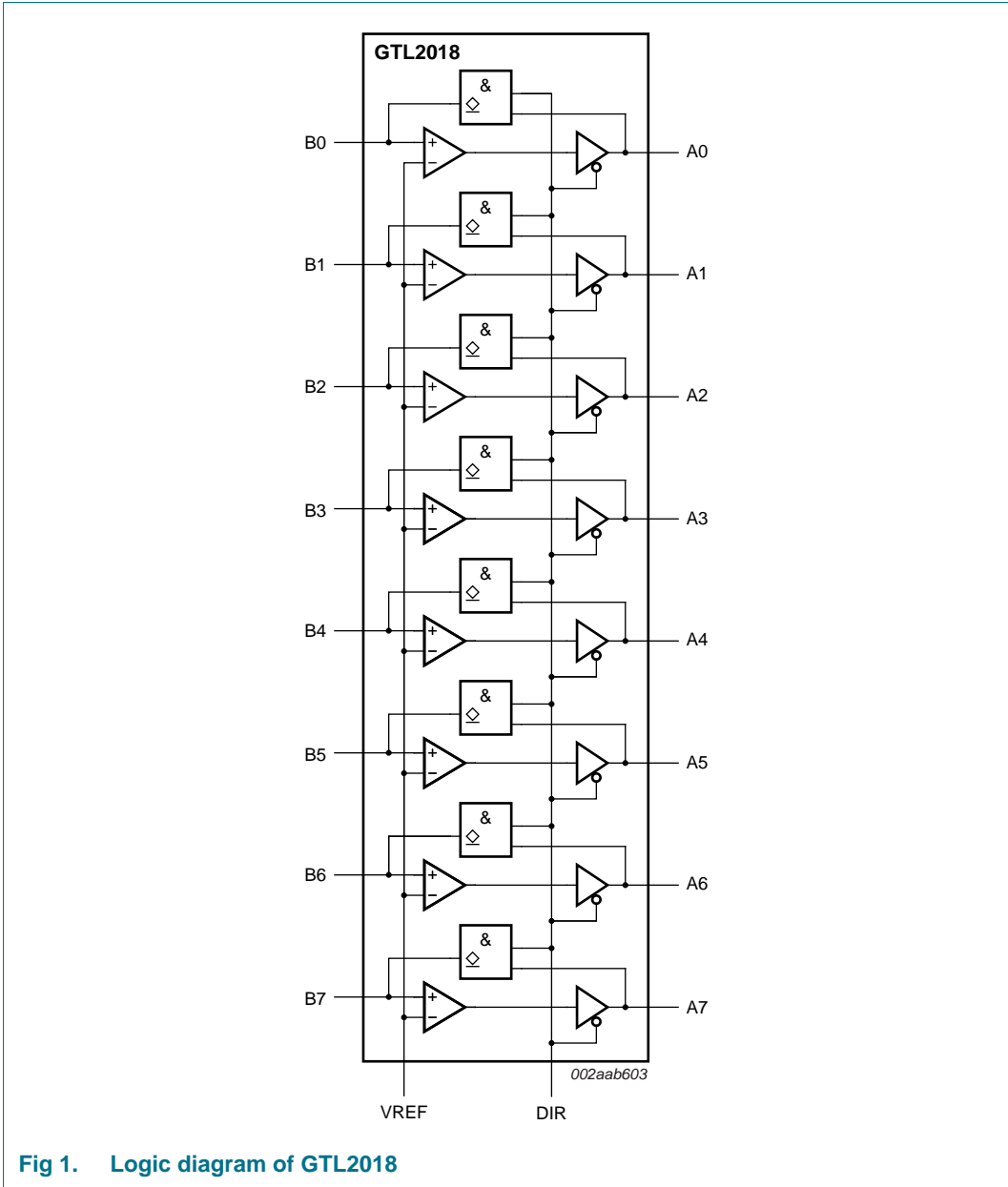
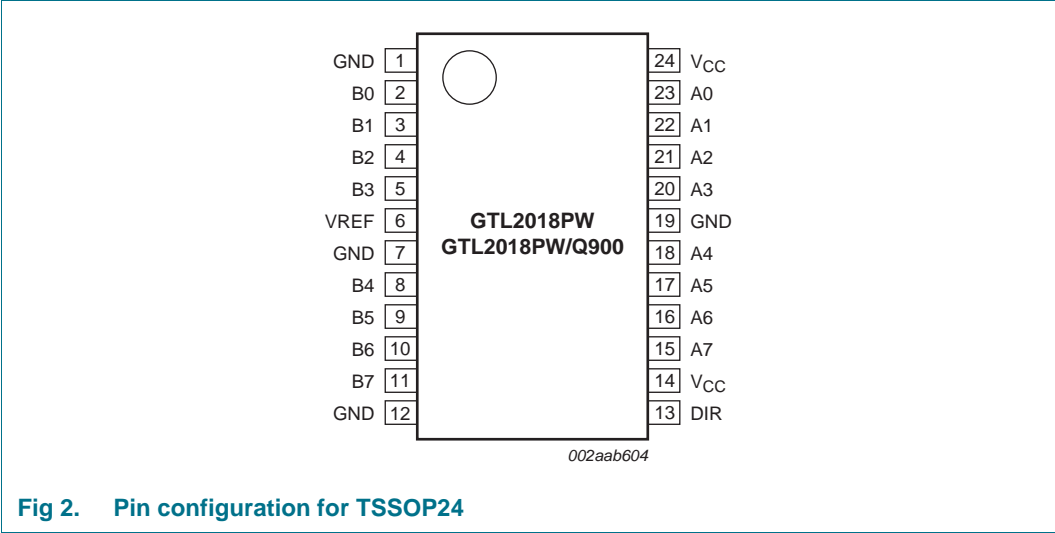


Fig 1. Logic diagram of GTL2018

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1, 7, 12, 19	ground (0 V)
B0	2	data inputs/outputs (B side, GTL)
B1	3	
B2	4	
B3	5	
B4	8	
B5	9	
B6	10	
B7	11	
VREF	6	GTL reference voltage
DIR	13	direction control input (LVTTTL)
V _{CC}	14, 24	positive supply voltage
A7	15	data inputs/outputs (A side, LVTTTL)
A6	16	
A5	17	
A4	18	
A3	20	
A2	21	
A1	22	
A0	23	

7. Functional description

Refer to [Figure 1 “Logic diagram of GTL2018”](#).

7.1 Function table

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Input/output	
DIR	An (LVTTTL)	Bn (GTL)
H	input	Bn = An
L	An = Bn	input

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
V_I	input voltage	A port	-0.5 ^[1]	7.0	V
		B port	-0.5 ^[1]	4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-	-50	mA
V_O	output voltage	output in OFF or HIGH state; A port	-0.5 ^[1]	7.0	V
		output in OFF or HIGH state; B port	-0.5 ^[1]	4.6	V
I_{OL}	LOW-level output current	A port	^[2] -	32	mA
		B port	^[2] -	80	mA
I_{OH}	HIGH-level output current	A port	^[3] -	-32	mA
T_{stg}	storage temperature		^[4] -60	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] Current into any output in the LOW state.

[3] Current into any output in the HIGH state.

[4] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	-	3.6	V
V_{TT}	termination voltage ^[2]	GTL–	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	V
V_{ref}	reference voltage	overall	0.5	$\frac{2}{3}V_{TT}$	$0.5V_{CC}$	V
		GTL–	0.5	0.6	0.63	V
		GTL	0.76	0.8	0.84	V
		GTL+	0.87	1.0	1.10	V
V_I	input voltage	B port	0	V_{TT}	3.6	V
		except B port ^[3]	0	3.3	5.5	V
V_{IH}	HIGH-level input voltage	B port	$V_{ref} + 0.050$	-	-	V
		except B port	2	-	-	V
V_{IL}	LOW-level input voltage	B port	-	-	$V_{ref} - 0.050$	V
		except B port	-	-	0.8	V
I_{OH}	HIGH-level output current	A port	-	-	-16	mA
I_{OL}	LOW-level output current	B port	-	-	40	mA
		A port	-	-	16	mA
T_{amb}	ambient temperature	operating in free air	-40	-	+85	°C

[1] Unused inputs must be held HIGH or LOW to prevent them from floating.

[2] V_{TT} maximum of 3.6 V with resistor sized to so I_{OL} maximum is not exceeded.

[3] A0 to A7 $V_{I(max)}$ is 3.6 V if configured as outputs (DIR = LOW).

10. Static characteristics

Table 7. Static characteristics

Recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{OH}	HIGH-level output voltage	A port; $V_{CC} = 3.0\text{ V}$ to 3.6 V ; $I_{OH} = -100\text{ }\mu\text{A}$	^[2] $V_{CC} - 0.2$	-	-	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OH} = -16\text{ mA}$	^[2] 2.0	-	-	V
V_{OL}	LOW-level output voltage	B port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 40\text{ mA}$	^[2] -	0.23	0.4	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 8\text{ mA}$	^[2] -	0.28	0.4	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 12\text{ mA}$	^[2] -	0.40	0.55	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 16\text{ mA}$	^[2] -	0.55	0.8	V
		A port; $V_{CC} = 3.0\text{ V}$; $I_{OL} = 16\text{ mA}$	^[2] -	0.55	0.8	V
I_I	input current	control inputs; $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND	-	-	± 1	μA
		B port; $V_{CC} = 3.6\text{ V}$; $V_I = V_{TT}$ or GND	-	-	± 1	μA
		A port; $V_{CC} = 0\text{ V}$ or 3.6 V ; $V_I = 5.5\text{ V}$	-	-	10	μA
		A port; $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$	-	-	± 1	μA
		A port; $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$	-	-	-5	μA
I_{OZ}	off-state output current	A port; $V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 3.6 V	-	-	± 100	μA
I_{CC}	supply current	A port; $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ mA}$	-	8	12	mA
		B port; $V_{CC} = 3.6\text{ V}$; $V_I = V_{TT}$ or GND; $I_O = 0\text{ mA}$	-	8	12	mA
ΔI_{CC} ^[3]	additional supply current	per input; A port or control inputs; $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC} - 0.6\text{ V}$	-	-	500	μA
C_i	input capacitance	control inputs; $V_I = 3.0\text{ V}$ or 0 V	-	2	2.5	pF
C_{io}	input/output capacitance	A port; $V_O = 3.0\text{ V}$ or 0 V	-	4.6	6	pF
		B port; $V_O = V_{TT}$ or 0 V	-	3.4	4.3	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

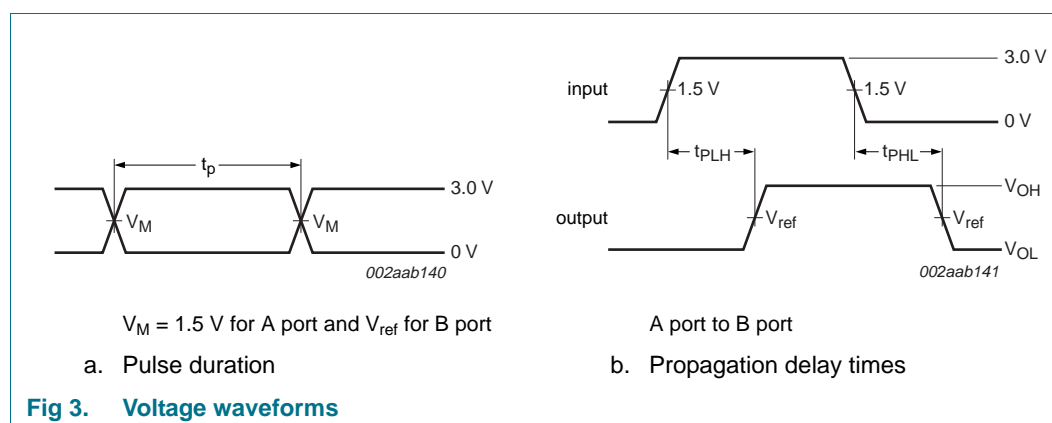
$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$.

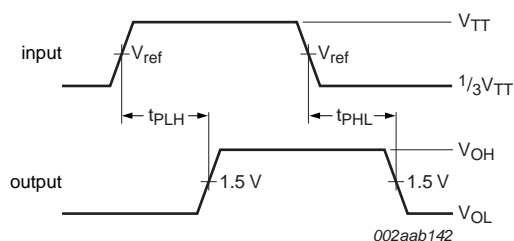
Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
GTL-; $V_{ref} = 0.6 \text{ V}$; $V_{TT} = 0.9 \text{ V}$						
t_{PLH}	LOW to HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn; see Figure 3	-	3.3	7	ns
t_{PLH}	LOW to HIGH propagation delay	Bn to An; see Figure 4	-	5.3	8	ns
t_{PHL}	HIGH to LOW propagation delay	Bn to An; see Figure 4	-	5.2	8	ns
GTL; $V_{ref} = 0.8 \text{ V}$; $V_{TT} = 1.2 \text{ V}$						
t_{PLH}	LOW to HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn; see Figure 3	-	3.4	7	ns
t_{PLH}	LOW to HIGH propagation delay	Bn to An; see Figure 4	-	5.2	8	ns
t_{PHL}	HIGH to LOW propagation delay	Bn to An; see Figure 4	-	4.9	7	ns
GTL+; $V_{ref} = 1.0 \text{ V}$; $V_{TT} = 1.5 \text{ V}$						
t_{PLH}	LOW to HIGH propagation delay	An to Bn; see Figure 3	-	2.8	5	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn; see Figure 3	-	3.4	7	ns
t_{PLH}	LOW to HIGH propagation delay	Bn to An; see Figure 4	-	5.1	8	ns
t_{PHL}	HIGH to LOW propagation delay	Bn to An; see Figure 4	-	4.7	7	ns

[1] All typical values are at $V_{CC} = 3.3 \text{ V}$ and $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

11.1 Waveforms

$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 3.0 \text{ V}$; $V_M = 0.5V_{CC}$ at $V_{CC} \leq 2.7 \text{ V}$ for A ports and control pins;
 $V_M = V_{ref}$ for B ports.





PRR \leq 10 MHz; $Z_o = 50 \Omega$; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns

Fig 4. Propagation delay, Bn to An

12. Test information

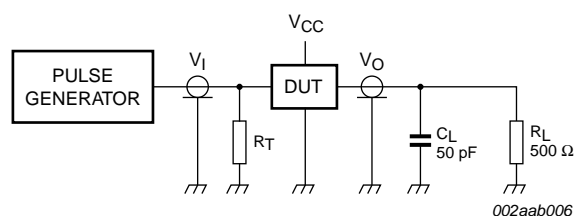
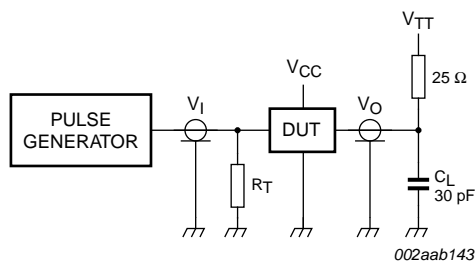


Fig 5. Load circuitry for switching times



R_L = load resistor.

C_L = load capacitance; includes jib and probe capacitance.

R_T = termination resistance; should be equal to Z_o of pulse generators.

Fig 6. Load circuit for B outputs

13. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

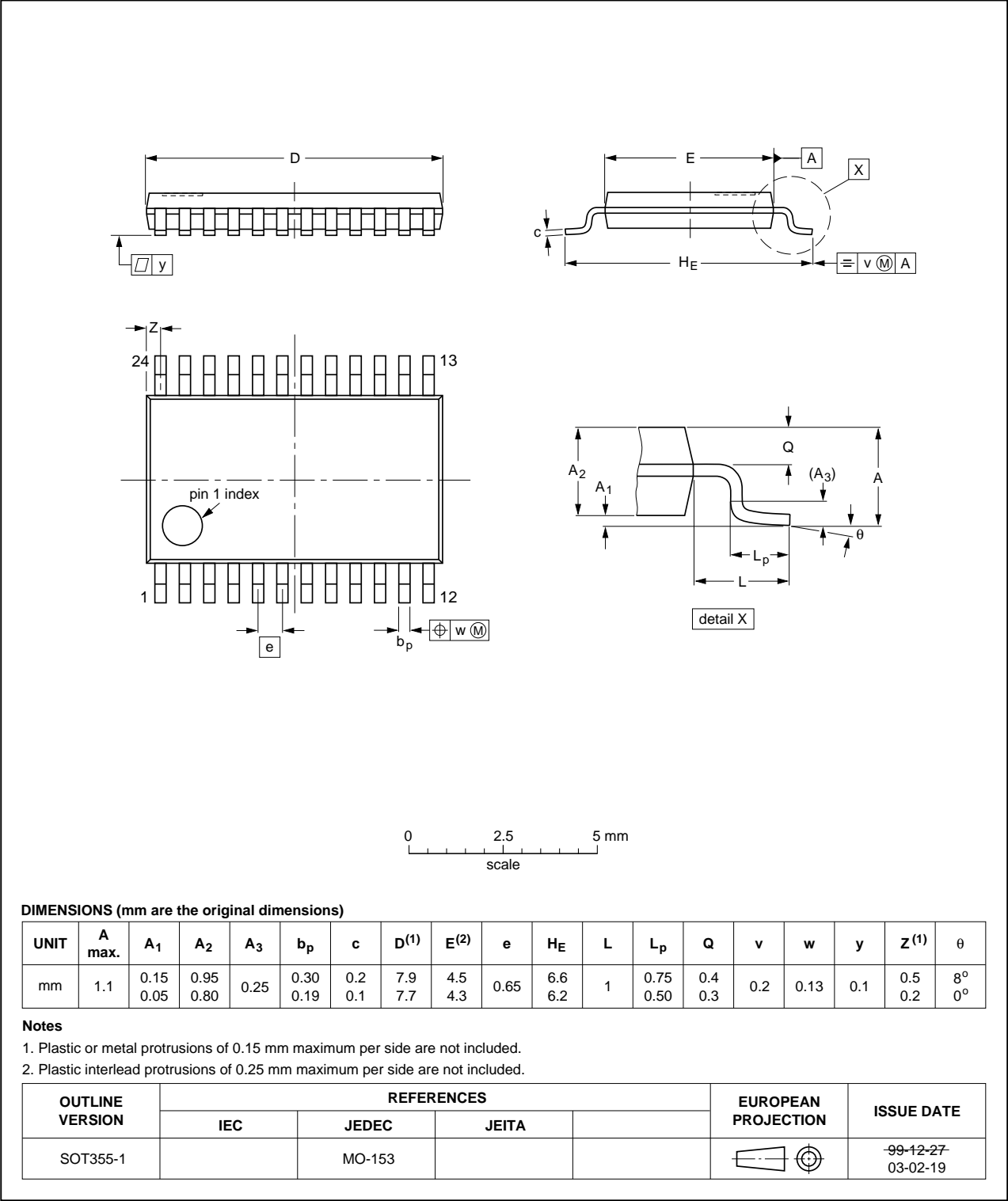


Fig 7. Package outline SOT355-1 (TSSOP24)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 8](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 9](#) and [10](#)

Table 9. SnPb eutectic process (from J-STD-020C)

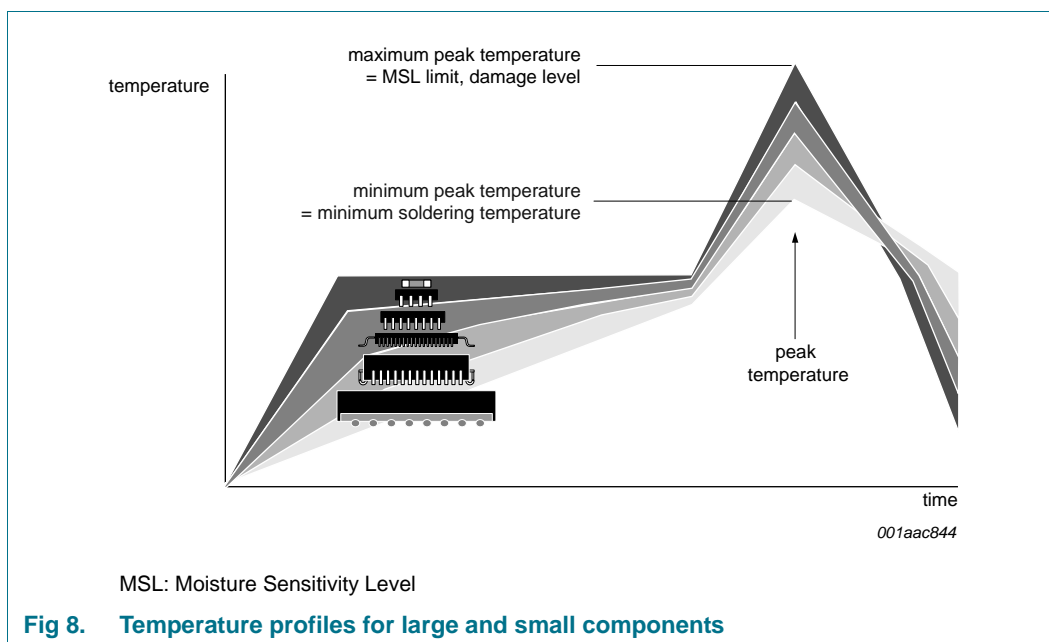
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 8](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTTL	Low Voltage Transistor-Transistor Logic
PRR	Pulse Repetition Rate
TTL	Transistor-Transistor Logic

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2018 v.2	20110829	Product data sheet	-	GTL2018 v.1
Modifications:	<ul style="list-style-type: none">• Section 2 "Features and benefits":<ul style="list-style-type: none">– 6th bullet item corrected from "...exceeds 500 mA per JESD78" to "...exceeds 100 mA per JESD78"– 7th bullet item: removed phrase "200 V MM per JESD22-A115"– added (new) 8th bullet item "AEC-Q100 compliance available"• Table 2 "Ordering information":<ul style="list-style-type: none">– added type number GTL2018PW/Q900– added Table note [1]• Figure 2 "Pin configuration for TSSOP24" modified: added type number GTL2018PW/Q900			
GTL2018 v.1	20070215	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the

product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

19. Contents

1	General description	1
2	Features and benefits	1
3	Quick reference data	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Functional description	4
7.1	Function table	4
8	Limiting values	4
9	Recommended operating conditions	5
10	Static characteristics	6
11	Dynamic characteristics	7
11.1	Waveforms	7
12	Test information	8
13	Package outline	9
14	Soldering of SMD packages	10
14.1	Introduction to soldering	10
14.2	Wave and reflow soldering	10
14.3	Wave soldering	10
14.4	Reflow soldering	11
15	Abbreviations	12
16	Revision history	13
17	Legal information	14
17.1	Data sheet status	14
17.2	Definitions	14
17.3	Disclaimers	14
17.4	Trademarks	15
18	Contact information	15
19	Contents	16

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 29 August 2011

Document identifier: GTL2018