

# HEF4894B

## 12-stage shift-and-store register LED driver

Rev. 8 — 22 November 2011

Product data sheet

### 1. General description

The HEF4894B is a 12-stage serial shift register. It has a storage latch associated with each stage for strobing data from the serial input (D) to the parallel LED driver outputs (QP0 to QP11). Data is shifted on positive-going clock (CP) transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the output whenever the output enable (OE) input signal is HIGH.

Two serial outputs (QS1 and QS2) are available for cascading a number of HEF4894B devices. Serial data is available at QS1 on positive-going clock edges to allow high-speed operation in cascaded systems with a fast clock rise time. The same serial data is available at QS2 on the next negative going clock edge. This is used for cascading HEF4894B devices when the clock has a slow rise time.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

Type number	Package		
	Name	Description	Version
HEF4894BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
HEF4894BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
HEF4894BTT	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1



### 4. Functional diagram

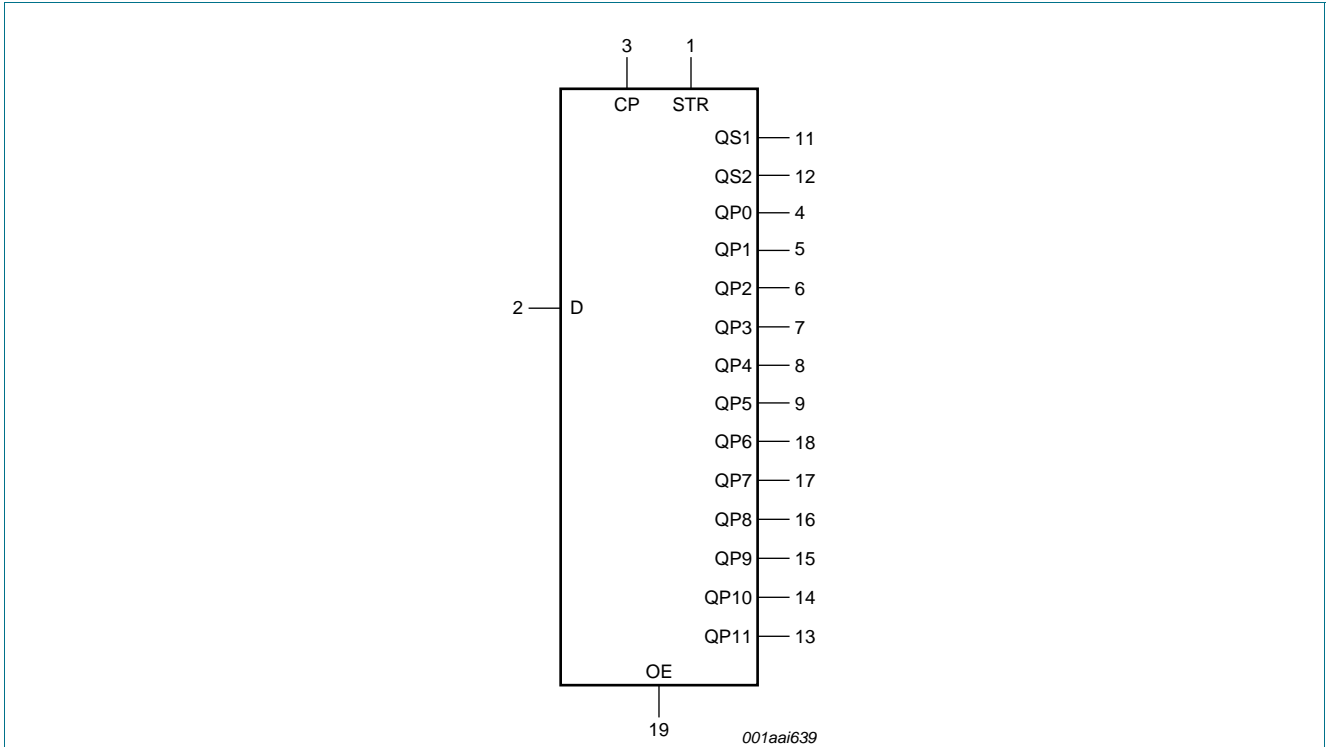


Fig 1. Logic Symbol

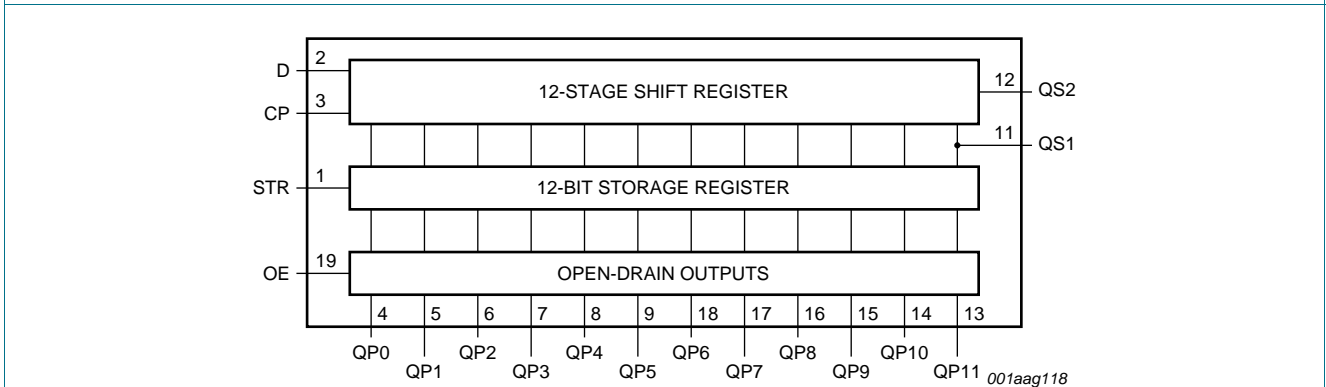


Fig 2. Functional diagram

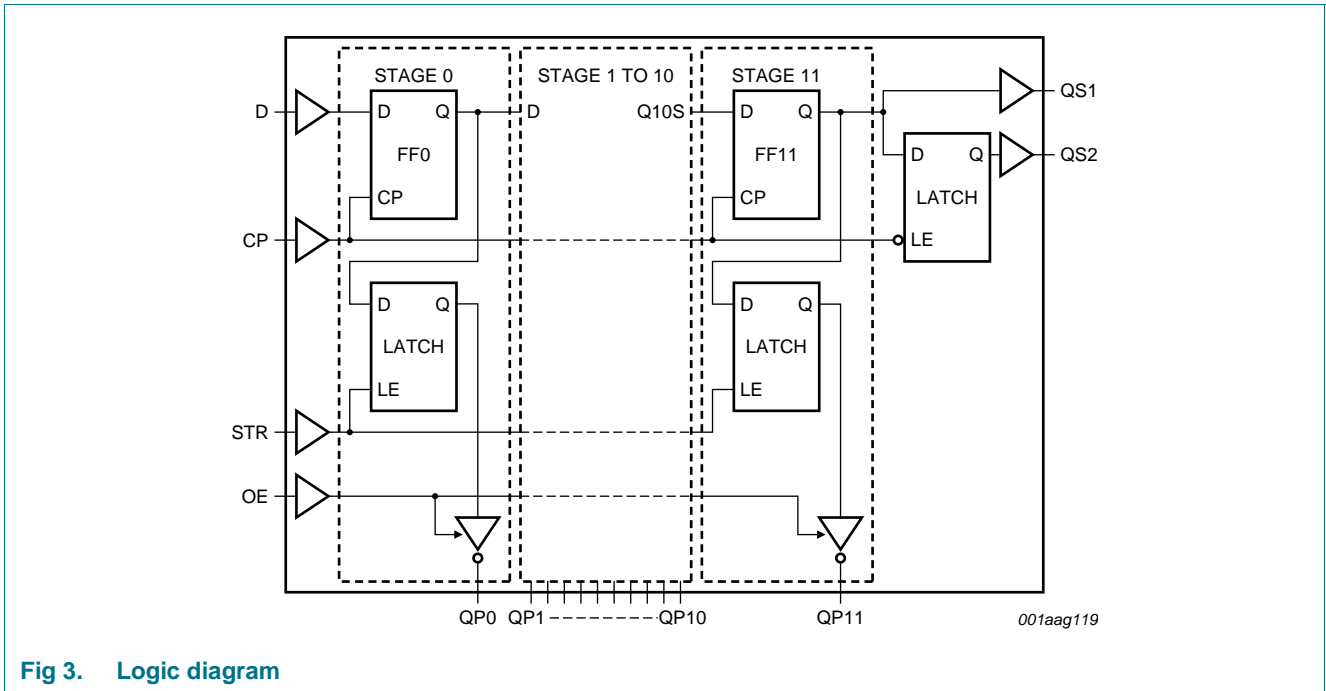


Fig 3. Logic diagram

## 5. Pinning information

### 5.1 Pinning

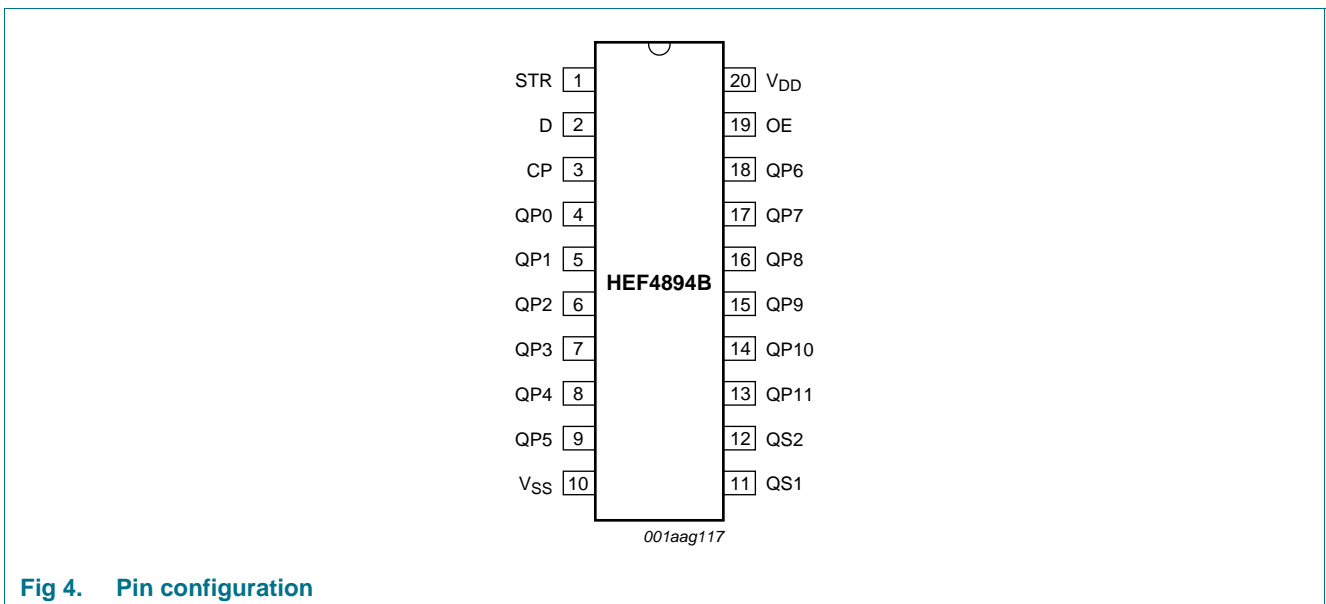


Fig 4. Pin configuration

## 5.2 Pin description

**Table 2.** Pin description

Symbol	Pin	Description
D	2	serial input
QP0 to QP11	4, 5, 6, 7, 8, 9, 18, 17, 16, 15, 14, 13	parallel output
QS1	11	serial output
QS2	12	serial output
CP	3	clock input
STR	1	strobe input
OE	19	output enable input
V <sub>DD</sub>	20	supply voltage
V <sub>SS</sub>	10	ground (0 V)

## 6. Functional description

**Table 3.** Function table<sup>[1]</sup>

At the positive clock edge the information in the 10<sup>th</sup> register stage is transferred to the 11<sup>th</sup> register stage and the QS output

Control			Input	Parallel output		Serial output	
CP	OE	STR	D	QP0	QPn	QS1 <sup>[2]</sup>	QS2 <sup>[3]</sup>
↑	L	X	X	Z	Z	Q10S	no change
↓	L	X	X	Z	Z	no change	Q11S
↑	H	L	X	no change	no change	Q10S	no change
↑	H	H	L	Z	QPn – 1	Q10S	no change
↑	H	H	H	L	QPn – 1	Q10S	no change
↓	H	H	H	no change	no change	no change	Q11S

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition; Z = high-impedance OFF-state.

[2] Q10S = the data in register stage 10 before the LOW to HIGH clock transition.

[3] Q11S = the data in register stage 11 before the HIGH to LOW clock transition.

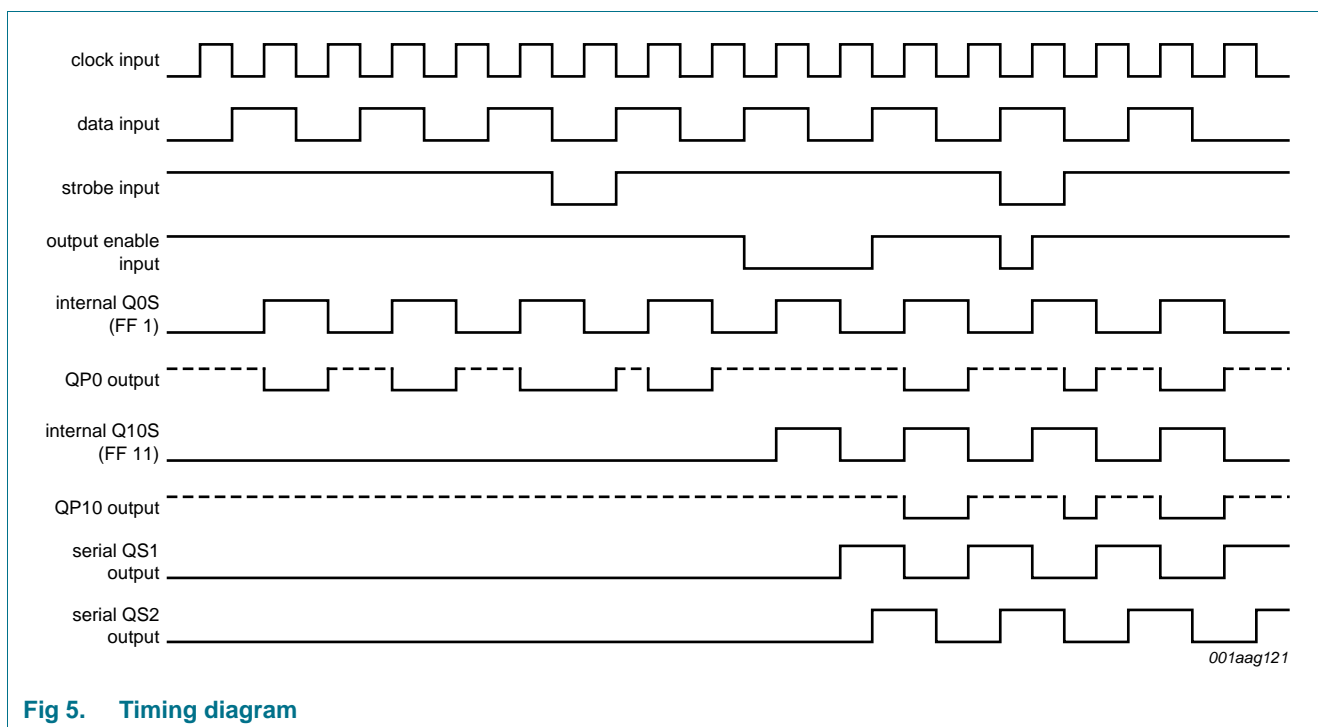


Fig 5. Timing diagram

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	QSn outputs; $V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
		QPn outputs; $V_O < 0.5\text{ V}$	-	40	mA
$I_I$	input leakage current		-	$\pm 10$	mA
$I_O$	output current	QSn outputs	-	$\pm 10$	mA
		QPn outputs	-	40	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		DIP20 package	[1] -	750	mW
		SO20 package	[2] -	500	mW
		TSSOP20 package	[3] -	500	mW
P	power dissipation	per output	-	100	mW

[1] For DIP20 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[2] For SO20 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

[3] For TSSOP20 package:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		$T_{amb} = +125\text{ °C}$		Unit	
				Min	Max	Min	Max	Min	Max	Min	Max		
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V	
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V	
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V	
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V	
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V	
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V	
$V_{OH}$	HIGH-level output voltage	QSn outputs; $ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V	
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V	
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V	
$V_{OL}$	LOW-level output voltage	QSn outputs; $ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V	
		QPn outputs; $ I_O  < 20\text{ mA}$	5 V	-	0.75	-	0.75	-	1.5	-	1.5	V	
			10 V	-	0.75	-	0.75	-	1.5	-	1.5	V	
			15 V	-	0.75	-	0.75	-	1.5	-	1.5	V	
$I_{OH}$	HIGH-level output current	QSn outputs	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
			$V_O = 4.6\text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
			$V_O = 9.5\text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
			$V_O = 13.5\text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
$I_{OL}$	LOW-level output current	QSn outputs	$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
			$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
			$V_O = 1.5\text{ V}$	15 V	4.2	-	3.2	-	2.4	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.1$	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$	

**Table 6. Static characteristics ...continued**  
 $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = +25\text{ }^{\circ}\text{C}$		$T_{amb} = +85\text{ }^{\circ}\text{C}$		$T_{amb} = +125\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$I_{OZ}$	OFF-state output current	QPn output is HIGH; $V_O = 15\text{ V}$	5 V	-	2	-	2	-	15	-	15	$\mu\text{A}$
			10 V	-	2	-	2	-	15	-	15	$\mu\text{A}$
			15 V	-	2	-	2	-	15	-	15	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	5	-	5	-	150	-	150	$\mu\text{A}$
			10 V	-	10	-	10	-	300	-	300	$\mu\text{A}$
			15 V	-	20	-	20	-	600	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	-	-	pF	

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**  
 $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified. For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	CP to QS1; see <a href="#">Figure 6</a>	5 V	<a href="#">[1]</a> $132\text{ ns} + (0.55\text{ ns/pF})C_L$	-	160	320	ns
			10 V	$53\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF})C_L$	-	45	90	ns
		CP to QS2; see <a href="#">Figure 6</a>	5 V	$92\text{ ns} + (0.55\text{ ns/pF})C_L$	-	120	240	ns
			10 V	$39\text{ ns} + (0.23\text{ ns/pF})C_L$	-	50	100	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
$t_{PLH}$	LOW to HIGH propagation delay	CP to QS1; see <a href="#">Figure 6</a>	5 V	<a href="#">[1]</a> $102\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$44\text{ ns} + (0.23\text{ ns/pF})C_L$	-	55	110	ns
			15 V	$32\text{ ns} + (0.16\text{ ns/pF})C_L$	-	40	80	ns
		CP to QS2; see <a href="#">Figure 6</a>	5 V	$102\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$49\text{ ns} + (0.23\text{ ns/pF})C_L$	-	60	120	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF})C_L$	-	45	90	ns
$t_{PZL}$	OFF-state to LOW propagation delay	CP to QPn; see <a href="#">Figure 6</a>	5 V		-	240	480	ns
			10 V		-	80	160	ns
			15 V		-	55	110	ns
		STR to QPn; see <a href="#">Figure 7</a>	5 V		-	140	280	ns
			10 V		-	70	140	ns
			15 V		-	55	110	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	CP to QPn; see <a href="#">Figure 6</a> and <a href="#">7</a>	5 V		-	170	340	ns
			10 V		-	75	150	ns
			15 V		-	60	120	ns
		STR to QPn; see <a href="#">Figure 7</a>	5 V		-	100	200	ns
			10 V		-	40	100	ns
			15 V		-	35	70	ns

**Table 7. Dynamic characteristics ...continued**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$  unless otherwise specified. For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Typ	Max	Unit	
t <sub>en</sub>		OE to QPn; see <a href="#">Figure 8</a>	5 V	[2]	-	100	200	ns	
			10 V		-	55	110	ns	
			15 V		-	50	100	ns	
t <sub>dis</sub>		OE to QPn; see <a href="#">Figure 8</a>	5 V	[2]	-	80	160	ns	
			10 V		-	40	80	ns	
			15 V		-	30	60	ns	
t <sub>t</sub>	transition time	QS1, QS2; see <a href="#">Figure 6</a>	5 V	[1][3]		85	170	ns	
			10 V		$35\text{ ns} + (1.00\text{ ns/pF})C_L$	-	40	80	ns
			15 V		$19\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
t <sub>w</sub>	pulse width	CP; LOW and HIGH; see <a href="#">Figure 6</a>	5 V		60	30	-	ns	
			10 V		30	15	-	ns	
			15 V		24	12	-	ns	
		STR; HIGH; see <a href="#">Figure 7</a>	5 V		80	40	-	ns	
			10 V		60	30	-	ns	
			15 V		24	12	-	ns	
t <sub>su</sub>	set-up time	D to CP; see <a href="#">Figure 9</a>	5 V		60	30	-	ns	
			10 V		20	10	-	ns	
			15 V		15	5	-	ns	
t <sub>h</sub>	hold time	D to CP; see <a href="#">Figure 9</a>	5 V		+5	-15	-	ns	
			10 V		20	5	-	ns	
			15 V		20	5	-	ns	
f <sub>clk(max)</sub>	maximum clock frequency	CP; see <a href="#">Figure 6</a>	5 V		5	10	-	MHz	
			10 V		11	22	-	MHz	
			15 V		14	28	-	MHz	

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C<sub>L</sub> in pF).

[2] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>dis</sub> is the same as t<sub>PLZ</sub>.

[3] t<sub>t</sub> is the same as t<sub>TLH</sub> and t<sub>THL</sub>.

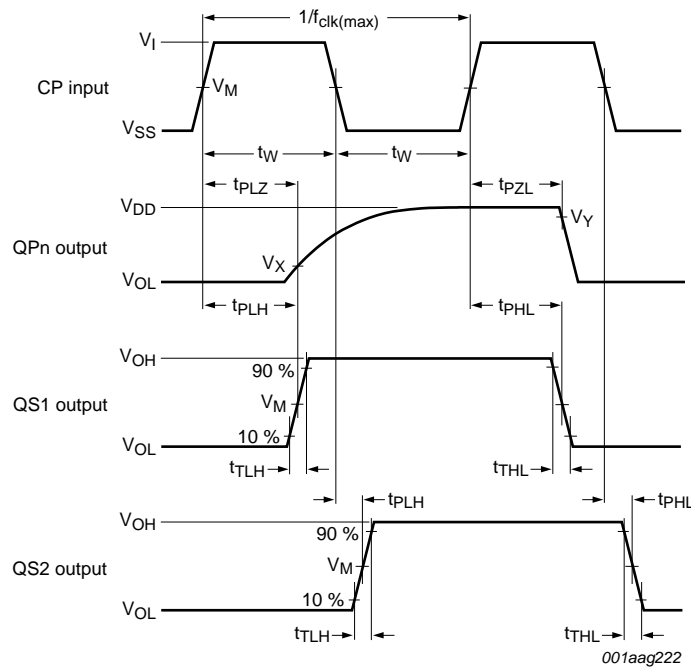
**Table 8. Dynamic power dissipation**

P<sub>D</sub> can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	V <sub>DD</sub>	Typical formula	Where
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 1200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ \mu\text{W}$	f <sub>i</sub> = input frequency in MHz; f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF; Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs; V <sub>DD</sub> = supply voltage in V.
		10 V	$P_D = 5550 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ \mu\text{W}$	
		15 V	$P_D = 15000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ \mu\text{W}$	



11. Waveforms

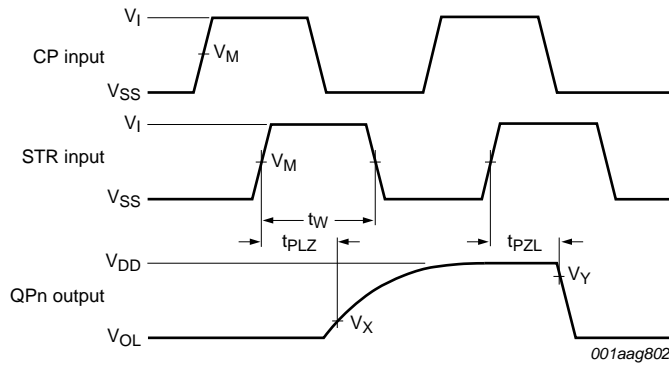


Parallel output measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. Propagation delay clock (CP) to output (QPn, QS1, QS2), clock pulse width and maximum clock frequency**

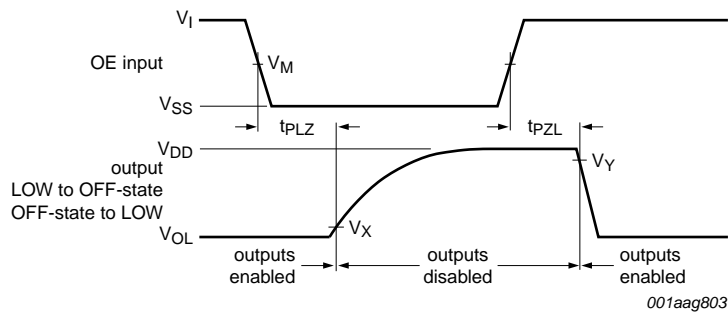
**Table 9. Measurement points**

Supply	Input	Output		
$V_{DD}$	$V_M$	$V_M$	$V_X$	$V_Y$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_O$	$0.9V_O$



Measurement points are given in [Table 9](#).  
 $V_{OL}$  is the typical output voltage level that occurs with the output load.

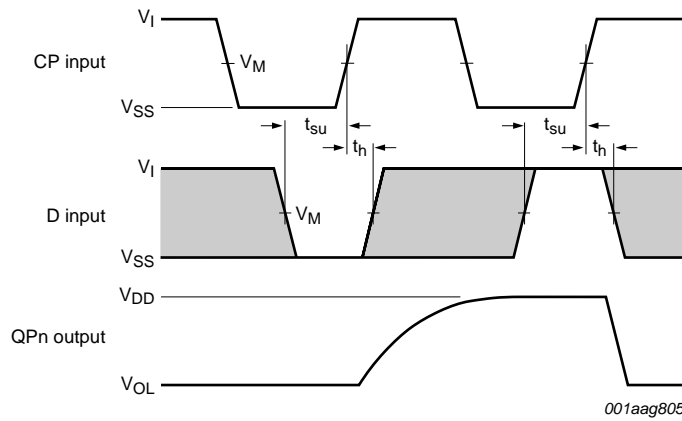
**Fig 7. Strobe (STR) to output (QPn) propagation delays and the strobe pulse width**



Measurement points are given in [Table 9](#).

$V_{OL}$  is the typical output voltage level that occurs with the output load.

**Fig 8. Enable and disable times for input OE**

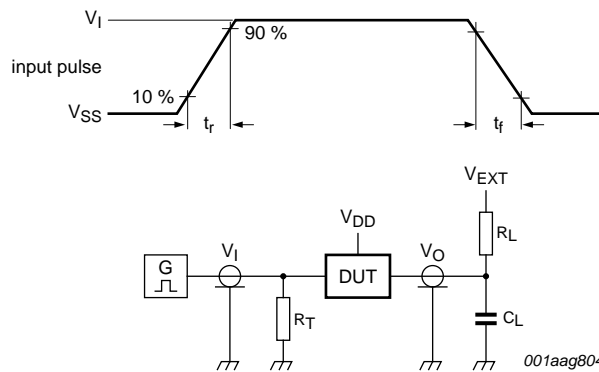


Measurement points are given in [Table 9](#).

$V_{OL}$  is a typical output voltage level that occurs with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 9. Set-up and hold times for the data input (D)**



Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test;

$R_L$  = Load resistance;

$C_L$  = load capacitance;

$R_T$  = Termination resistance should be equal to output impedance of  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 10. Test circuit for measuring switching times**

**Table 10. Test data**

Supply	Input		$V_{EXT}$		Load	
$V_{DD}$	$V_I$	$t_r, t_f$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$	$C_L$	$R_L$
5 V to 15 V	$V_{DD}$	$\leq 20$ ns	$V_{DD}$	open	50 pF	1 k $\Omega$

## 12. Application information

Application example: serial-to-parallel data converting LED driver.

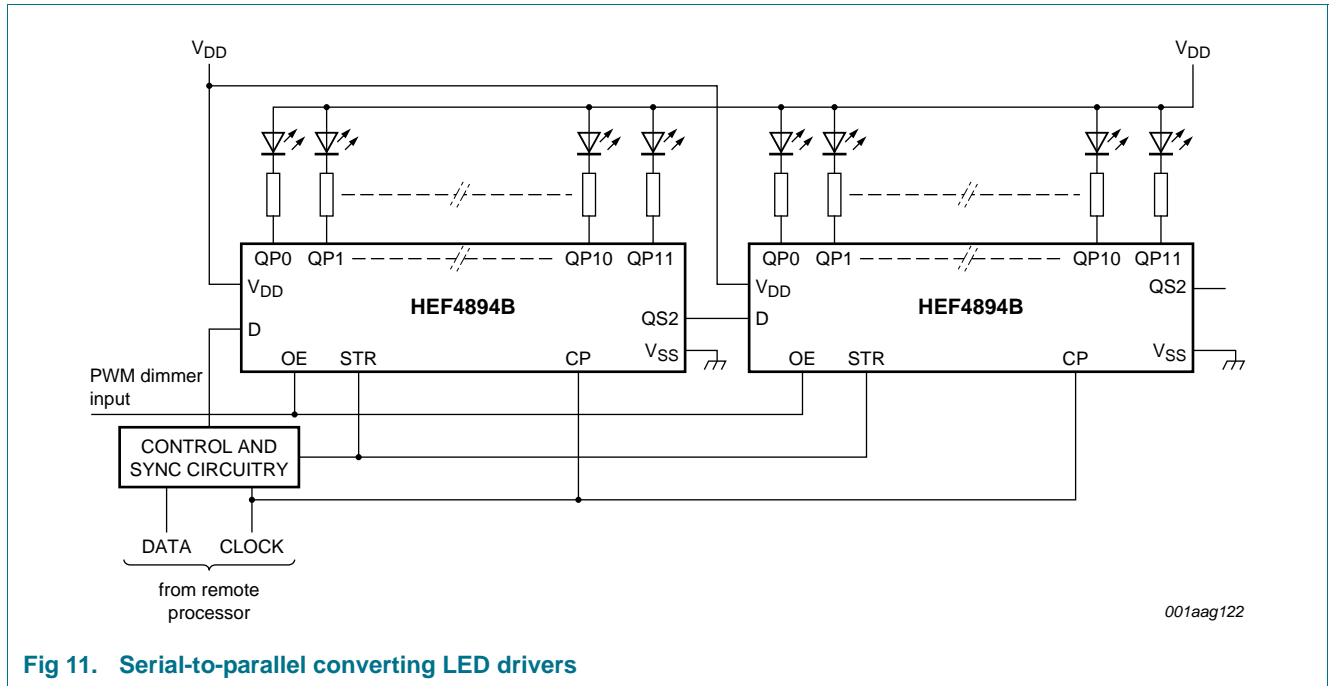


Fig 11. Serial-to-parallel converting LED drivers

13. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

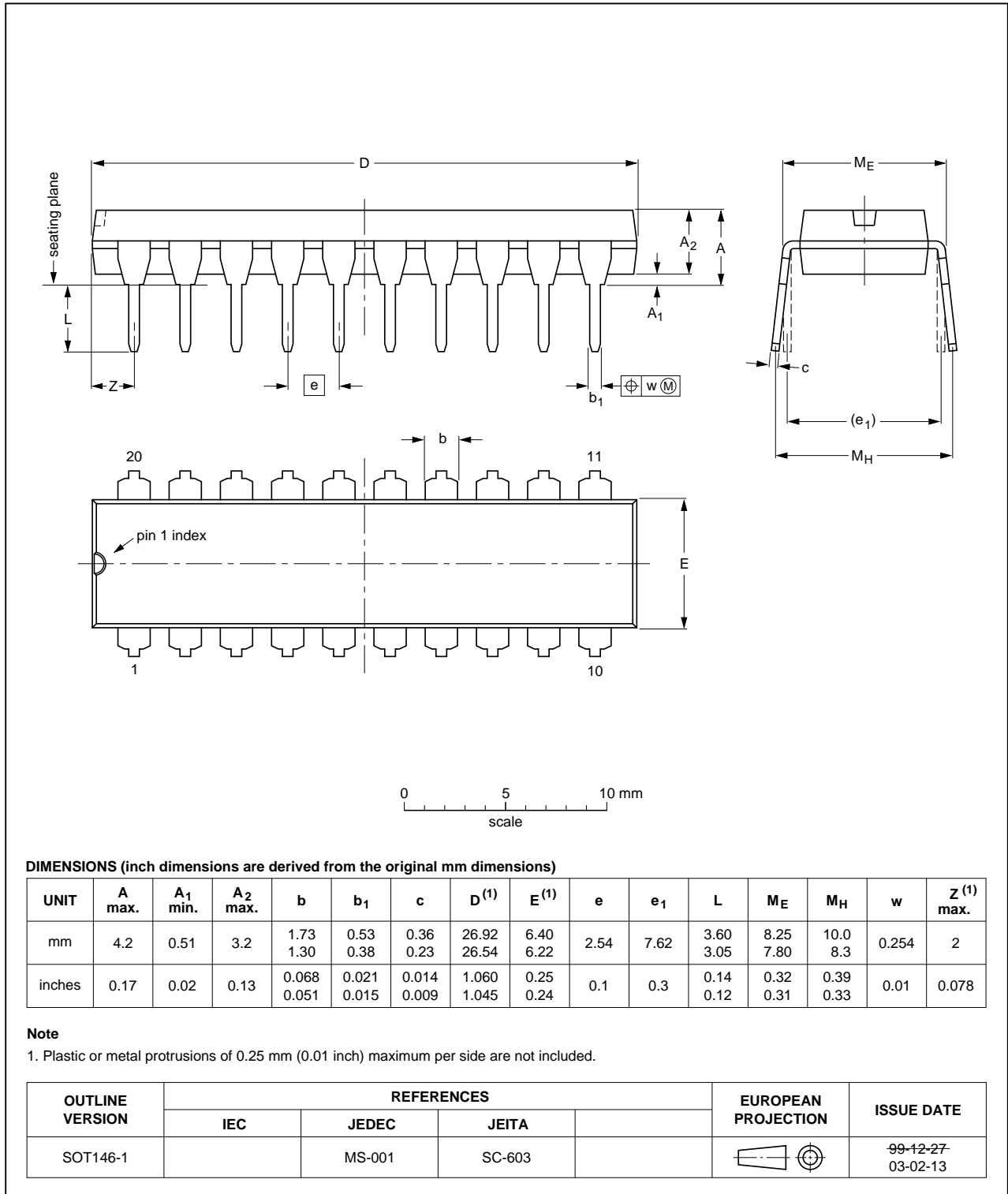


Fig 12. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

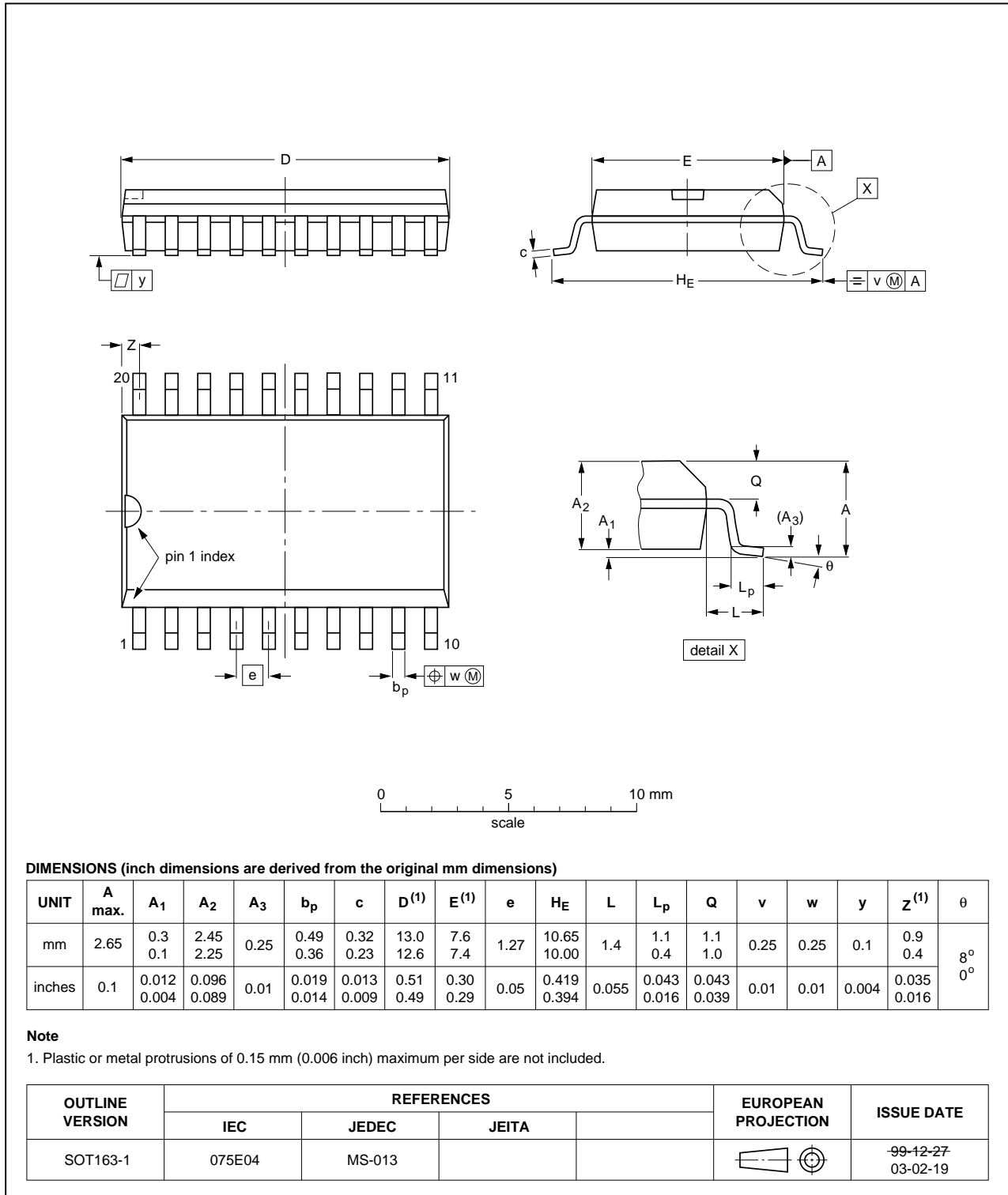


Fig 13. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

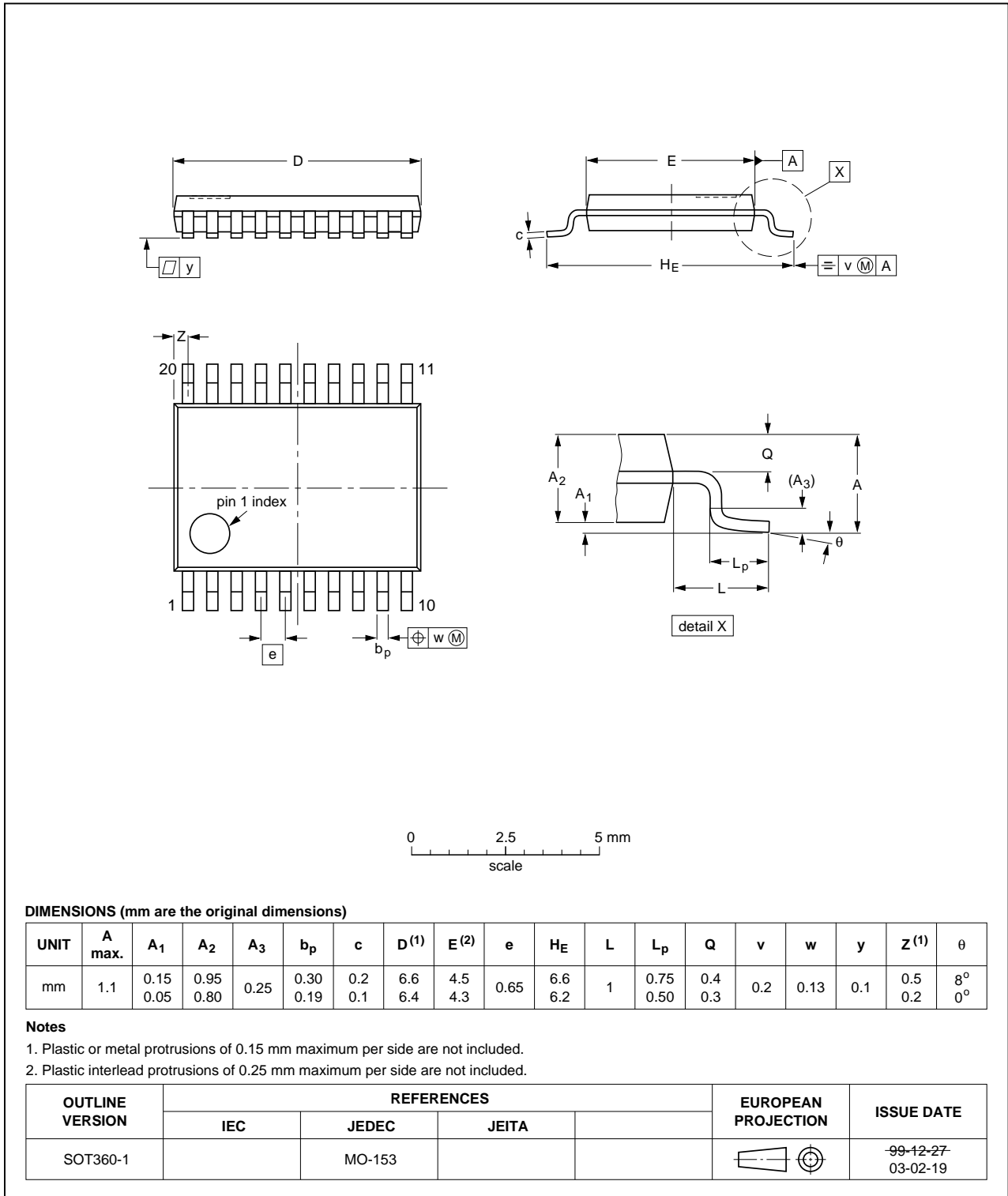


Fig 14. Package outline SOT360-1 (TSSOP20)

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4894B v.8	20111122	Product data sheet	-	HEF4894B v.7
Modifications:	<ul style="list-style-type: none"><li>• Section Applications removed</li><li>• <a href="#">Table 6</a>: I<sub>OH</sub> minimum values changed to maximum</li></ul>			
HEF4894B v.7	20100813	Product data sheet	-	HEF4894B v.6
HEF4894B v.6	20100408	Product data sheet	-	HEF4894B v.5
HEF4894B v.5	20091222	Product data sheet	-	HEF4894B v.4
HEF4894B v.4	20080827	Product data sheet	-	HEF4894B_CN V v.3
HEF4894B_CN V v.3	19950101	Product specification	-	HEF4894B_CN V v.2
HEF4894B_CN V v.2	19950101	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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