IP3253/IP3254-TTL

Integrated 4-, 6- and 8-channel passive EMI-filter network with high-level ESD protection

Rev. 1 — 5 May 2011 Product data sheet

1. Product profile

1.1 General description

The IP3253/IP3254-TTL family consists of 4-, 6- and 8-channel LC low-pass filter arrays designed to filter unwanted RF signals on the I/O ports of portable communication and computing devices. In addition, the IP3253/IP3254-TTL family incorporates diodes which protect downstream components from ElectroStatic Discharge (ESD) voltages up to ±15 kV.

These devices are fabricated using monolithic silicon technology integrating up to 8 inductors and 16 diodes in a 0.4 mm pitch 8-, 12- or 16-pin ultra-thin leadless Quad Flat No-leads (QFN) plastic package.

1.2 Features and benefits

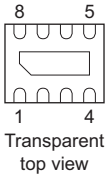
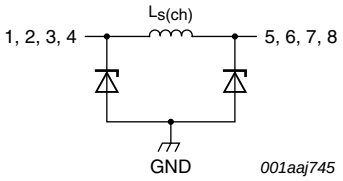
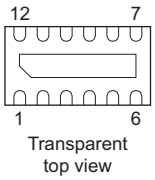
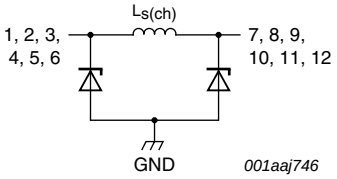
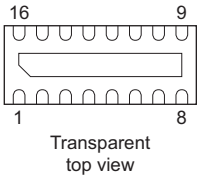
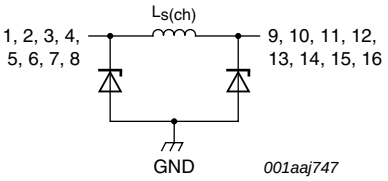
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- 4-, 6- and 8-channel integrated π-type LC filter network
- ESD protection to ±15 kV contact discharge according to IEC 61000-4-2, level 4
- ESD protection to ±30 kV contact discharge according to MIL-STD-883 (method 3015) Human Body Model (HBM)
- QFN plastic package with 0.4 mm pitch and 0.5 mm height

1.3 Applications

- General-purpose ElectroMagnetic Interference (EMI), Radio-Frequency Interference (RFI) filtering and downstream ESD protection for:
  - Cellular phone and Personal Communication System (PCS) mobile handsets
  - Cordless telephones
  - Wireless data (WAN/LAN) systems

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
IP3253CZ8-4-TTL; IP3254CZ8-4-TTL (SOT1166-1)			
1 and 8	filter channel 1		
2 and 7	filter channel 2		
3 and 6	filter channel 3		
4 and 5	filter channel 4		
ground pad	ground		
IP3253CZ12-6-TTL; IP3254CZ12-6-TTL (SOT1167-1)			
1 and 12	filter channel 1		
2 and 11	filter channel 2		
3 and 10	filter channel 3		
4 and 9	filter channel 4		
5 and 8	filter channel 5		
6 and 7	filter channel 6		
ground pad	ground		
IP3253CZ16-8-TTL; IP3254CZ16-8-TTL (SOT1168-1)			
1 and 16	filter channel 1		
2 and 15	filter channel 2		
3 and 14	filter channel 3		
4 and 13	filter channel 4		
5 and 12	filter channel 5		
6 and 11	filter channel 6		
7 and 10	filter channel 7		
8 and 9	filter channel 8		
ground pad	ground		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP3253CZ8-4-TTL	HUSON8	plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 × 1.7 × 0.55 mm	SOT1166-1
IP3253CZ12-6-TTL	HUSON12	plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 × 2.5 × 0.55 mm	SOT1167-1
IP3253CZ16-8-TTL	HUSON16	plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 × 3.3 × 0.55 mm	SOT1168-1
IP3254CZ8-4-TTL	HUSON8	plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 × 1.7 × 0.55 mm	SOT1166-1
IP3254CZ12-6-TTL	HUSON12	plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 × 2.5 × 0.55 mm	SOT1167-1
IP3254CZ16-8-TTL	HUSON16	plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 × 3.3 × 0.55 mm	SOT1168-1

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+5.6	V
V_{ESD}	electrostatic discharge voltage	all pins to ground; contact discharge				
		HBM; MIL-STD-883, method 3015		-	±30	kV
		IEC 61000-4-2, level 4	[1]	-	±15	kV
I_{ch}	channel current (DC)	T_{amb} = 85 °C		-	30	mA
P_{ch}	channel power dissipation			-	10	mW
P_{tot}/pack	total power dissipation per package	T_{amb} = 85 °C		-	500	mW
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C

[1] Device tested with 1000 pulses of ±15 kV contact discharges, according to the IEC 61000-4-2 model, far exceeding IEC 61000-4-2 level 4 (8 kV contact discharge).

5. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$L_{s(ch)}$	channel series inductance			-	18	-	nH
C_{ch}	channel capacitance	for the total channel; f_i = 100 kHz	[1]				
	IP3253CZx-y-TTL	$V_{bias(DC)}$ = 2.5 V		20	25	28.2	pF
		$V_{bias(DC)}$ = 0 V		34	43	48	pF
	IP3254CZx-y-TTL	$V_{bias(DC)}$ = 2.5 V		25	33	40	pF
		$V_{bias(DC)}$ = 0 V		38	50	60	pF
I_{LR}	reverse leakage current	per channel; V_I = 3.5 V		-	-	0.1	μA
V_{BR}	breakdown voltage	positive clamp; I_I = 1 mA		5.8	-	10	V
V_F	forward voltage	negative clamp; I_F = −1 mA		−1.5	-	−0.4	V
$R_{(ch-ch)}$	resistance between channels	V_I = 3.5 V		10	-	-	MΩ
$R_{s(ch)}$	channel series resistance			-	8	-	Ω

[1] Guaranteed by design.

Table 5. Frequency characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
α_{il}	insertion loss	R_{source} = 50 Ω; R_L = 50 Ω; 1 GHz < f_i < 4 GHz		-	30	-	dB
f_{-3dB}	cut-off frequency	R_{source} = 50 Ω; R_L = 50 Ω; V_I = 0 V					
	IP3253CZx-y-TTL			-	175	-	MHz
	IP3254CZx-y-TTL			-	145	-	MHz
$f_{rolloff}$	roll-off frequency	R_{source} = 50 Ω; R_L = 50 Ω; V_I = 0 V	[1]				
	IP3253CZx-y-TTL			-	350	-	MHz
	IP3254CZx-y-TTL			-	315	-	MHz

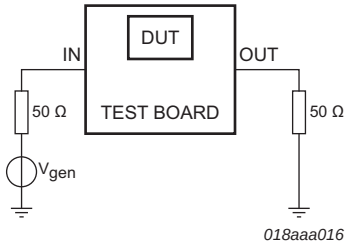
[1] Measured at 6 dB attenuation.

6. Application information

6.1 Insertion loss

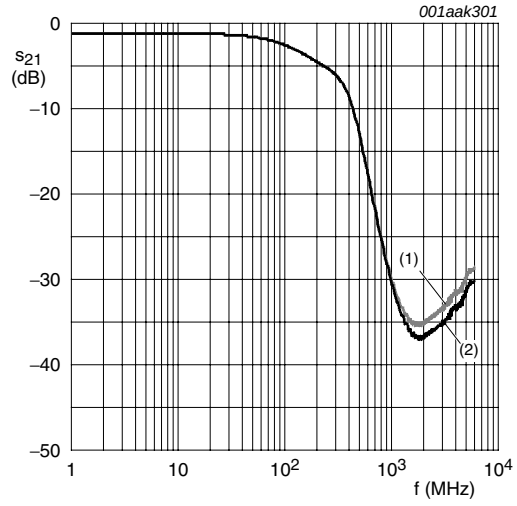
The devices are specifically designed as EMI/RFI filters for multichannel interfaces.

The block schematic for measuring insertion loss in a 50 Ω system is shown in Figure 1. An example of the measurement curves for all channels is shown in Figure 2.



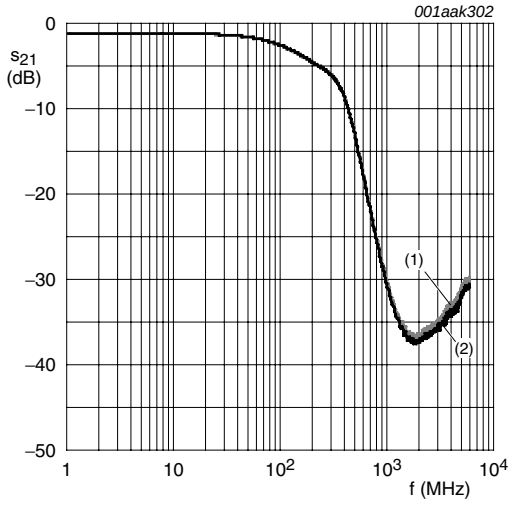
Test Printed-Circuit Board (PCB) utilizes laser-drilled micro-via holes which connect the ground plane to the device ground pins.

Fig 1. Frequency response setup



(1) Channel 1 (pin 1 to pin 8)

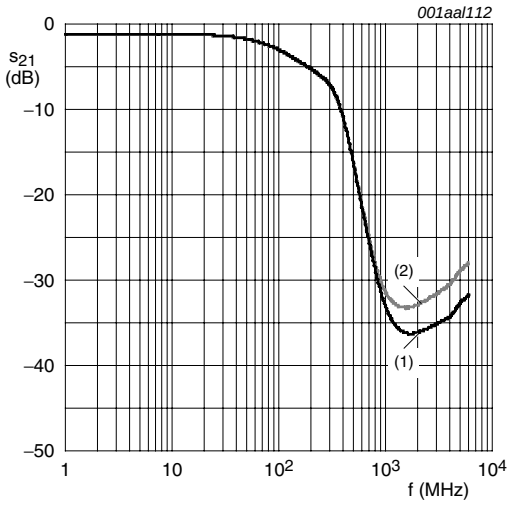
(2) Channel 4 (pin 4 to pin 5)



(1) Channel 3 (pin 3 to pin 6)

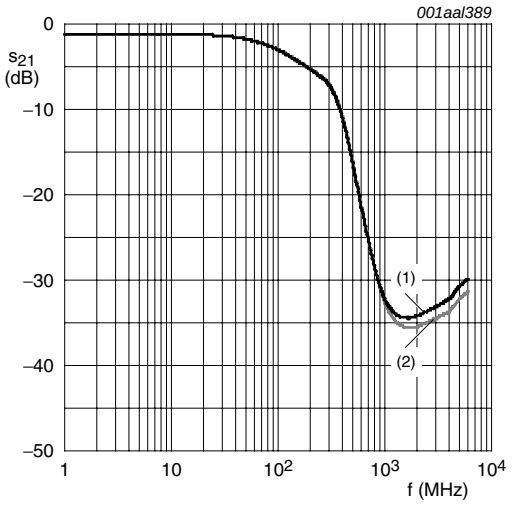
(2) Channel 2 (pin 2 to pin 7)

Fig 2. IP3253CZ8-4-TTL measured insertion loss magnitudes



(1) Channel 1 (pin 1 to pin 8)

(2) Channel 4 (pin 4 to pin 5)



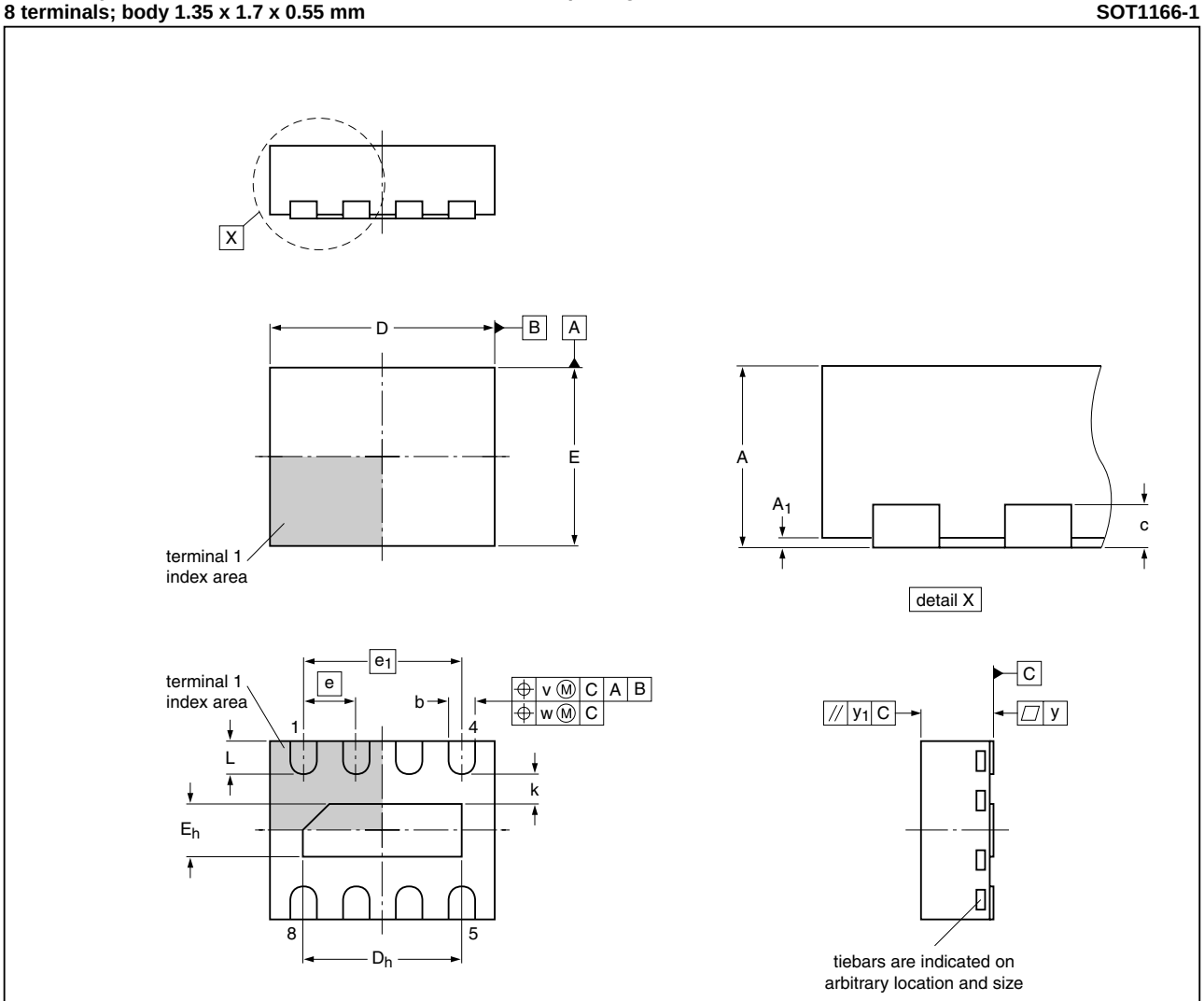
(1) Channel 3 (pin 3 to pin 6)

(2) Channel 2 (pin 2 to pin 7)

Fig 3. IP3254CZ8-4-TTL measured insertion loss magnitudes

7. Package outline

HUSON8: plastic, thermal enhanced ultra thin small outline package; no leads; 8 terminals; body 1.35 x 1.7 x 0.55 mm **SOT1166-1**



Dimensions

Unit[1]		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	0.55	0.05	0.25		1.8	1.3	1.45	0.45				0.30				
mm	nom			0.20	0.127	1.7	1.2	1.35	0.40	0.4	1.2		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.15		1.6	1.1	1.25	0.35			0.2	0.20				

Note

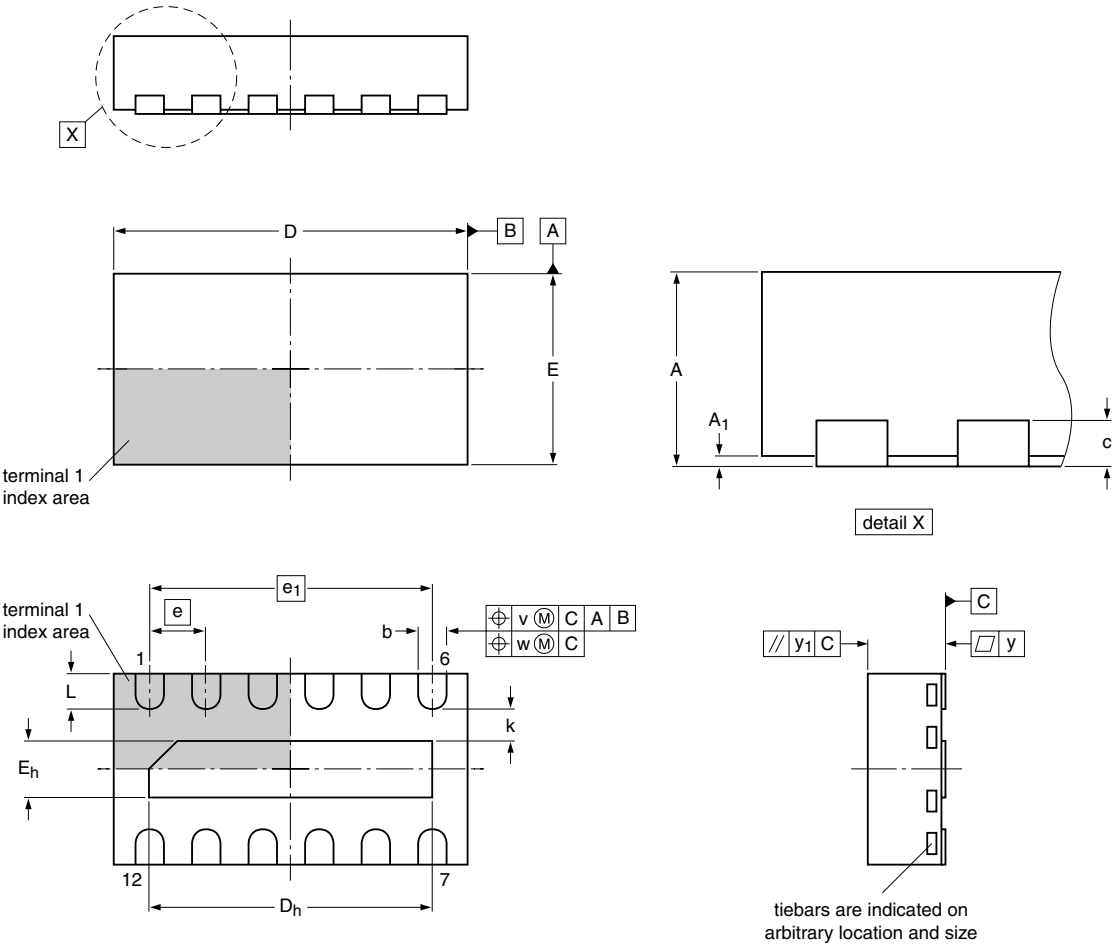
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1166-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1166-1	- - -	- - -	- - -			~~10-03-18~~ 10-03-22

Fig 4. Package outline SOT1166-1 (HUSON8)

HUSON12: plastic, thermal enhanced ultra thin small outline package; no leads; 12 terminals; body 1.35 x 2.5 x 0.55 mm **SOT1167-1**



Dimensions

Unit[1]		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	0.55	0.05	0.25		2.6	2.1	1.45	0.45				0.30				
mm	nom			0.20	0.127	2.5	2.0	1.35	0.40	0.4	2.0		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.15		2.4	1.9	1.25	0.35			0.2	0.20				

Note

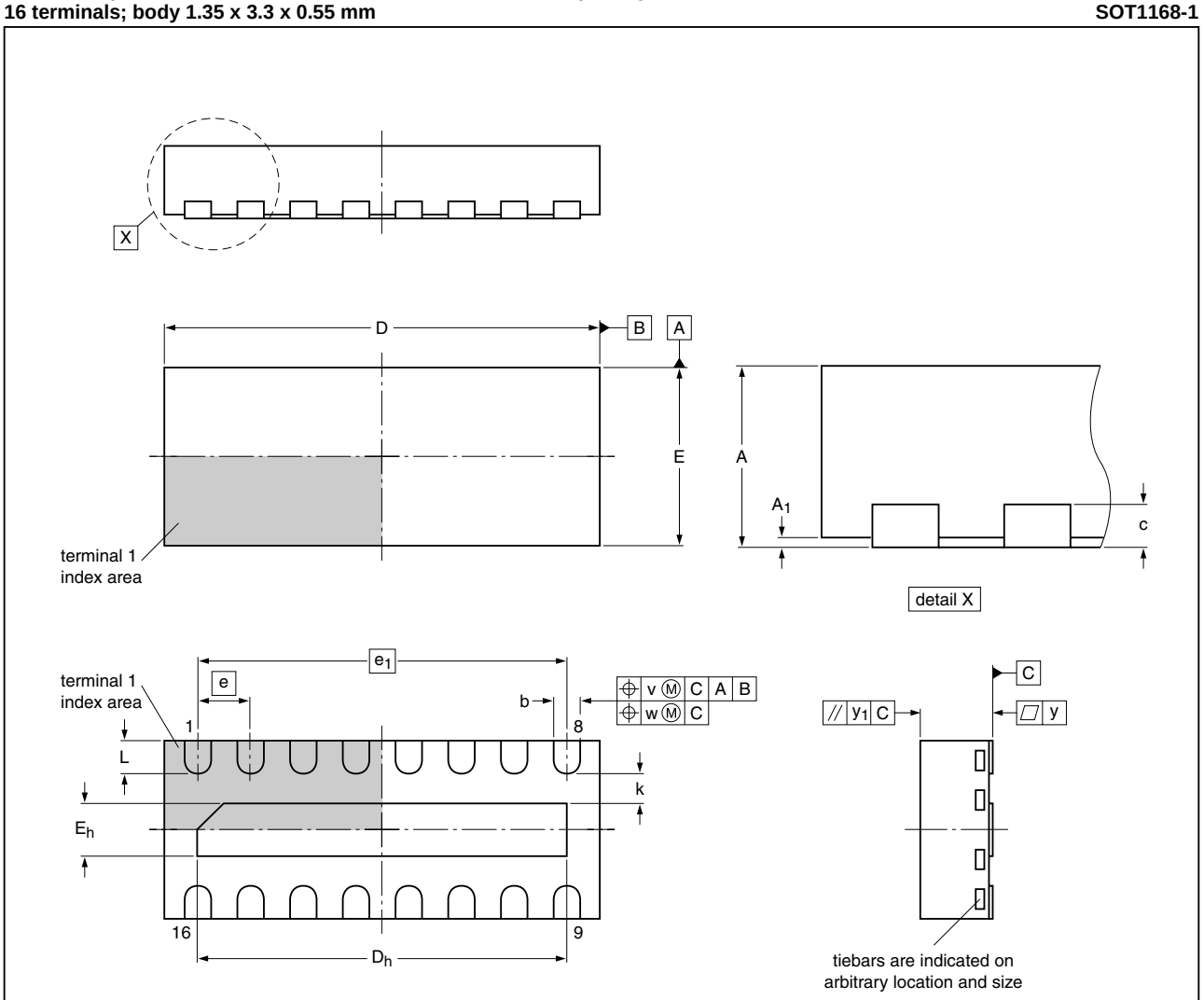
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1167-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1167-1	- - -	- - -	- - -		~~10-03-18~~ 10-03-22

Fig 5. Package outline SOT1167-1 (HUSON12)

HUSON16: plastic, thermal enhanced ultra thin small outline package; no leads; 16 terminals; body 1.35 x 3.3 x 0.55 mm **SOT1168-1**



Dimensions

Unit[1]		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	0.55	0.05	0.25		3.4	2.9	1.45	0.45				0.30				
mm	nom			0.20	0.127	3.3	2.8	1.35	0.40	0.4	2.8		0.25	0.1	0.05	0.05	0.05
	min		0.00	0.15		3.2	2.7	1.25	0.35			0.2	0.20				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1168-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1168-1	- - -	- - -	- - -		~~10-03-18~~ 10-03-22

Fig 6. Package outline SOT1168-1 (HUSON16)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3253_IP3254-TTL v.1	20110505	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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