PCA8886

Dual channel capacitive proximity switch with auto-calibration and large voltage operating range

Rev. 2 — 20 September 2012 Product data sheet

1. General description

The PCA8886 is a low power dual channel capacitive proximity switch that uses a patented (EDISEN) digital method to detect a change in capacitance on remote sensing plates. Changes in the static capacitance (as opposed to dynamic capacitance changes) are automatically compensated using continuous auto-calibration. Remote sensing plates (for example, conductive foil) can be connected directly to the IC[1] or remotely using a coaxial cable.

2. Features and benefits

- Dynamic proximity switch
- Digital processing method
- Automatic calibration
- Adjustable sensitivity, can be made very high
- Adjustable response time
- Wide input capacitance range (10 pF to 60 pF)
- A large distance (several meters) between the sensing plate and the IC is possible
- Open-drain output (P-type MOSFET, external load between pin and ground)
- Output configurable as push-button, toggle, or pulse
- Wide voltage operating range (V_{DD} = 3 V to 9 V)
- Designed for battery powered applications (I_{DD} = 6 μA, typical)
- Large temperature operating range (T_{amb} = –40 °C to +85 °C)
- AEC-Q100 compliant for automotive applications
- Available in TSSOP16

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

3. Applications

- Proximity detection
- Proximity sensing in
  - Door locks and grips
  - Portable entertainment units
  - Computing tablets
- Switch for medical applications
- Dashboard: switch to toggle menus and resetting trip counter
- Switch for use in explosive environments
- Vandal proof switches
- Transportation: Switches in or under upholstery, leather, handles, mats, and glass
- Buildings: switch in or under carpets, glass, or tiles
- Sanitary applications: use of standard metal sanitary parts (for example, tap) as switch
- Hermetically sealed keys on a keyboard

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8886TS	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	PCA8886

4.1 Ordering options

Table 2. Ordering options

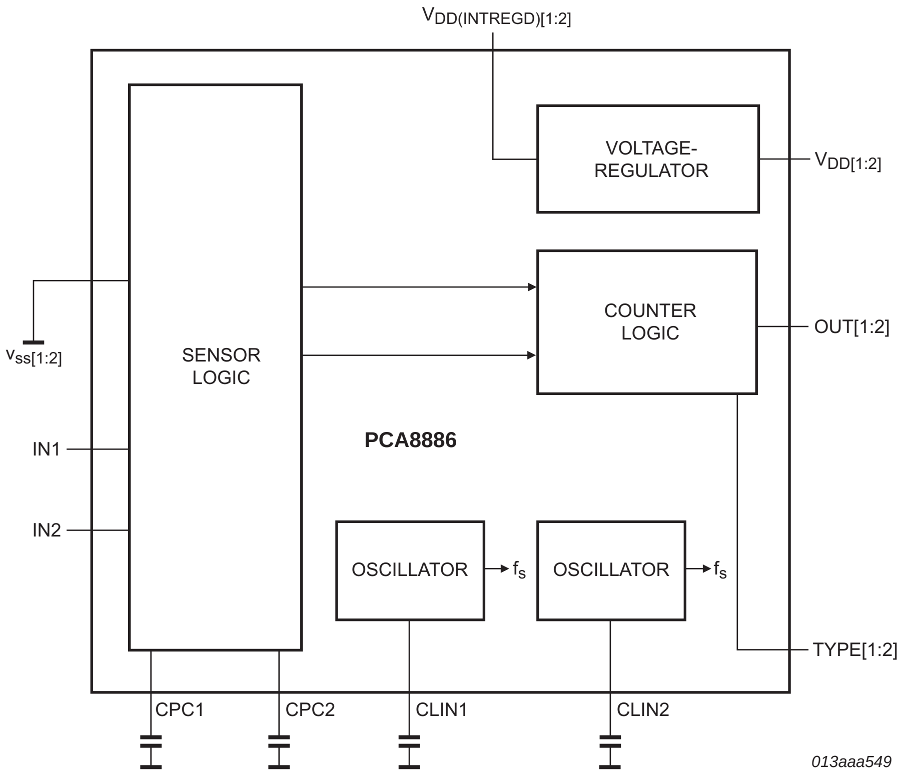
Type number	IC revision	Sales item (12NC)	Delivery form
PCA8886TS/Q900/1	1	935297325118	tape and reel, 13 inch

5. Marking

Table 3. Marking codes

Type number	Marking code
PCA8886TS/Q900/1	PCA8886

6. Block diagram

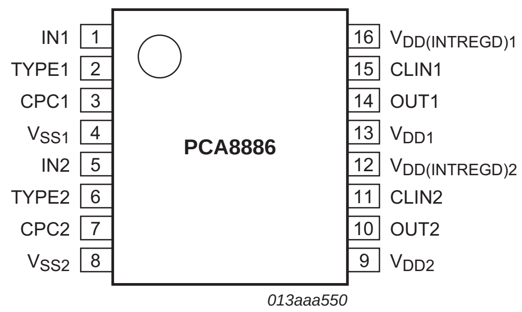


The PCA8886 integrates two identical capacitive proximity switches which can be configured separately.

Fig 1. Block diagram of PCA8886

7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 16.

Fig 2. Pin configuration of PCA8886TS (TSSOP16)

7.2 Pin description

Table 4. Pin description

Symbol	Pin TSSOP16 (PCA8886TS)	Type	Description
IN1	1	analog input/output	sensor input 1
TYPE1	2	input	select output configuration of pin OUT1
CPC1	3	analog input/output	sensitivity setting 1
V_{SS1}	4	supply	ground supply voltage 1
IN2	5	analog input/output	sensor input 2
TYPE2	6	input	select output configuration of pin OUT2
CPC2	7	analog input/output	sensitivity setting 2
V_{SS2}	8	supply	ground supply voltage 2
V_{DD2}	9	supply	supply voltage 2
OUT2	10	output	switch output 2
CLIN2	11	analog input/output	sampling rate setting 2
$V_{DD(INTREGD)2}$[1]	12	supply	internal regulated supply voltage output 2
V_{DD1}	13	supply	supply voltage 1
OUT1	14	output	switch output 1
CLIN1	15	analog input/output	sampling rate setting 1
$V_{DD(INTREGD)1}$[1]	16	supply	internal regulated supply voltage output 1

[1] The internal regulated supply voltage outputs must be decoupled with a decoupling capacitor to $V_{SS[1:2]}$.

8. Functional description

Figure 3 and Figure 4 show the functional principle of one channel of the PCA8886.

The discharge time (t_{dch}) of a chip-internal RC timing circuit, to which the external sensing plates are connected via pins IN[1:2], is compared to the discharge time ($t_{dch(ref)}$) of a second chip-internal reference RC timing circuit. Both RC timing circuits are periodically charged from $V_{DD(INTREGD)[1:2]}$ via identical switches and then discharged via a resistor to ground (V_{SS}). Both switches are synchronized.

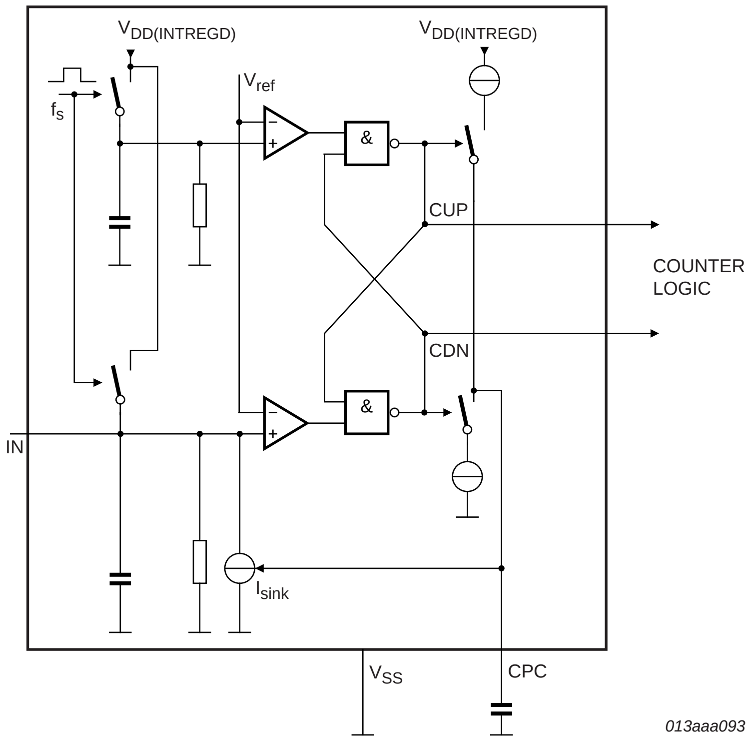


Fig 3. Functional diagram of the sensor logic (one channel)

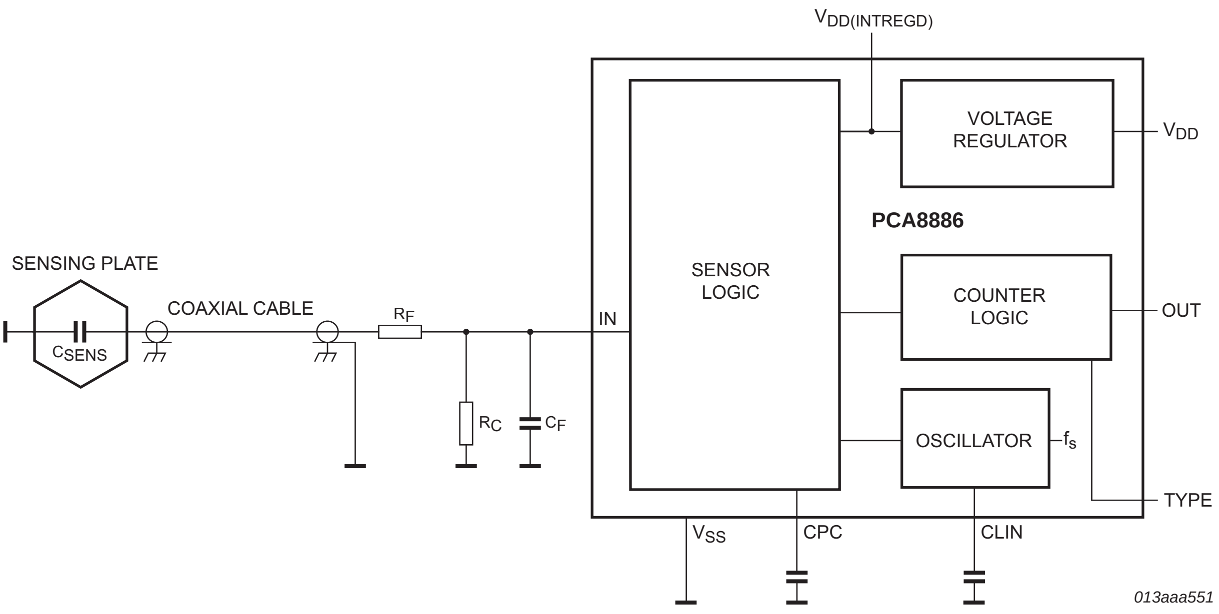
The charge-discharge cycle is governed by the sampling rate (f_s). If the voltage of one of the RC timing circuits falls below the internal reference voltage V_{ref}, the respective comparator output will become LOW. The logic following the comparators determines which comparator switches first. If the upper (reference) comparator switches, then a pulse is given on CUP. If the lower (input) comparator switches first, then a pulse is given on CDN (see Figure 3).

The pulses control the charge on the external capacitor C_{CPC} on pins CPC[1:2]. Every time a pulse is given on CUP, capacitor C_{CPC} is charged from $V_{DD(INTREGD)}$ for a fixed time causing the voltage on C_{CPC} to rise. Likewise when a pulse occurs on CDN, capacitor C_{CPC} is connected to a current sink to ground for a fixed time causing the voltage on C_{CPC} to fall.

If the capacitance on pins IN[1:2] increases, the discharge time t_{dch} increases too. Therefore it will take longer for the voltage on the corresponding comparator to drop below V_{ref}. Only once this happens, the comparator output will become LOW and this results in a pulse on CDN discharging the external capacitor C_{CPC} slightly. Thus most pulses will now be given by CUP. Without further action, capacitor C_{CPC} would then fully charge.

However, a chip-internal automatic calibration mechanism that is based on a voltage controlled sink current (I_{sink}) connected to pins IN[1:2] attempts to equalize the discharge time t_{dch} with the internal reference discharge time $t_{dch(ref)}$. The current source is controlled by the voltage on C_{CPC} which causes the capacitance on pins IN[1:2] to be discharged more quickly in the case that the voltage on C_{CPC} is rising, thereby compensating for the increase in capacitance on input pins IN[1:2]. This arrangement constitutes a closed-loop control system that constantly attempts to equalize the discharge time t_{dch} with $t_{dch(ref)}$. This allows compensating for slow changes in capacitance on input pins IN[1:2]. Fast changes due to an approaching hand for example will not be compensated. In the equilibrium state, the discharge times are equal and the pulses alternate between CUP and CDN.

From this also follows, that an increase in capacitor value C_{CPC} results in a smaller voltage change per pulse CUP or CDN. Thus the compensation due to internal current sink source I_{sink} is slower and therefore the sensitivity of the sensor will increase. Likewise a decrease in capacitor C_{CPC} will result in a lower sensitivity. (For further information see Section 13.)



C_{SENS} = sensing plate capacitance.

C_{CABLE} = cable capacitance.

R_C = external pull-down resistor.

R_F = low pass filter resistor.

C_F = low pass filter capacitor.

Fig 4. Functional principle of one channel of the PCA8886

The counter, following the sensor logic depicted in Figure 3, counts the pulses of CUP or CDN respectively. The counter is reset every time the pulse sequence changes from CUP to CDN or the other way around. Pins OUT[1:2] will only be activated when enough consecutive CUP or CDN pulses occur. Low-level interference or slow changes in the input capacitance do not cause the output to switch.

Various measures, such as asymmetrical charge and discharge steps, are taken to ensure that the output switches off correctly. A special start-up circuit ensures that the device reaches equilibrium quickly when the supply is attached.

Pins OUT[1:2] are open-drain outputs capable of pulling an external load R_{ext} (at maximum current of 20 mA) up to V_{DD}. The load resistor must be dimensioned appropriately, taking the maximum expected V_{DD} voltage into account. The output will be automatically deactivated (short circuit protection) for loads in excess of 30 mA. Pins OUT[1:2] can also drive CMOS inputs without connection of the external load.

A small internal 150 nA current sink I_{sink} enables a full voltage swing to take place on pins OUT[1:2], even if no load resistor is connected. This is useful for driving purely capacitive CMOS inputs. The falling slope can be fairly slow in this mode, depending on load capacitance.

The sampling rate (f_s) corresponds to half of the frequency used in the RC timing circuit. The sampling rate can be adjusted within a specified range by selecting the value of C_{CLIN}. The oscillator frequency is internally modulated by 4 % using a pseudo random signal. This prevents interference caused by local AC-fields.

8.1 Output switching modes

The output switching behavior can be selected using pins TYPE[1:2] (see Figure 5)

- Push-button (TYPE[1:2] connected to $V_{SS[1:2]}$): The output OUT is active as long as the capacitive event[2] lasts.
- Toggle (TYPE[1:2] connected to $V_{DD(INTREGD)[1:2]}$): The output OUT is activated by the first capacitive event and deactivated by a following capacitive event.
- Pulse (C_{TYPE} connected between TYPE[1:2] and $V_{SS[1:2]}$): The output OUT is activated for a defined time at each capacitive event. The pulse duration is determined by the value of C_{TYPE} and is approximately 2.5 ms/nF.

A typical value for C_{TYPE} is 4.7 nF which results in an output pulse duration of about 10 ms. The maximum value of C_{TYPE} is 470 nF which results in a pulse duration of about 1 s. Capacitive events are ignored that occur during the time the output is active.

Figure 5 illustrates the switching behavior for the output switching modes. Additionally the graph illustrates, that short-term disturbances on the sensor are suppressed by the circuit.

2. A capacitive event is a dynamic increase of capacitance at the sensor input pins IN[1:2].

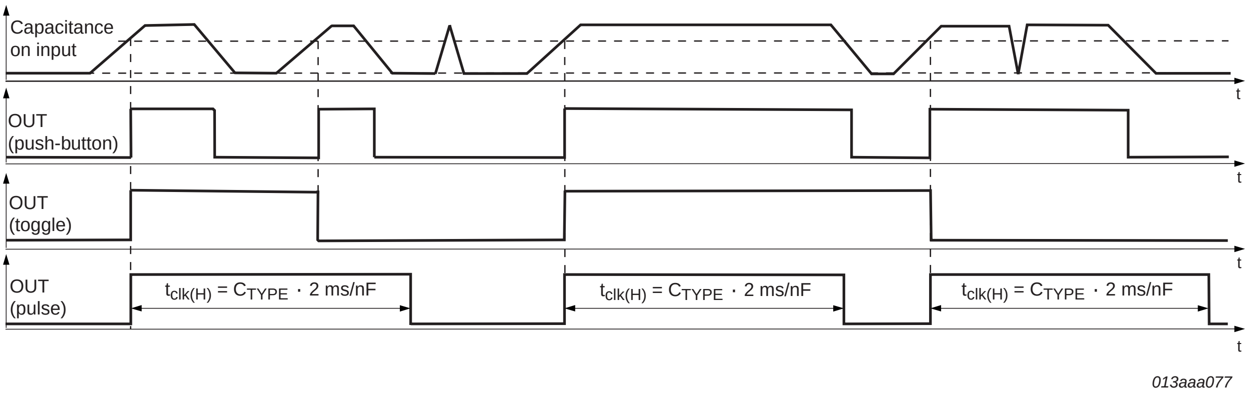


Fig 5. Switching modes timing diagram of PCA8886

8.2 Voltage regulator

The PCA8886 implements a chip-internal voltage regulator supplied by pins $V_{DD[1:2]}$ that provides an internal supply ($V_{DD(INTREGD)}$), limited to a maximum of 4.6 V. Figure 6 shows the relationship between $V_{DD[1:2]}$ and $V_{DD(INTREGD)[1:2]}$.

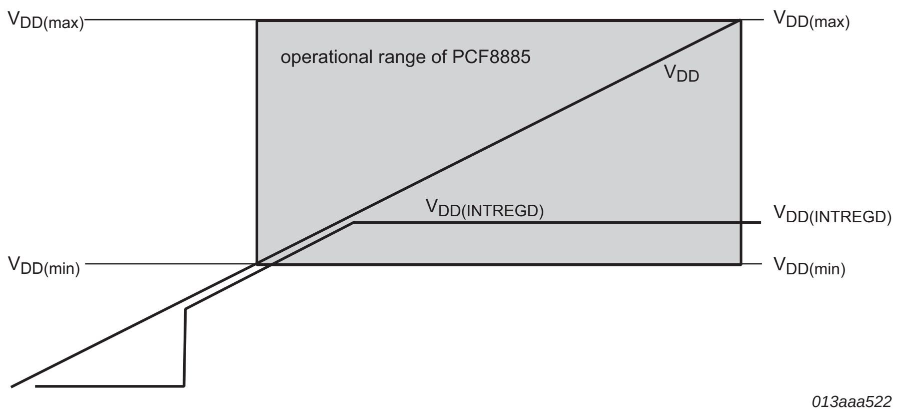


Fig 6. Integrated voltage regulator

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+9	V
V_I	input voltage	on pins IN[1:2], TYPE[1:2], CPC[1:2]		–0.5	$V_{DD(INTREGD)}$ + 0.5	V
I_O	output current	on pins OUT[1:2]		–10	+50	mA
I_{SS}	ground supply current			–10	+50	mA
I_I	input current	on any other pin		–10	+10	mA
P_{tot}	total power dissipation			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±2500	V
		CDM	[2]	-	±1000	V
I_{lu}	latch-up current		[3]	-	100	mA
T_{stg}	storage temperature		[4]	–60	+125	°C
T_{amb}	ambient temperature	operating device		–40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 7 “JESD22-A114”.

[2] Pass level; Charged-Device Model (CDM), according to Ref. 8 “JESD22-C101”.

[3] Pass level; latch-up testing, according to Ref. 9 “JESD78” at maximum ambient temperature ($T_{amb(max)}$ = +85 °C).

[4] According to the store and transport requirements (see Ref. 12 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

10. Static characteristics

Table 6. Static characteristics

V_{DD} = 5 V, T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage		[1]	3.0	-	9.0	V
$V_{DD(INTREGD)}$	internal regulated supply voltage			3.0	4.0	4.6	V
$\Delta V_{DD(INTREGD)}$	internal regulated supply voltage variation	regulator voltage drop		-	10	50	mV
I_{DD}	supply current	idle state; f_s = 1 kHz	[2]	-	6	10	µA
		idle state; f_s = 1 kHz; V_{DD} = 3.0 V	[2]	-	4.4	7	µA
I_{sink}	sink current	internal constant current to $V_{SS[1:2]}$		-	150	-	nA
V_O	output voltage	on pins OUT[1:2]; pull-up voltage		0	V_{DD}	9.0	V
I_O	output current	P-MOS	[3]	0	10	20	mA
		short circuit protection $V_O \geq 0.6$ V		20	30	50	mA
V_{sat}	saturation voltage	on pins OUT[1:2]; I_O = +10 mA		0.1	0.2	0.4	V
		on pins OUT[1:2]; I_O = +10 mA; V_{DD} = 3.0 V		0.1	0.3	0.5	V
C_{dec}	decoupling capacitance	on pins $V_{DD(INTREGD)[1:2]}$	[4]	100	-	220	nF
V_I	input voltage	on pins CPC[1:2]		0.6	-	$V_{DD(INTREGD)} - 0.5$	V

[1] When the input capacitance range is limited to 10 pF $\leq C_i \leq$ 40 pF or an external pull-down resistor R_C is used, the device can be operated down to V_{DD} = 3.0 V over the full temperature range.

[2] Idle state is the steady state after completed power-on without any activity on the sensor plate and the voltage on the reservoir capacitor C_{CPC} settled.

[3] For reliability reasons, the average output current must be limited to 4.6 mA at 70 °C and 3.0 mA at 85 °C.

[4] External ceramic chip capacitor recommended (see Figure 15).

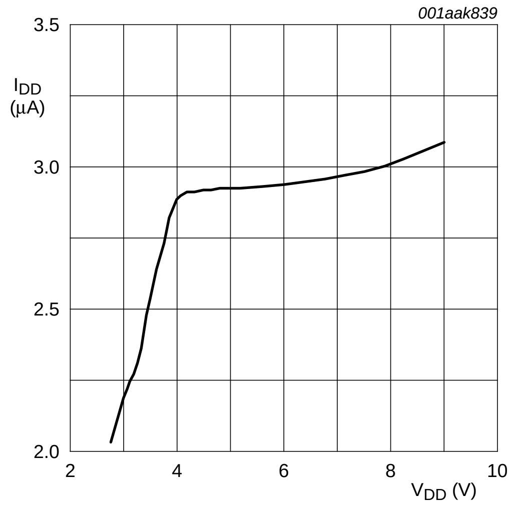
11. Dynamic characteristics

Table 7. Dynamic characteristics
V_{DD} = 5V, C_{CLIN} = 22 pF, C_{CPC} = 470 nF, T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{CLIN}	capacitance on pin CLIN		0	22	100	pF
C_{CPC}	capacitance on pin CPC	X7R ceramic chip capacitor	90	470	2500	nF
$N_{res(dig)eq}$	equivalent digital resolution		-	14	-	bit
C_{TYPE}	capacitance on pin TYPE		0.1	-	470	nF
C_i	input capacitance	sensing plate and connecting cable	10	-	60	pF
		sensing plate and connecting cable; T_{amb} = −40 °C to +85 °C; V_{DD} = 3.0 V	10	-	40	pF
$t_{startup}$	start-up time	until normal operation is established	-	0.5	-	s
t_p	pulse duration	on pins OUT[1:2]; in pulse mode; $C_{TYPE} \geq 10$ nF	-	2.5	-	ms/nF
f_s	sampling frequency	C_{CLIN} = 0 pF	-	3.3	-	kHz
		C_{CLIN} = 22 pF (typical value)	-	1	-	kHz
		C_{CLIN} = 100 pF	-	275	-	Hz
t_{sw}	switching time	at f_s = 1 kHz	-	64	-	ms

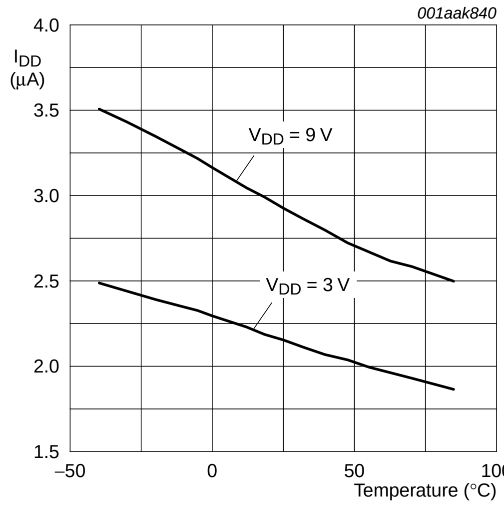
12. Characteristic curves

12.1 Power consumption



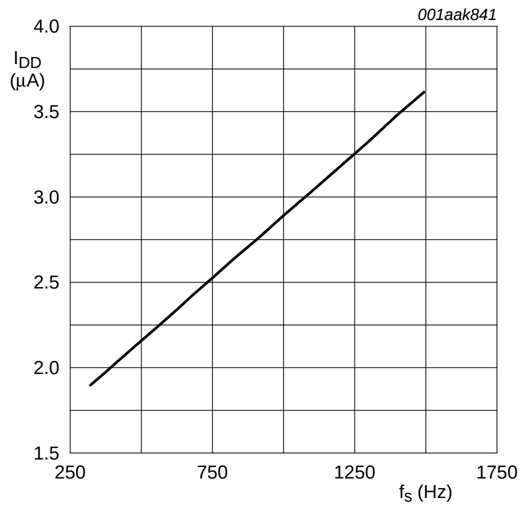
Idle state; f_s = 1 kHz; T_{amb} = 25 °C.

Fig 7. I_{DD} with respect to V_{DD}



Idle state; f_s = 1 kHz.

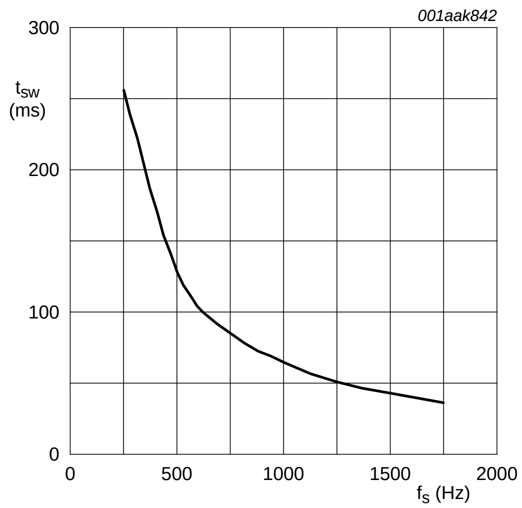
Fig 8. I_{DD} with respect to temperature



Idle state; V_{DD} = 6 V; T_{amb} = 25 °C.

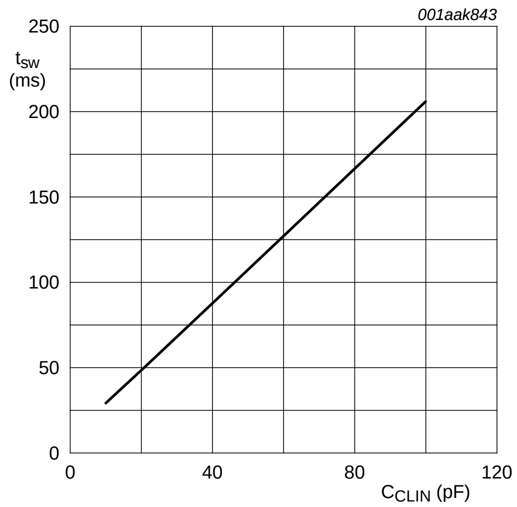
Fig 9. I_{DD} with respect to sampling frequency (f_s)

12.2 Typical reaction time



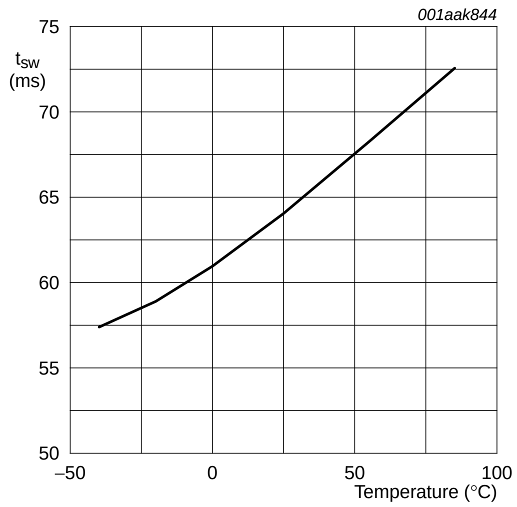
V_{DD} = 6 V; T_{amb} = 25 °C.

Fig 10. Switching time (t_{sw}) with respect to sampling frequency (f_s)



V_{DD} = 6 V; T_{amb} = 25 °C.

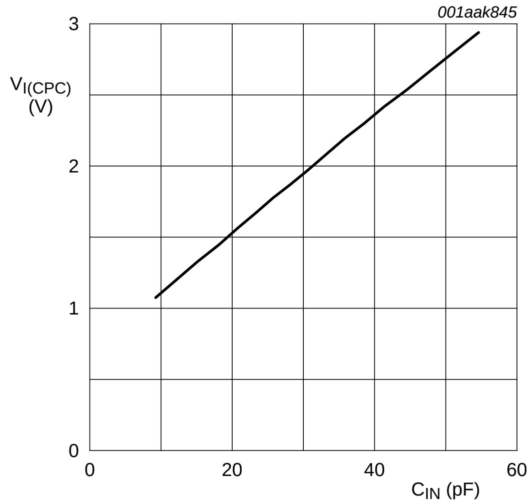
Fig 11. Switching time (t_{sw}) with respect to capacitor (C_{CLIN}) on pins CLIN[1:2]



V_{DD} = 6 V.

Fig 12. Switching time (t_{sw}) with respect to temperature

12.3 Reservoir capacitor voltage

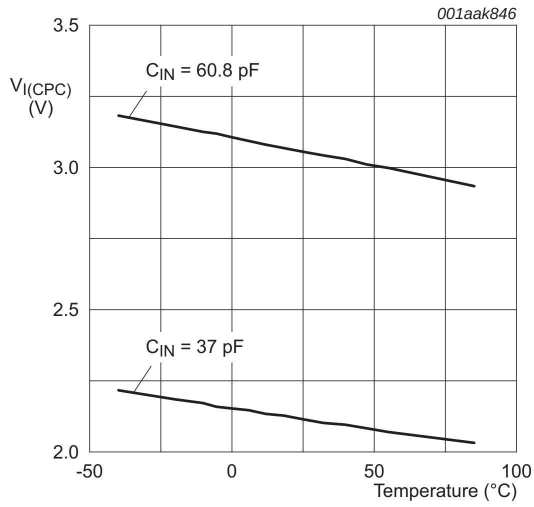


V_{DD} = 6 V; T_{amb} = 25 °C.

$V_{I(CPC)}$ = input voltage on pins CPC[1:2].

C_{IN} = capacitor on pins IN[1:2].

Fig 13. Input voltage on pins CPC[1:2] ($V_{I(CPC)}$) with respect to capacitor (C_{IN}) on pins IN[1:2]



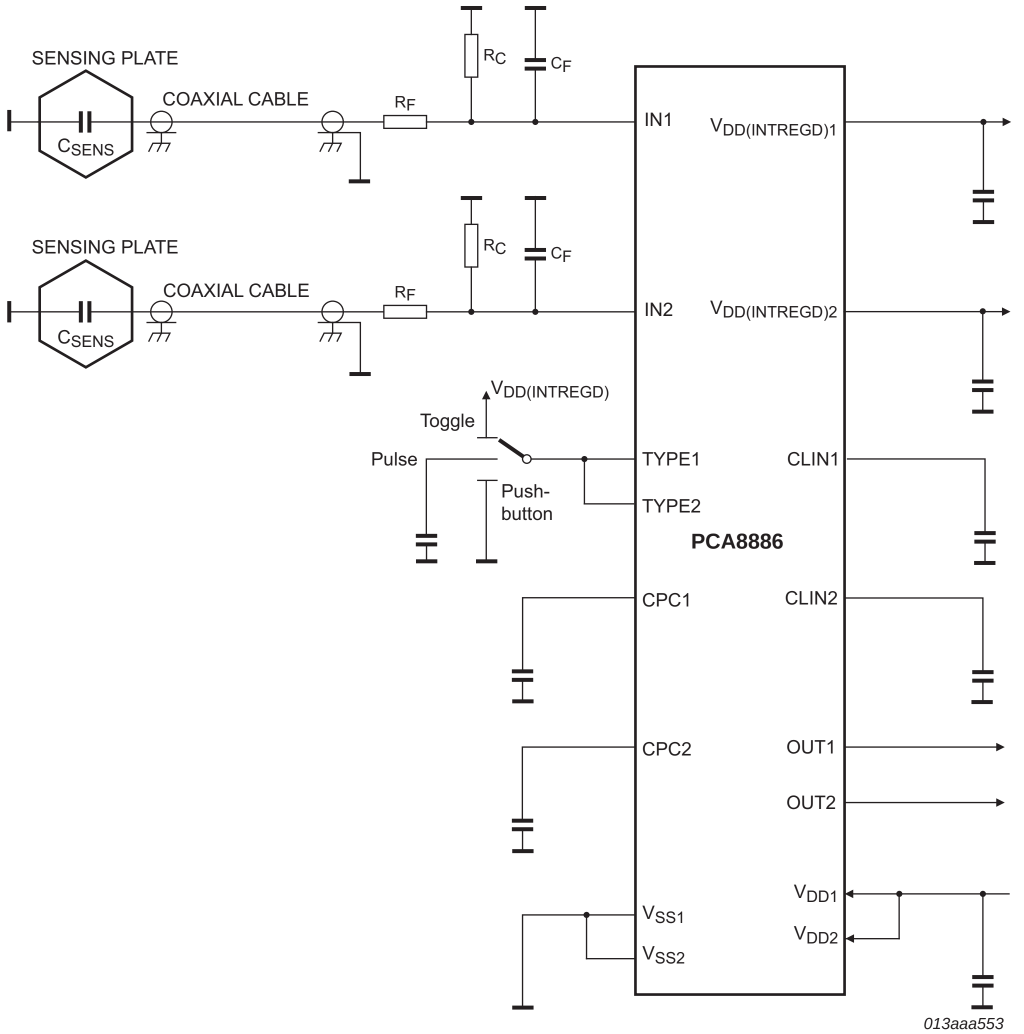
V_{DD} = 6 V.

$V_{I(CPC)}$ = input voltage on pins CPC[1:2]

Fig 14. Input voltage ($V_{I(CPC)}$) on pins CPC[1:2] with respect to temperature

13. Application information

Figure 15 shows the typical connections for a general application[3]. The positive supply is connected to pins $V_{DD[1:2]}$. It is recommended to connect smoothing capacitors to ground to both $V_{DD[1:2]}$ and $V_{DD(INTREGD)[1:2]}$ (values for C_{dec}, see Table 6).



C_{SENS} = sensing plate capacitance.

The coaxial cable is optional.

Fig 15. Typical application

The sampling rate is determined by the capacitance C_{CLIN} on pins CLIN[1:2]. A higher sampling rate reduces the reaction time and increases the current consumption.

The sensing plate capacitance C_{SENS} may consist of a small metal area, for example behind an isolating layer. The sensing plate can be connected to a coaxial cable (C_{CABLE}) which in turn is connected to the input pins IN[1:2]. Alternatively, the sensing plate can be

3. For further information, see Ref. 2 “AN10832”. Information about the appropriate evaluation board can be found in Ref. 11 “UM10505”.

directly connected to the input pins IN[1:2]. An internal low pass filter is used to reduce RF interference. An additional low pass filter consisting of a resistor R_F and capacitor C_F can be added to the input to further improve RF immunity as required. For good performance, the total amount of capacitance on the input (C_{SENS} + C_{CABLE} + C_F) should be in the proper range, the optimum point being around 30 pF. These conditions allow the control loop to adapt to the static capacitance on C_{SENS} and to compensate for slow changes in the sensing plate capacitance. A higher capacitive input loading is possible if an additional discharge resistor R_C is placed as shown in Figure 15. Resistor R_C simply reduces the discharge time such that the internal timing requirements are fulfilled.

The sensitivity of the sensor can be influenced by the sensing plate area and capacitor C_{CPC}. The sensitivity is significantly reduced when C_{CPC} is reduced. When maximum sensitivity is desired C_{CPC} can be increased, but this also increases sensitivity to interference. Pins CPC[1:2] has high-impedance and is sensitive to leakage currents. Therefore C_{CPC} should be a high-quality foil or ceramic capacitor, for example an X7R type.

For the choice of proper component values for a given application, the component specifications in Table 6 and Table 7 must be followed.

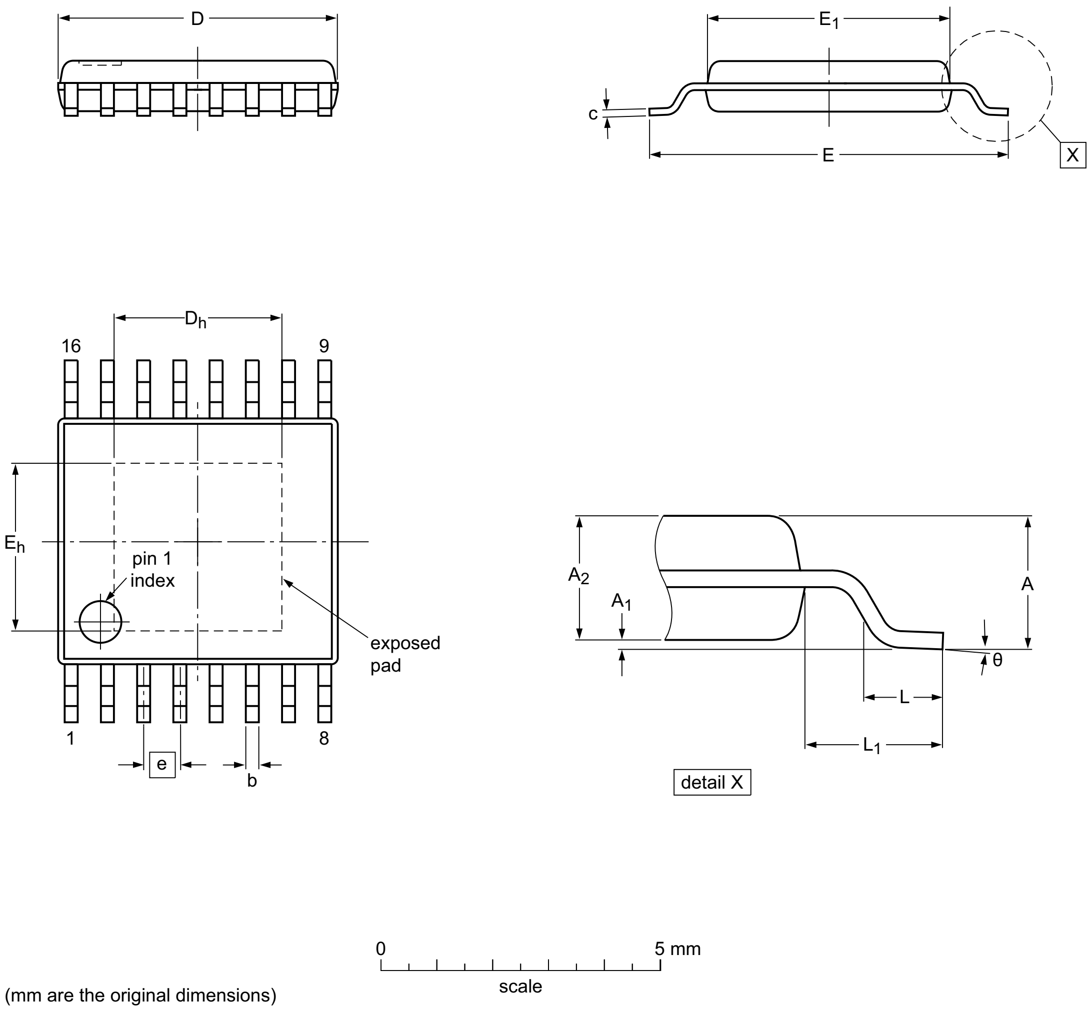
14. Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

TSSOP16: plastic small outline package; 16 leads; body width 4.4 mm **PCA8886**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	c	D	D_h	E	E_1	E_h	e	L	L_1	θ
mm	max	1.20	0.10	1.05	0.30	0.20	5.1		6.6	4.5			0.75		8°
	nom			0.90			5.0	2.997	6.4	4.4	2.997	0.65	0.60	1.0	
	min		0.025	0.80	0.19	0.09	4.9		6.2	4.3			0.45		0°

pca8886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA8886		MO-153 ISSUE C				~~12-08-28~~ 12-09-04

Fig 16. Package outline of PCA8886TS (TSSOP16)

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17. Packing information

17.1 Tape and reel information

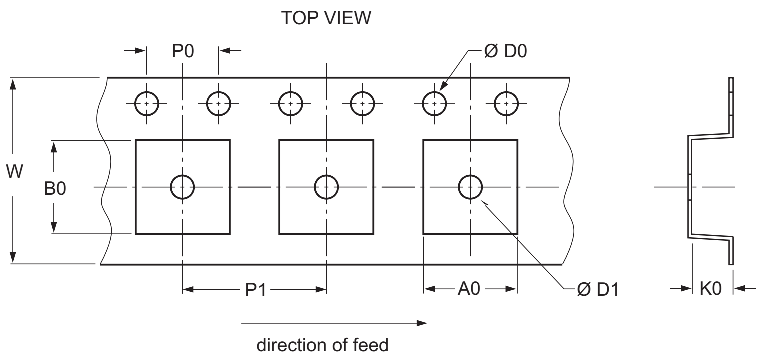


Fig 17. Carrier tape details for PCA8886

Table 8. Carrier tape dimensions of PCA8886

Symbol	Description	Value	Unit
Compartments			
A0	pocket width in x direction	6.9	mm
B0	pocket width in y direction	5.6	mm
K0	pocket depth	1.5 to 1.6	mm
P1	pocket hole pitch	8	mm
D1	pocket hole diameter	1.5 to 1.6	mm
Overall dimensions			
W	tape width	12	mm
D0	sprocket hole diameter	1.5 to 1.55	mm
P0	sprocket hole pitch	4	mm

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

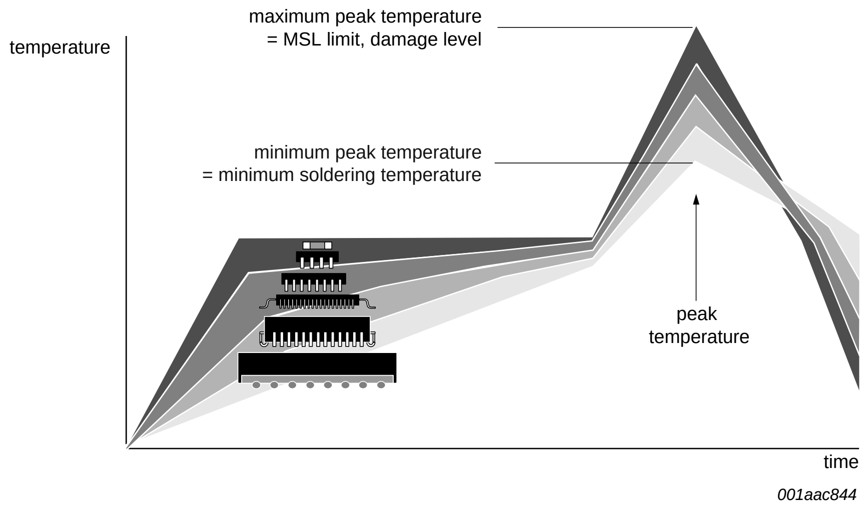
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
IC	Integrated Circuit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RC	Resistance-Capacitance
RF	Radio Frequency
SMD	Surface Mount Device

20. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10832 —** PCF8883 - capacitive proximity switch with auto-calibration

[3] **AN11122 —** Water and condensation safe touch sensing with the NXP capacitive touch sensors

[4] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[7] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[8] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[9] **JESD78 —** IC Latch-Up Test

[10] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[11] **UM10505 —** OM11057 quick start guide

[12] **UM10569 —** Store and transport requirements

21. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8886 v.2	20120920	Product data sheet	-	PCA8886 v.1
PCA8886 v.1	20111123	Objective data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Tables

25. Figures

26. Contents

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