PCA9605

Simple 2-wire bus buffer

Rev. 1 — 28 February 2011 Product data sheet

1. General description

The PCA9605 is a monolithic CMOS integrated circuit for bus buffering in applications including I^{2}C-bus, SMBus, DDC, PMBus, and other systems based on similar principles.

The buffer extends the bus load limit by buffering both the SCL and SDA lines, allowing the maximum permissible bus capacitance on both sides of the buffer.

The PCA9605 includes a unidirectional buffer for the clock signal, and a bidirectional buffer for the data signal. Slave devices which employ clock stretching are therefore not supported.

In its most basic implementation, the buffer will allow an extended number of slave devices to be attached to one (or more) master devices. In this case, all master devices would be positioned on the Sxx_IN side of the PCA9605.

The direction pin (DIR) further enhances this function by allowing the unidirectional clock signal to be reversed, thus allowing master devices on both sides of the buffer.

The enable (EN) function allows sections of the bus to be isolated. Individual parts of the system can be brought on-line successively. This means a controlled start-up using a diverse range of components, operating speeds and loads is easily achieved.

2. Features and benefits

- Simple impedance isolating buffer for 2-wire buses
- 30 mA maximum static open-drain pull-down capability supports a wide range of bus standards
- Works with I^{2}C-bus (Standard-mode, Fast-mode, Fast-mode Plus), SMBus (standard and high power mode), and PMBus
- Fast switching times allow operation in excess of 1 MHz
- Enable allows bus segments to be disconnected
- Hysteresis on inputs provides noise immunity
- Operating voltages from 2.7 V to 5.5 V
- Very low supply current
- Uncomplicated characteristics suitable for quick implementation in most common 2-wire bus applications

3. Applications

- Electronic signs and displays
- Lighting control (including architectural and stage lighting)
- Game consoles/boxes
- Gaming machine networks
- Building automation
- TV/projector/monitor interconnection (DDC)
- Power management systems
- Desktop and portable computers
- Security systems
- Interfacing standard 3 mA I^2C-bus parts to a 30 mA Fm+ bus

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9605D	PCA9605	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9605DP	9605	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

5. Block diagram

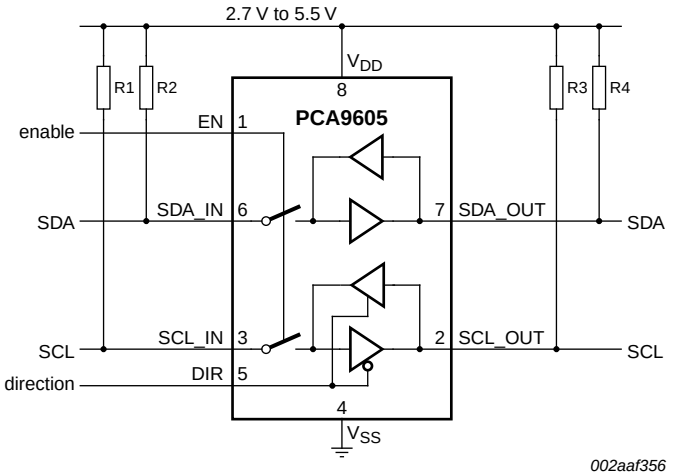


Fig 1. Block diagram of PCA9605

6. Pinning information

6.1 Pinning

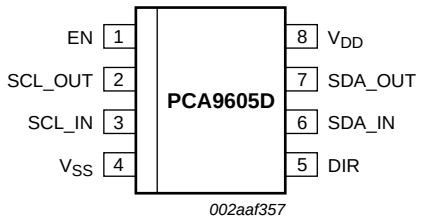


Fig 2. Pin configuration for SO8

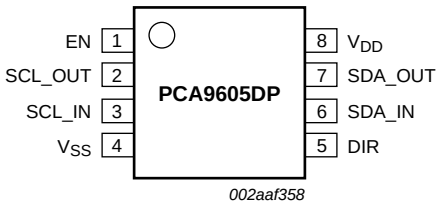


Fig 3. Pin configuration for TSSOP8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
EN	1	enable
SCL_OUT	2	clock buffer, slave side
SCL_IN	3	clock buffer, master side
V_{SS}	4	supply ground
DIR	5	clock direction
SDA_IN	6	data buffer, master side
SDA_OUT	7	data buffer, slave side
V_{DD}	8	positive supply

7. Functional description

Refer to Figure 1 “Block diagram of PCA9605”.

7.1 V_{DD}, V_{SS} — supply pins

The power supply voltage for the PCA9605 may be any voltage in the range 2.7 V to 5.5 V. The IC supply must be common with the supply for the bus. Hysteresis on the ports is a percentage of the IC’s power supply, hence noise margin considerations should be taken into account when selecting an operating voltage.

7.2 SCL_IN, SCL_OUT — clock signal inputs/outputs

The clock signal buffer is unidirectional, although the direction may be reversed under control of the direction pin (DIR). In normal bus operations, for example the I^2C-bus, the master device generates a unidirectional clock signal to the slave. For lowest cost, the PCA9605 combines unidirectional buffering of the clock signal with a bidirectional buffer for the data signal. Clock stretching is therefore not supported and slave devices that may require clock stretching must be accommodated by the master adopting an appropriate

clocking when communicating with them. The buffer includes hysteresis to ensure clean switching signals are output, especially with slow rise times on high capacitively loaded buses. Output ports are open-drain type and require external pull-up resistors.

7.3 SDA_IN, SDA_OUT — data signal inputs/outputs

The data signal buffer is bidirectional. The port (SDA_IN, SDA_OUT) which first falls below the 'lock voltage' V_{lock}, will take control of the buffer direction and 'lock out' signals coming from the opposite side. As the 'input' signal continues to fall, it will then drive the 'output' side LOW. Again, hysteresis is applied to the buffer to minimize the effects of noise.

At some points during the communication, the data direction will reverse, e.g., when the slave transmits an acknowledge (ACK), or responds with its register contents. During these times, the controlling 'input' side will have to rise back above the 'unlock voltage' (V_{unlock}) before it releases the 'lock', which then allows the 'output' side to gain control, and pull (what was) the 'input' side LOW again. This will cause a 'pulse' on the 'input' side, which can be quite a long duration in high capacitance buses. However, this pulse will not interfere with the actual data transmission, as it should not occur during times of clock line transition (during normal I^2C-bus and SMBus protocols), and thus data signal set-up time requirements are still met. Ports are open-drain type and require external pull-up resistors.

7.4 Enable (EN) — activate buffer operations

The active HIGH enable input (EN) can be used to disable the buffer, for the purpose of isolating sections of the bus. The IC should only be disabled when the bus is idle. This prevents truncation of commands which may confuse other devices on the bus. Enable (EN) may also be used to progressively activate sections of the bus during system start-up. Bus sections slow to respond on power-up can be kept isolated from the main system to avoid interference and collisions. The pin must be externally driven to a valid state.

7.5 Direction (DIR) — clock buffer direction control

The direction input (DIR) is used to change the signal direction of the SCL ports. When the DIR pin is logic LOW, the clock signal input is SCL_IN and the buffered output is SCL_OUT. When the DIR pin is logic HIGH, the clock signal input is SCL_OUT and the buffered output is SCL_IN. The pin must be externally driven to a valid state.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[1]	−0.3	+7	V
V_n	voltage on any other pin		[1]	V_{SS} − 0.5	V_{DD} + 0.5	V
$I_{I/O}$	input/output current	any pin		-	50	mA
P_{tot}	total power dissipation			-	300	mW
T_{stg}	storage temperature			−55	+125	°C
T_{amb}	ambient temperature	operating		−40	+85	°C

[1] Voltages are specified with respect to pin 4 (V_{SS}).

9. Characteristics

Table 4. Characteristics

T_{amb} = −40 °C to +85 °C; voltages are specified with respect to ground (V_{SS}); V_{DD} = 5.5 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
V_{DD}	supply voltage	operating		2.7	-	5.5	V
I_{DD}	supply current	quiescent; V_{DD} = $V_{I(EN)}$ = 5.5 V		-	-	1	µA
		SCL_IN, SDA_IN = 800 kHz; V_{DD} = 5.5 V	[1]	-	170	-	µA
Buffer ports (SDA_IN, SCL_IN, SDA_OUT, SCL_OUT)							
$V_{I2C\text{-}bus}$	I^2C-bus voltage			-	-	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage	V_{DD} = 2.7 V	[2]	-	-	0.4	V
		V_{DD} = 5.5 V	[2]	-	-	0.5	V
V_{IH}	HIGH-level input voltage	V_{DD} = 2.7 V	[2]	1.2	-	-	V
		V_{DD} = 5.5 V	[2]	2.0	-	-	V
$V_{I(hys)}$	hysteresis of input voltage	V_{DD} = 2.7 V	[2]	80	-	-	mV
		V_{DD} = 5.5 V	[2]	200	-	-	mV
I_{LI}	input leakage current	$V_{I2C\text{-}bus}$ = V_{DD} or GND		−1	-	+1	µA
$I_{O(sink)}$	output sink current	LOW-level; $V_{I2C\text{-}bus}$ < V_{IL}		30	-	-	mA
V_{OL}	LOW-level output voltage	I_{OL} = 30 mA		-	80	300	mV
		I_{OL} = 100 µA		-	1	-	mV
Pins SDA_IN, SDA_OUT							
V_{lock}	direction lock voltage	V_{DD} = 2.7 V	[2]	-	-	1.3	V
		V_{DD} = 5.5 V	[2]	-	-	3.0	V
V_{unlock}	direction unlock voltage	V_{DD} = 2.7 V	[2]	2.0	-	-	V
		V_{DD} = 5.5 V	[2]	4.8	-	-	V

Table 4. Characteristics *...continued*

T_{amb} = −40 °C to +85 °C; voltages are specified with respect to ground (V_{SS}); V_{DD} = 5.5 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Enable (EN)							
$V_{th(en)}$	enable threshold voltage	EN active; V_{DD} = 2.7 V		2.0	-	-	V
		EN active; V_{DD} = 5.5 V		4.8	-	-	V
$V_{th(dis)}$	disable threshold voltage	EN standby; V_{DD} = 2.7 V		-	-	0.9	V
		EN standby; V_{DD} = 5.5 V		-	-	2.1	V
V_{hys}	hysteresis voltage	V_{DD} = 2.7 V		100	-	-	mV
		V_{DD} = 5.5 V		200	-	-	mV
I_{LI}	input leakage current	$V_{I(EN)} = V_{DD}$		-	-	±0.1	µA
Direction (DIR)							
$V_{I(dir)}$	direction input voltage	direction SCL_OUT to SCL_IN					
		V_{DD} = 2.7 V		2.0	-	-	V
		V_{DD} = 5.5 V		4.8	-	-	V
		direction SCL_IN to SCL_OUT					
		V_{DD} = 2.7 V		-	-	0.9	V
		V_{DD} = 5.5 V		-	-	2.1	V
V_{hys}	hysteresis voltage	V_{DD} = 2.7 V		100	-	-	mV
		V_{DD} = 5.5 V		200	-	-	mV
I_{LI}	input leakage current	$V_{DIR} = V_{DD}$		-	-	±0.1	µA
Timing characteristics (Figure 4)							
t_d	delay time	R_{PU} = 200 Ω	[1]	-	70	-	ns
t_f	fall time	R_{PU} = 200 Ω	[1]	-	16	-	ns

[1] Guaranteed by design, not subject to test.

[2] Supply voltage dependent; refer to graphs (Figure 5 through Figure 8) for typical trend.

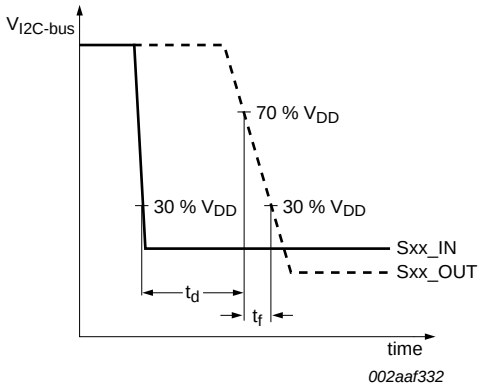
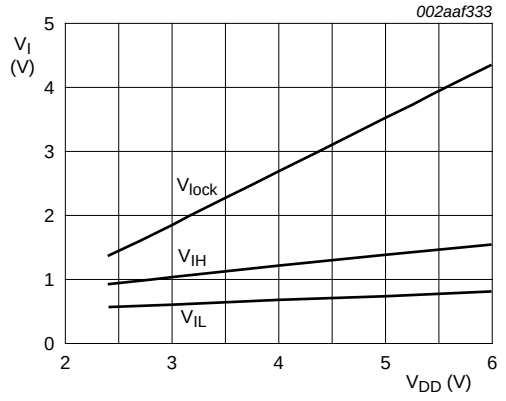


Fig 4. Timing diagram



T_{amb} = 25 °C

Fig 5. Typical input levels versus supply voltage

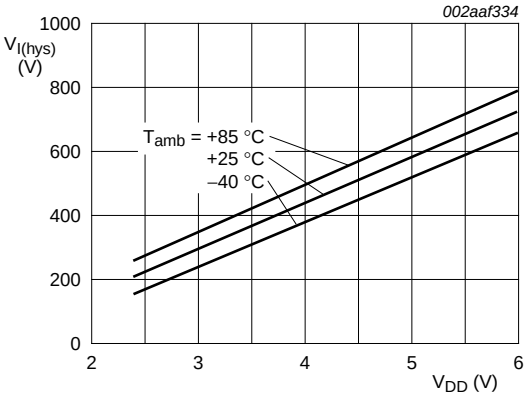
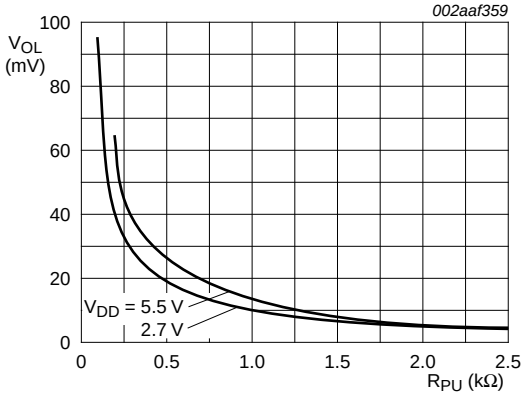
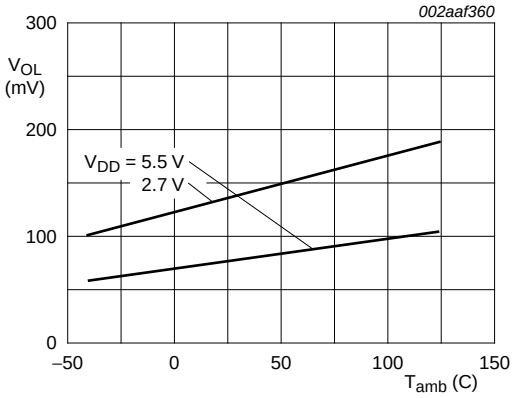


Fig 6. Typical $V_{IH} - V_{IL}$ hysteresis versus supply voltage



T_{amb} = 25 °C

Fig 7. Typical LOW-level output voltage versus pull-up resistance



I_{OL} = 30 mA

Fig 8. Typical LOW-level output voltage versus ambient temperature

9.1 Bidirectional data buffer

The bidirectional data buffer will determine which side has first fallen below V_{lock} and give that side of the buffer control over the direction of the buffer. For the purpose of this one LOW-going pulse, that side now becomes the 'input' (be it SDA_IN or SDA_OUT).

When the 'input' side falls to near V_{IL}, it will begin to drive the 'output' side of the buffer LOW. It will continue to hold the 'output' low until the 'input' exceeds V_{IH} at which point the 'output' is released and will rise as fast as it is permitted by the load and pull-up to which it is attached. (Assuming, of course, that the 'output' is not otherwise held LOW by some other device on the bus on that side of the buffer.)

When the 'input' side again exceeds V_{unlock}, it will release its control of the buffer direction. At this point, if the 'output' side was being held LOW (< V_{unlock}) by another device, it will immediately gain control and now become the 'input'. What was the 'input' will now become the 'output', and the process will repeat as above, but in the opposite direction.

This means that as direction control is handed from one side of the buffer to the other, a voltage 'spike' of about V_{unlock} volts will appear on the side that was the 'input' and became the 'output'.

Figure 9 shows clock and data being buffered through the PCA9605. Channel 3 shows the SDA_IN port, with direction 'hand over' spike (upper left corner). The level of the SDA_OUT port (channel 4) can be seen to increase as it goes from being held LOW by the buffer, to being held LOW by another device on the bus.

Of course, the information on the SDA line is only latched into an I^2C-bus device on a clock edge. The spike on the data line does not occur at a time when data is being latched, and thus the set-up and hold conditions are still met for a valid I^2C-bus transaction.

Figure 9 also shows a glitch occurring on the SDA_OUT port (upper right corner). A more drastic example is shown in Figure 10. In this case, the side acting as the 'input' (SDA_OUT) is more lightly loaded than the side acting as the 'output' (SDA_IN). It therefore rises quickly to V_{unlock} level, before the SDA_IN has been able to exceed V_{IL}. Direction control briefly reverses, and SDA_OUT gets pulled back LOW again until SDA_IN has exceeded V_{IH}.

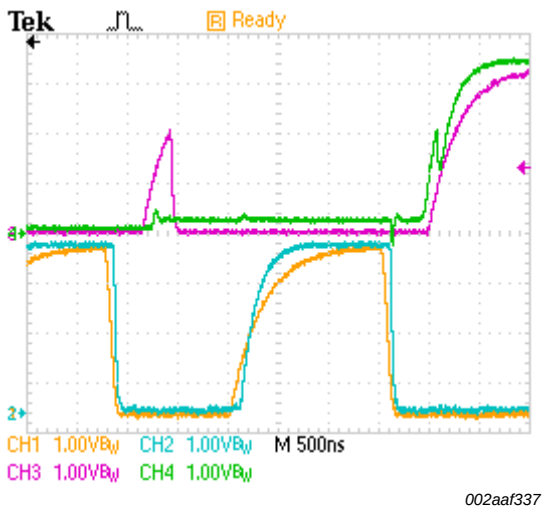


Fig 9. 'Hand over' spikes on the data bus

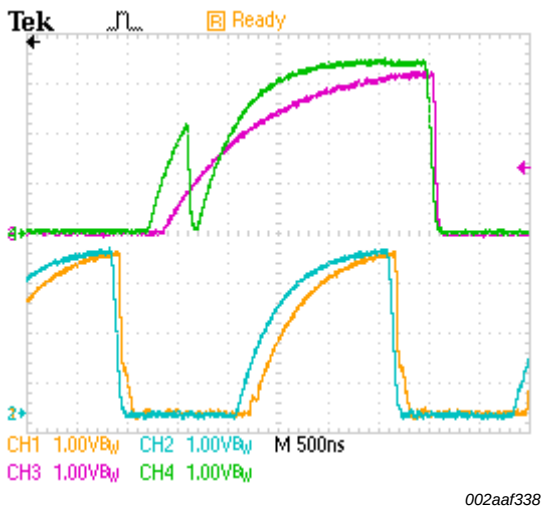


Fig 10. Fast rising SDA_xx 'input' side

Figure 11 shows that by choosing an appropriate value of pull-up resistance (or adding additional load capacitance if that is preferred), the rate of rise of both input and output can be matched, and the glitch on the rising edge eliminated.

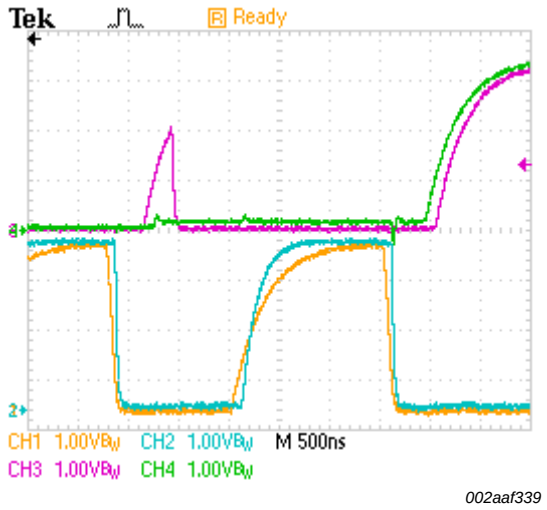


Fig 11. Matched 'input' and 'output' rise times

9.2 Operating conditions

A full byte transaction is shown in Figure 12. SDA_IN and SDA_OUT are shown at the top of the image, and SCL_IN and SCL_OUT are shown at the bottom. The START condition, address bits, read/write bit, acknowledge bit and STOP condition can all be clearly seen.

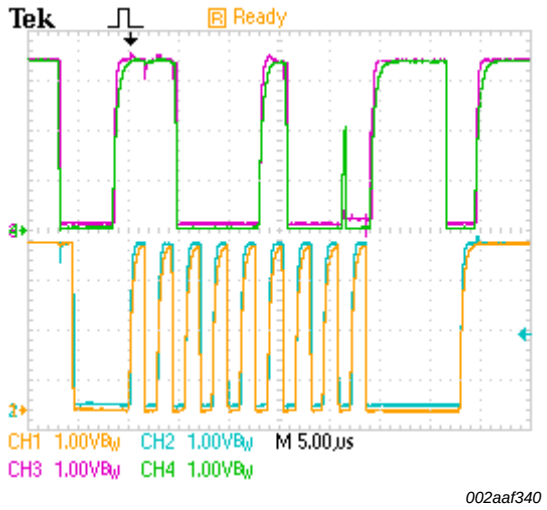
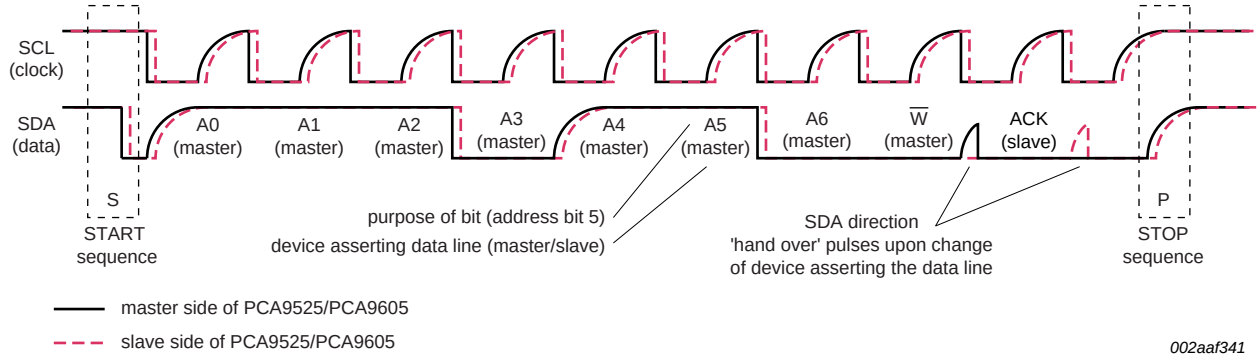


Fig 12. Full 400 kHz I²C-bus address byte transaction

10. Application information

10.1 Design considerations

Figure 13 shows a typical data transfer through the PCA9605. The PCA9605 has excellent application to extending loads and providing interfaces to connectors on high speed microprocessor cards. PCA9605 can operate well in excess of the Fast-mode 400 kHz I^2C-bus specification (Ref. 1), and is compatible with the Fast-mode Plus specification. Rise times are determined simply by the side of the buffer with the slowest RC time constant.



Remark: Input to output delay exaggerated for clarity.

Fig 13. Typical communication sequence through the PCA9605

Figure 14 shows a typical application for the PCA9605. In most applications there will be a single master on the Sxx_IN side of the buffer. One or more PCA9605s can be connected to this master, giving multiple isolated bus sections on which the slaves are located. Each bus section can have the maximum permissible load capacitance, and this capacitance will not influence any other bus section.

The master can control the enable (EN) signals such that each bus section can be independently activated. This allows for slaves sharing the same address to be placed on different bus sections and thus uniquely addressed.

The enable pin (EN) can similarly be used to interface buses of different operating frequencies. When certain bus sections are enabled, the system frequency may be limited by a bus section having a slave device specified only to 400 kHz (Fast-mode). When that bus section is disabled, the slow slave is isolated and the remaining bus can be run at 1 MHz (Fast-mode Plus).

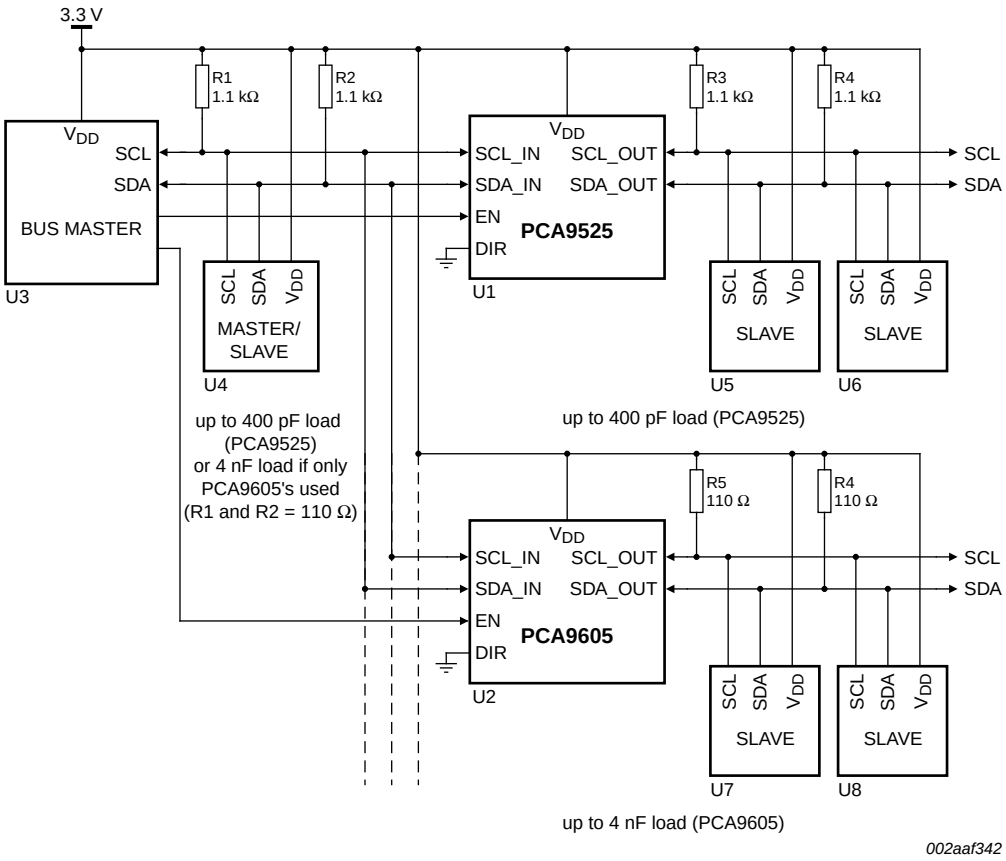


Fig 14. PCA9605 typical buffer application

Figure 15 shows the PCA9605 used with masters on both sides of the buffer. More than one master may be used on the Sxx_IN side of the IC. However, to locate a master on the Sxx_OUT side and have that master be able to communicate with devices on the Sxx_IN side, it must either have direct control over the direction pin (DIR) of the PCA9605, or it must request another controlling master to change the direction. In Figure 15, U4 uses an IRQ to signal to U2 that requests a direction change. Once in control, it could alternatively use the bus to signal 'release of control'.

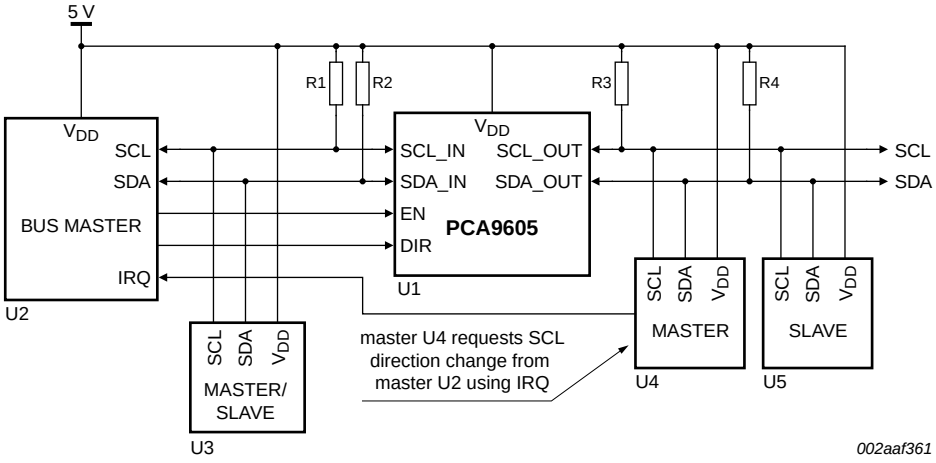


Fig 15. PCA9605 with masters on both sides of buffer

Multiplexers such as the PCA9544A are simple analog switches which provide no capacitive load isolation between connected branches. Figure 16 shows the PCA9605 enhancing an I^2C-bus multiplexer application by isolating the load capacitance of each branch. Figure 17 and Figure 18 show alternate forms of bus multiplexing, with the latter being an excellent way to eliminate the requirement for a master to dedicate pins to enabling multiple PCA9605 devices.

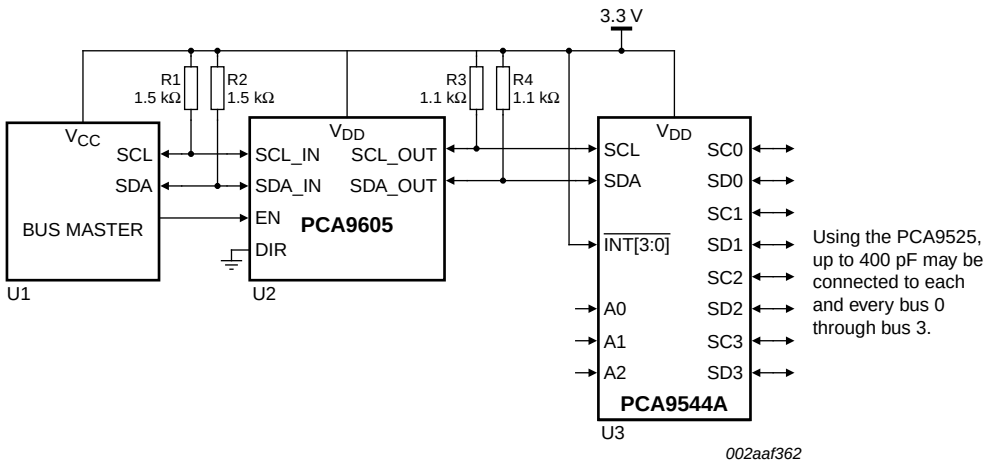


Fig 16. PCA9605 multiplexer isolation application

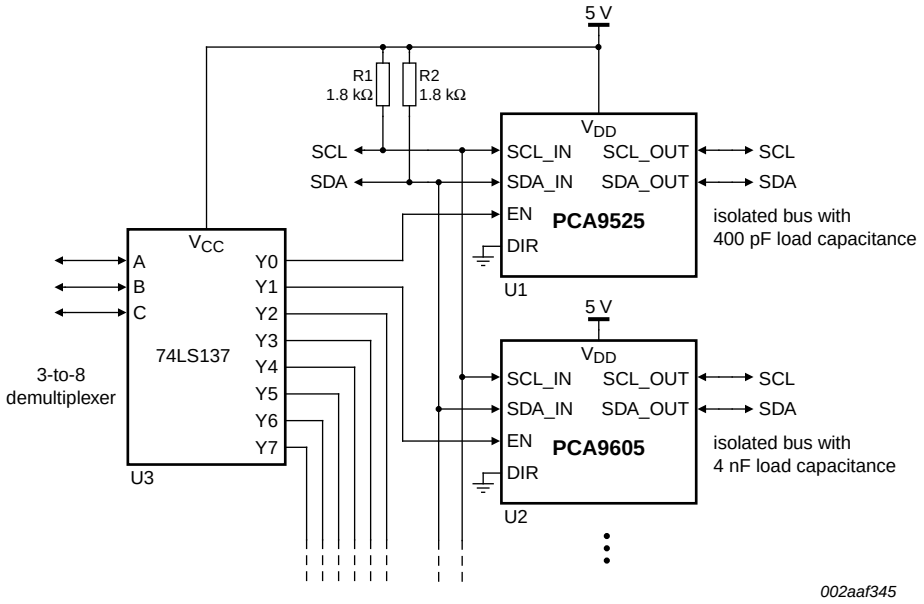


Fig 17. PCA9605 bus multiplexer application driven from a simple logic device

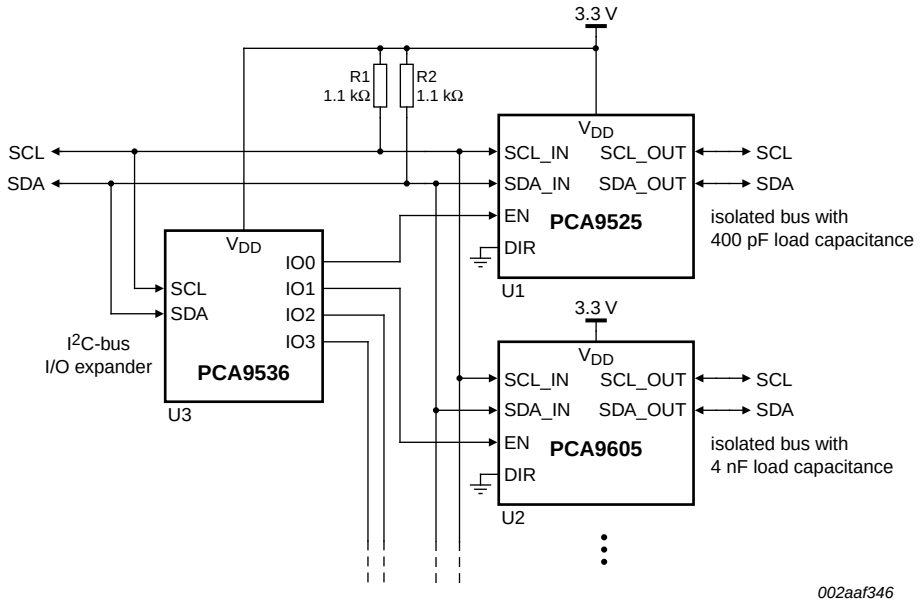
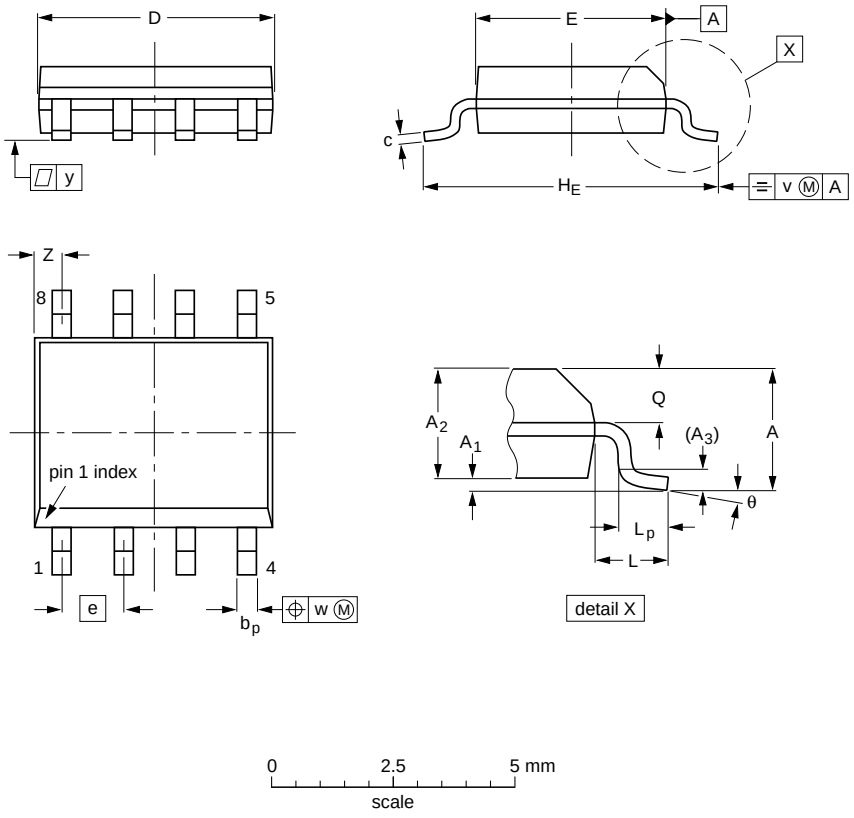


Fig 18. PCA9605 bus multiplexer application driven from an I²C-bus I/O expander

11. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

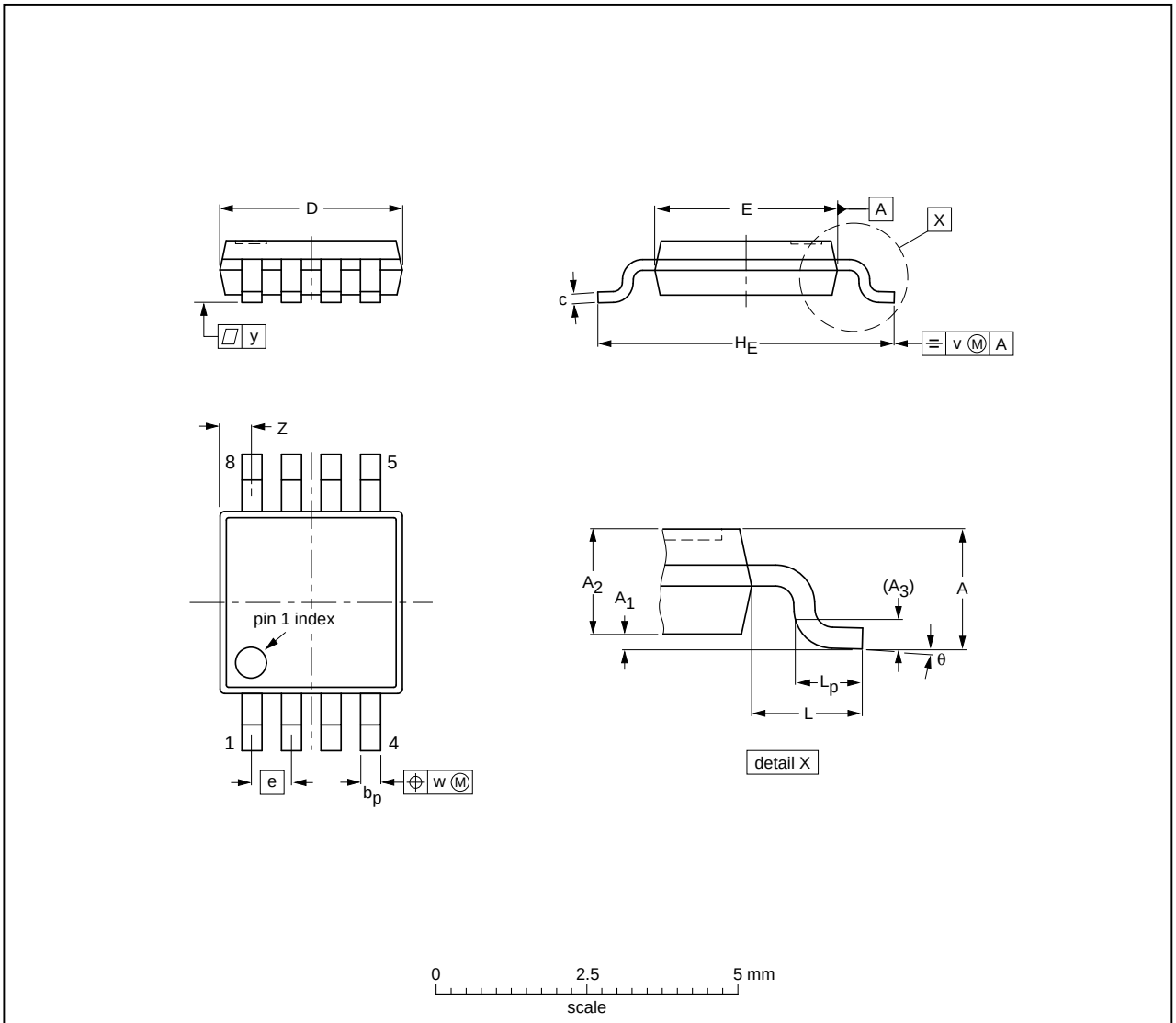
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 19. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 20. Package outline STO505-1 (TSSOP8)

12. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 5 and 6

Table 5. SnPb eutectic process (from J-STD-020C)

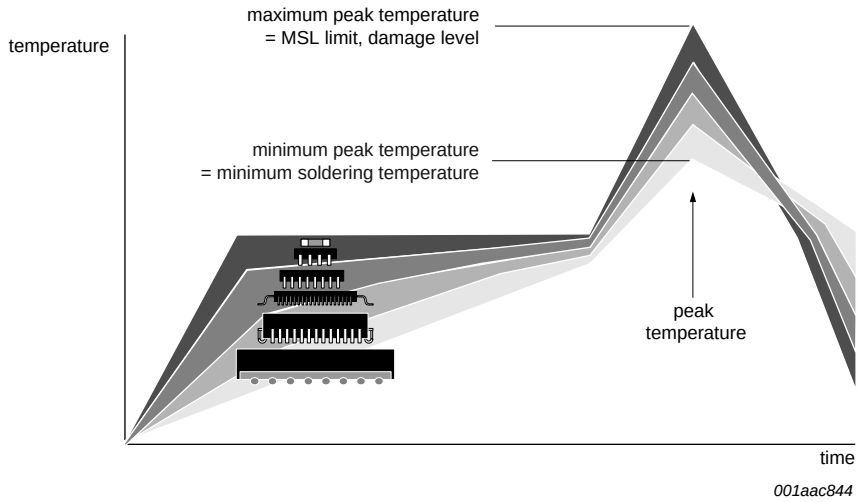
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 6. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.



MSL: Moisture Sensitivity Level

Fig 21. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 7. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DDC	Data Display Channel
Fm+	Fast-mode Plus
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
PMBus	Power Management Bus
SCL	Serial Clock Line
SDA	Serial Data Line
SMBus	System Management Bus

15. References

[1] **UM10204, I^2C-bus specification and user manual —** , Rev 03, 19 June 2007; NXP B.V. www.nxp.com/documents/user_manual/UM10204.pdf

[2] **System Management Bus (SMBus) Specification —** Version 2.0, August 3, 2000; SBS Implementers Forum.

16. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9605 v.1	20110228	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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