

# PHB101NQ04T

## N-channel TrenchMOS standard level FET

Rev. 02 — 10 March 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources

### 1.3 Applications

- DC-to-DC convertors
- Motors, lamps and solenoids
- General industrial applications
- Uninterruptible power supplies

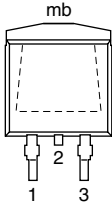
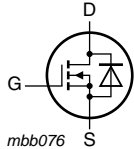
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	-	40	V
$I_D$	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 2</a>	-	-	157	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 11</a>	-	12.6	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	6.6	8	m $\Omega$

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT404 (D2PAK)</b></p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

**Table 3. Ordering information**

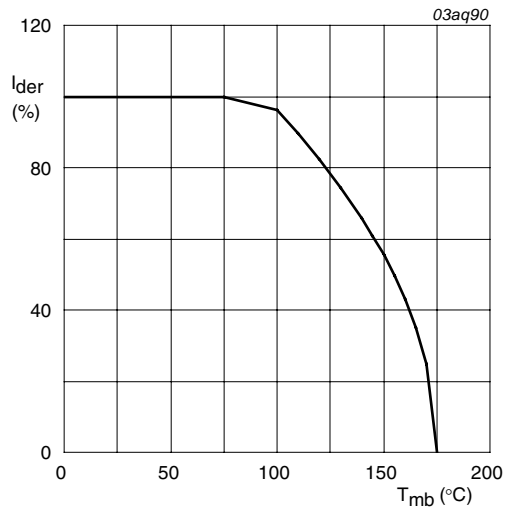
Type number	Package		Version
	Name	Description	
PHB101NQ04T	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

**Table 4. Limiting values**

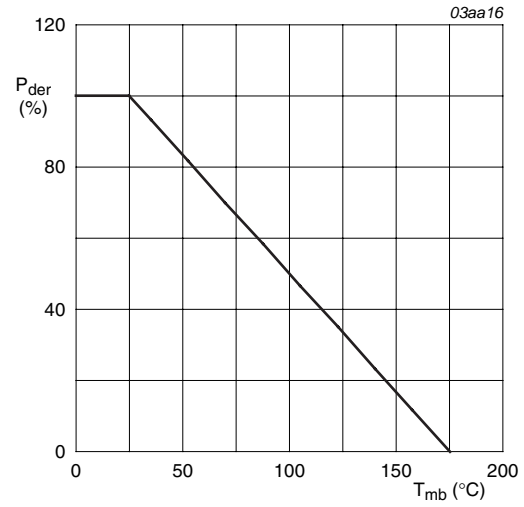
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	40	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	71	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	75	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	157	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 45\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; unclamped; $t_p = 0.17\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	200	mJ



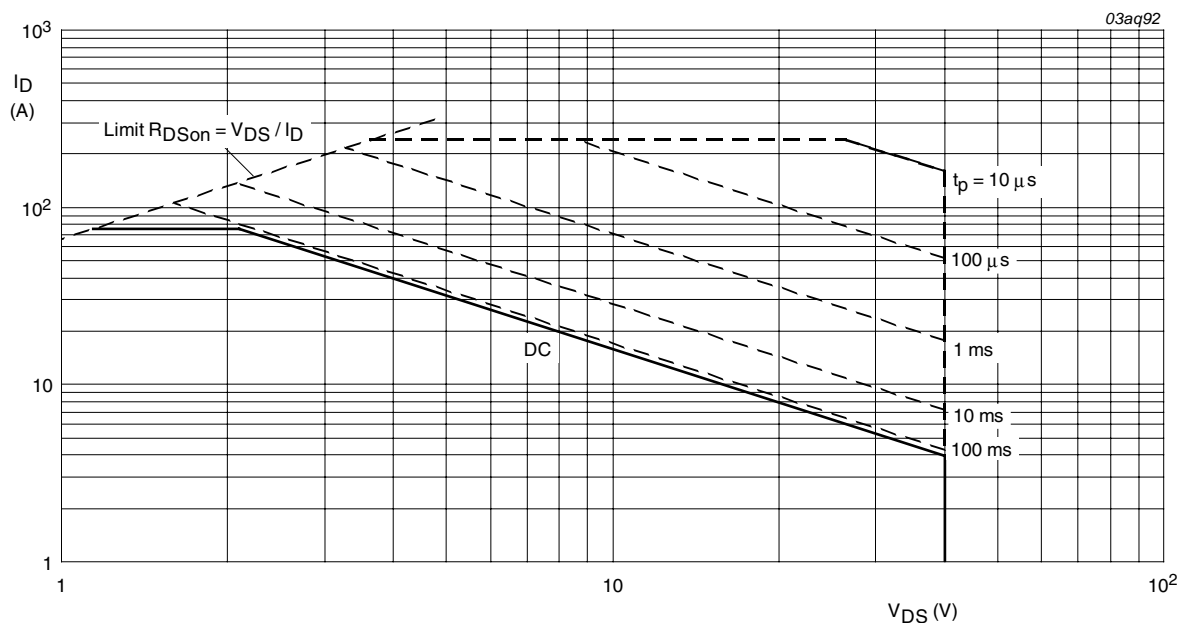
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



$$T_{mb} = 25^\circ\text{C}; I_{DM} \text{ is single pulse}; V_{GS} = 10\text{V}$$

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; vertical in still air;	-	50	-	K/W

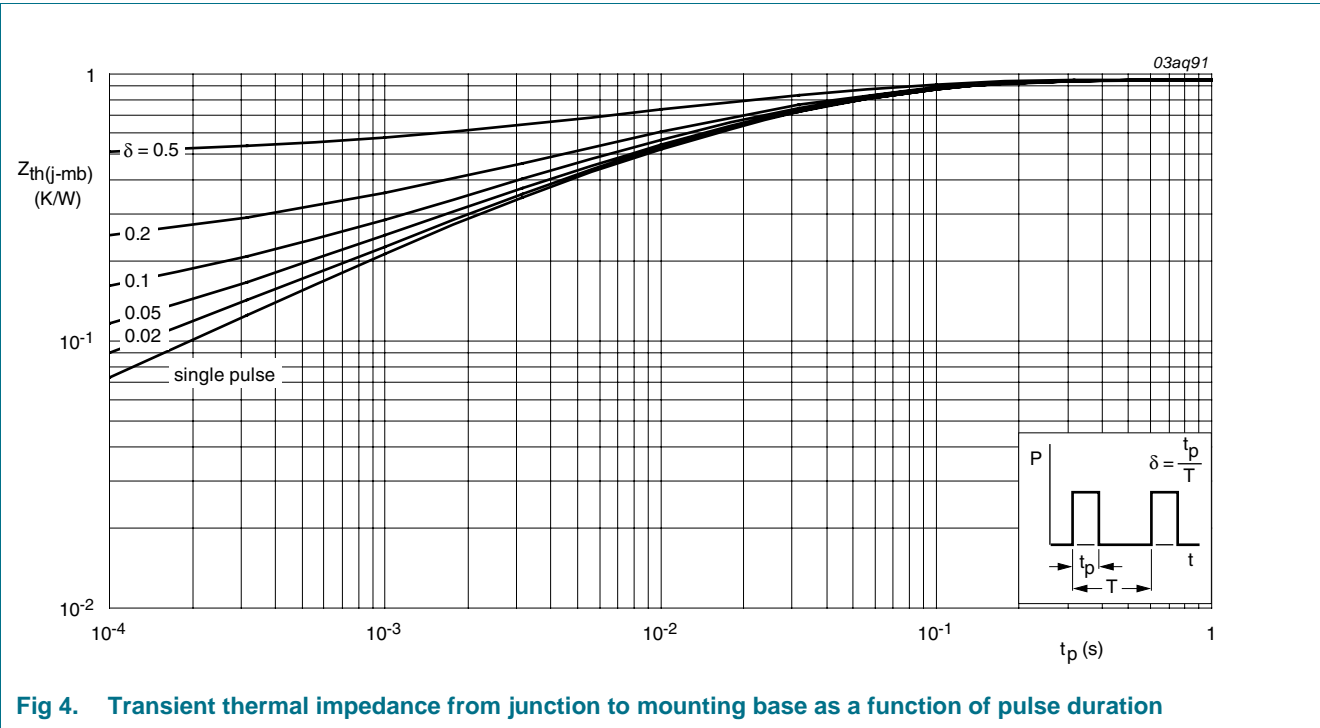


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	36	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	40	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	4.4	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	1	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	2	3	4	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	1	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	-	15.2	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	6.6	8	mΩ
Dynamic characteristics						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	-	36.6	-	nC
Q <sub>GS</sub>	gate-source charge		-	9.8	-	nC
Q <sub>GD</sub>	gate-drain charge		-	12.6	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	2020	-	pF
C <sub>oss</sub>	output capacitance		-	485	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	215	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 10 Ω; T <sub>j</sub> = 25 °C	-	20	-	ns
t <sub>r</sub>	rise time		-	51	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	51	-	ns
t <sub>f</sub>	fall time		-	33	-	ns
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C see <a href="#">Figure 13</a>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C	-	53	-	ns
Q <sub>r</sub>	recovered charge		-	44	-	nC

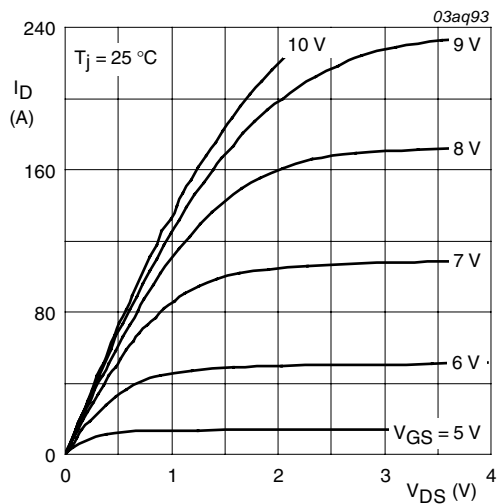


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

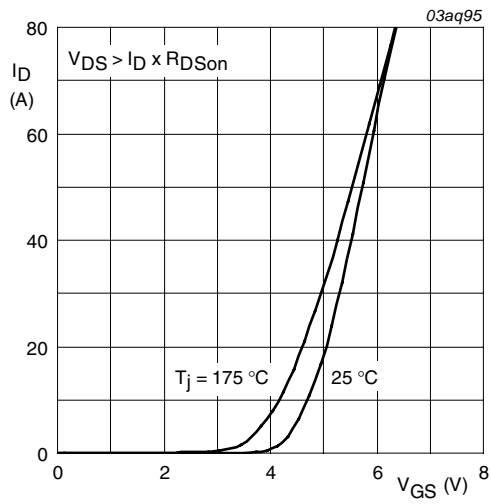


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

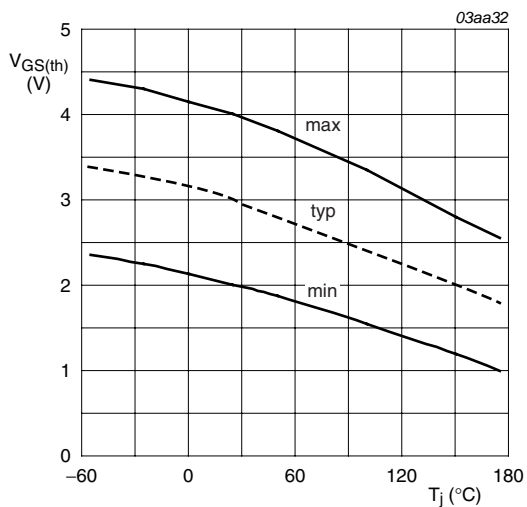


Fig 7. Gate-source threshold voltage as a function of junction temperature

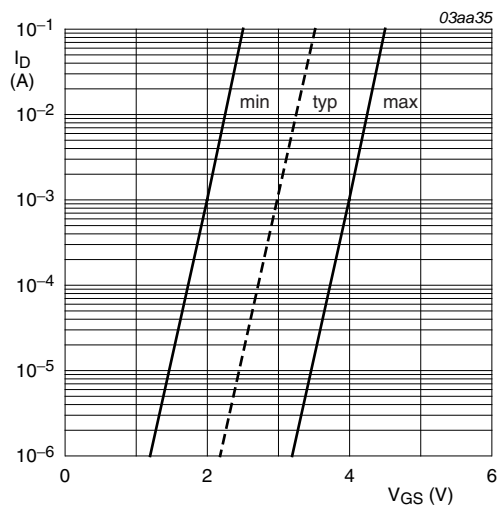
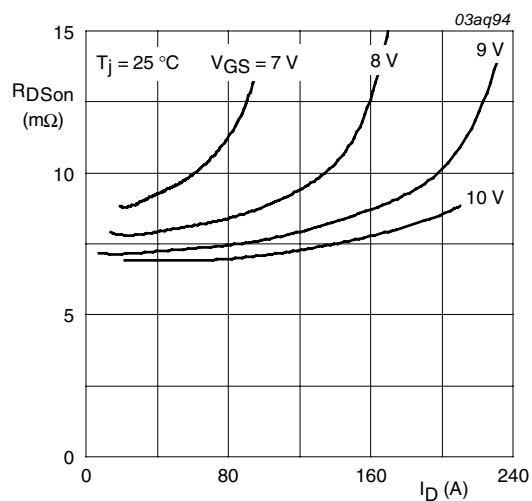
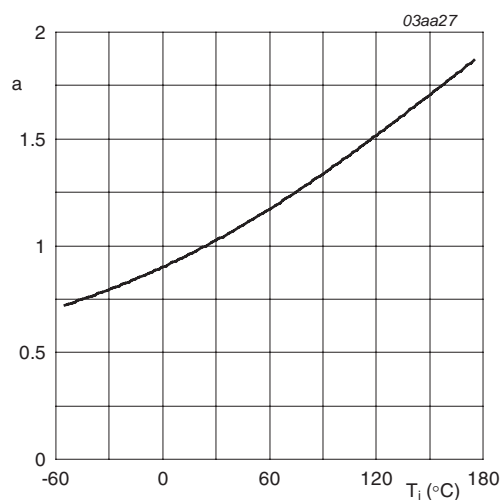


Fig 8. Sub-threshold drain current as a function of gate-source voltage



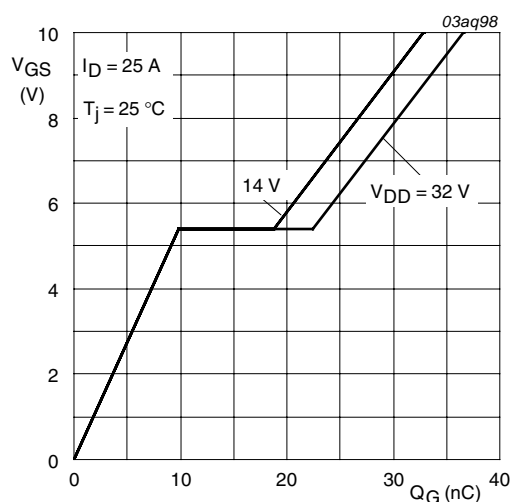
$$T_j = 25^{\circ}\text{C}$$

**Fig 9.** Drain-source on-state resistance as a function of drain current; typical values



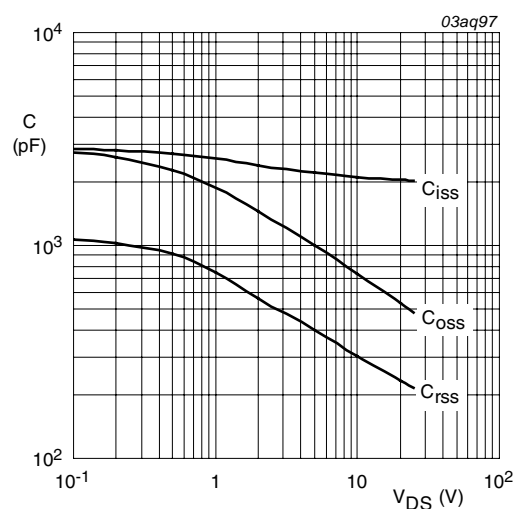
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^{\circ}\text{C})}}$$

**Fig 10.** Normalized drain-source on-state resistance factor as a function of junction temperature



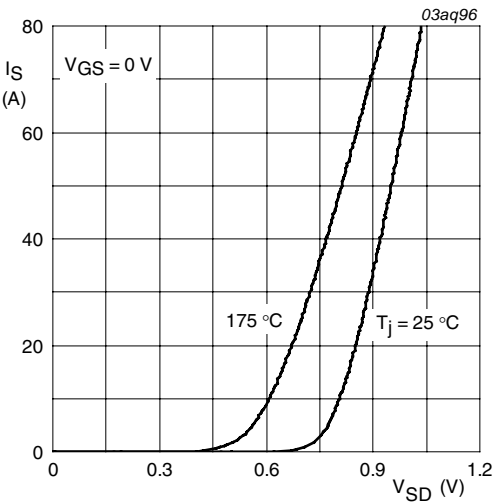
$$I_D = 25\text{A}; V_{DS} = 14\text{V and } 32\text{V}$$

**Fig 11.** Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

**Fig 12.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_J = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

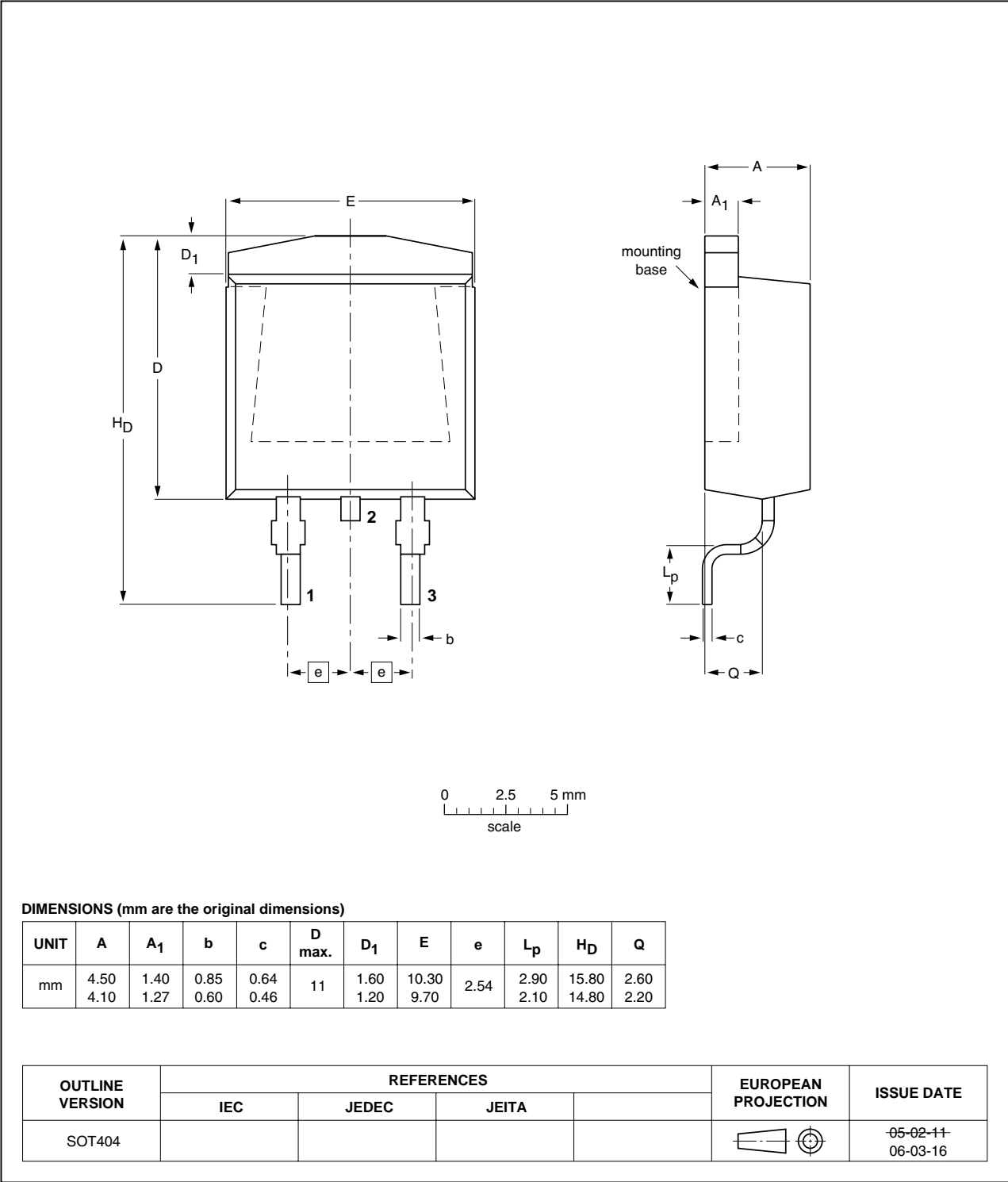


Fig 14. Package outline SOT404 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHB101NQ04T_2	20090310	Product data sheet	-	PHP_PHB101NQ04T-01
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number PHB101NQ04T separated from data sheet PHP_PHB101NQ04T-01.</li></ul>			
PHP_PHB101NQ04T-01 (9397 750 13167)	20040512	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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