

PHN210T

Dual N-channel TrenchMOS intermediate level FET

Rev. 02 — 15 December 2010

Product data sheet

1. Product profile

1.1 General description

Dual intermediate level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources
- Suitable for low gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor and relay drivers
- Logic level translators

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; Repetitive peak drain-source voltage	-	-	30	V
I_D	drain current	$T_{sp} = 25\text{ °C}$; Single device	[1]	-	3.4	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	[2]	-	2	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 1\text{ A}$; $T_j = 25\text{ °C}$	-	120	200	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 2.2\text{ A}$; $T_j = 25\text{ °C}$	-	80	100	m Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 2.3\text{ A}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ °C}$	-	0.7	-	nC

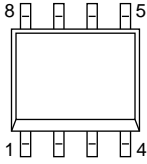
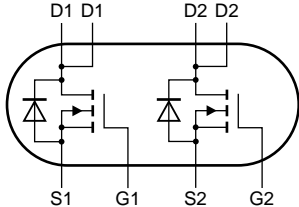
[1] Surface mounted on FR4 board, $t \leq 10\text{ sec}$.

[2] Surface mounted on FR4, $t \leq 10\text{ sec}$.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>SOT96-1 (SO8)</p>	 <p><i>mbk725</i></p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D	drain2		
6	D	drain2		
7	D	drain1		
8	D	drain1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHN210T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

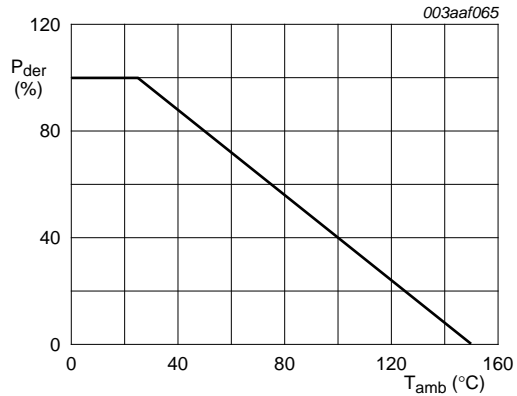
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	Continuous	-	30	V
		T _j ≥ 25 °C; T _j ≤ 150 °C; Repetitive peak drain-source voltage	-	30	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	T _{sp} = 70 °C; Dual device [1]	-	1.9	A
		T _{sp} = 70 °C; Single device [1]	-	2.8	A
		T _{sp} = 25 °C; Dual device [1]	-	2.4	A
		T _{sp} = 25 °C; Single device [1]	-	3.4	A
I _{DM}	peak drain current	T _{sp} = 25 °C; pulsed	-	14	A
P _{tot}	total power dissipation	T _{sp} = 25 °C [2]	-	2	W
T _{stg}	storage temperature		-65	150	°C
T _j	junction temperature		-65	150	°C
Source-drain diode					
I _S	source current	T _{sp} = 25 °C	-	2.2	A
I _{SM}	peak source current	T _{sp} = 25 °C; pulsed	-	14	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 3.4 A; V _{DD} ≤ 15 V; unclamped; R _{GS} = 50 Ω; t _p = 0.2 ms	-	13	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 15 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; unclamped	-	3.4	A

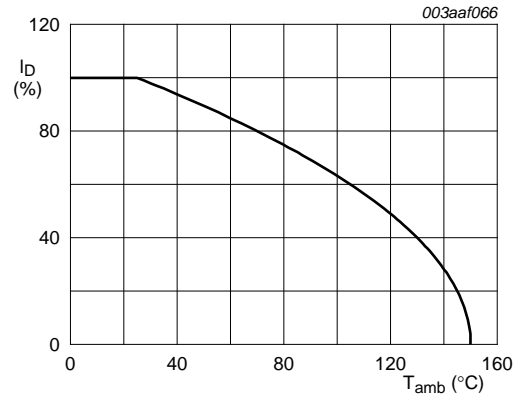
[1] Surface mounted on FR4 board, t ≤ 10 sec.

[2] Surface mounted on FR4, t ≤ 10 sec.



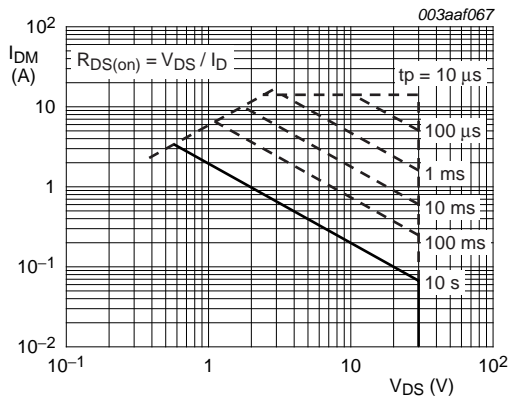
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of ambient temperature



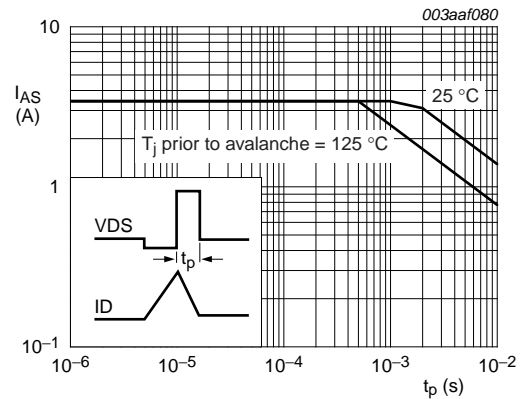
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature



$T_a = 25^{\circ}\text{C}$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



unclamped inductive load

Fig 4. Single-shot avalanche rating; avalanche current as a function of avalanche period

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Surface mounted; FR4 board	-	150	-	K/W
		Surface mounted; FR4 board; $t \leq 10$ sec	-	-	62.5	K/W

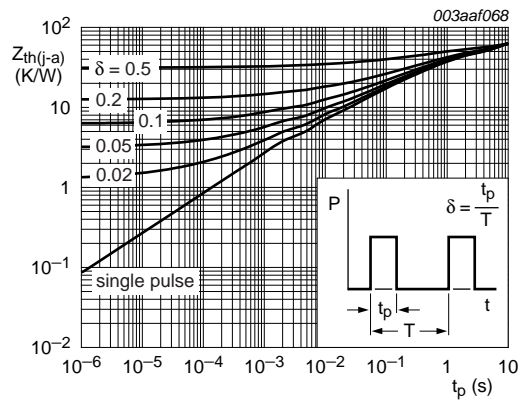


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 10 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	3.2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$	0.4	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1	2	2.8	V
I_{DSS}	drain leakage current	$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{DS} = 24 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	0.6	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 1 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	120	200	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 2.2 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	170	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 2.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	80	100	m Ω
$I_{D(son)}$	on-state drain current	$V_{DS} = 1 \text{ V}; V_{GS} = 10 \text{ V}$	3.5	-	-	A
		$V_{DS} = 5 \text{ V}; V_{GS} = 4.5 \text{ V}$	2	-	-	A
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 2.3 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	6	-	nC
Q_{GS}	gate-source charge		-	0.7	-	nC
Q_{GD}	gate-drain charge		-	0.7	-	nC
C_{iss}	input capacitance	$V_{DS} = 20 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	250	-	pF
C_{oss}	output capacitance		-	88	-	pF
C_{rss}	reverse transfer capacitance		-	54	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 18 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	6	-	ns
t_r	rise time		-	8	-	ns
$t_{d(off)}$	turn-off delay time		-	21	-	ns
t_f	fall time		-	15	-	ns
g_{fs}	transfer conductance	$V_{DS} = 20 \text{ V}; I_D = 2.2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	2	4.5	-	S
L_D	internal drain inductance	measured from drain lead to centre of die; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; $T_j = 25 \text{ }^\circ\text{C}$	-	5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 1.25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	69	-	ns
Q_r	recovered charge		-	55	-	nC

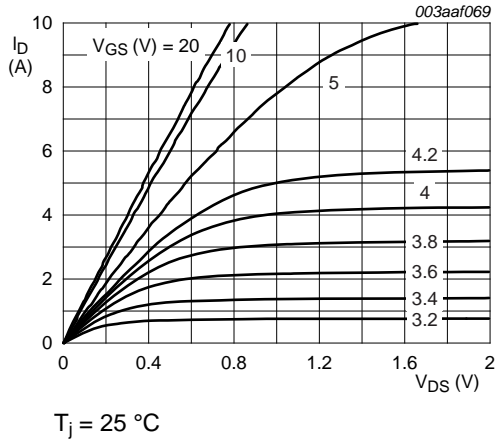


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

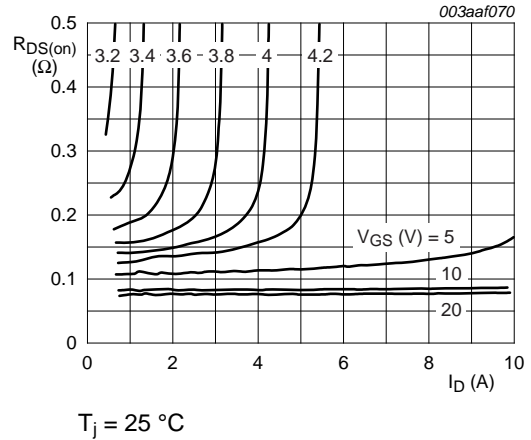


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

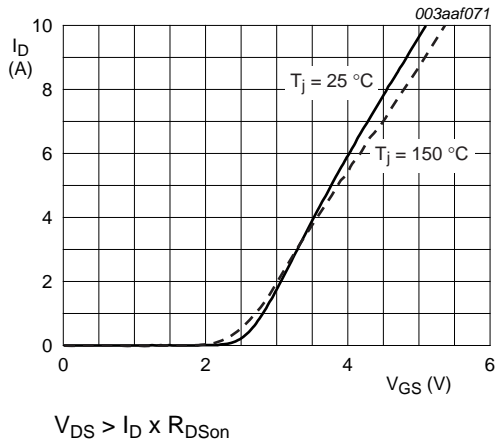


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

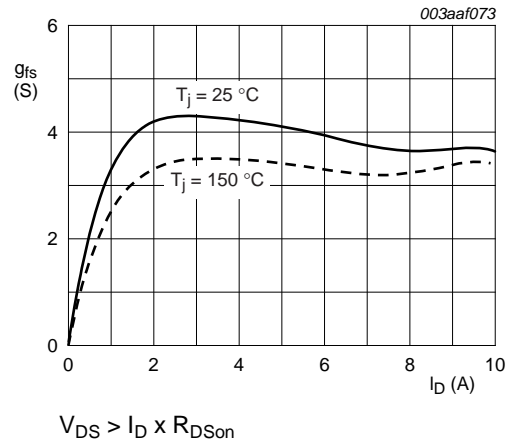


Fig 9. Forward transconductance as a function of drain current; typical values

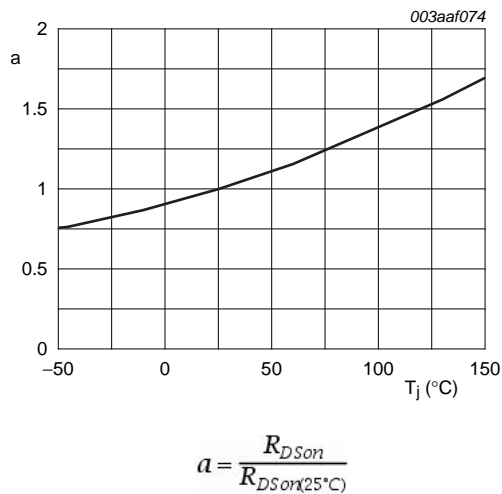


Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature

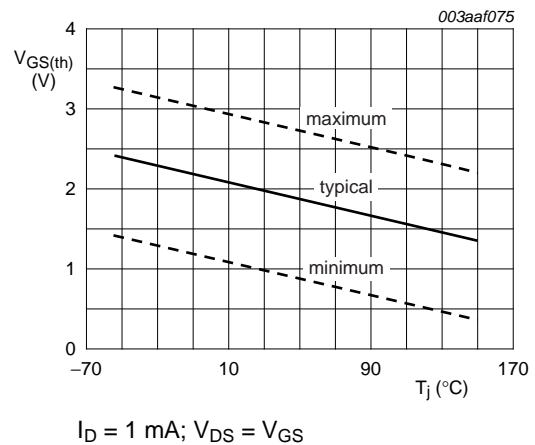
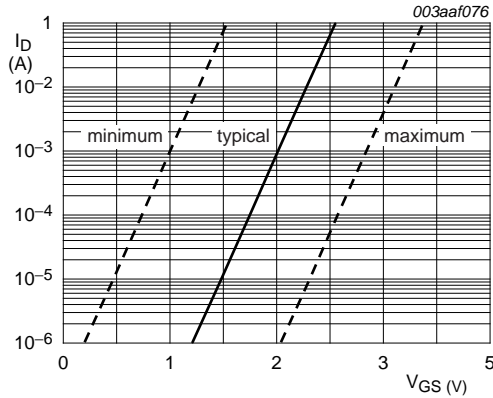
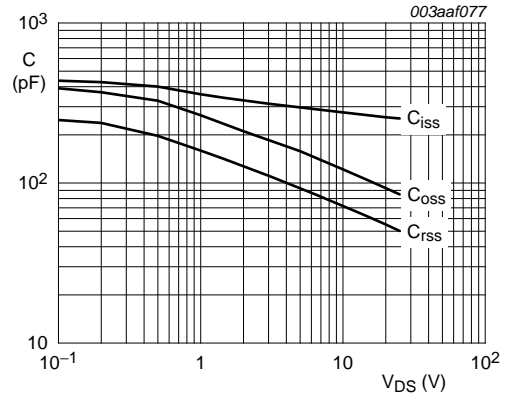


Fig 11. Gate-source threshold voltage as a function of junction temperature



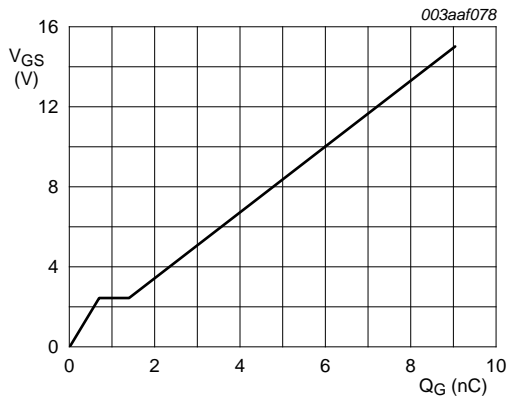
$T_j = 25\text{ }^\circ\text{C}$; $V_{DS} = V_{GS}$

Fig 12. Sub-threshold drain current as a function of gate-source voltage



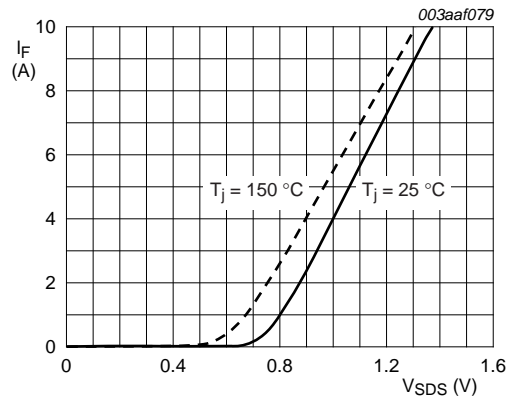
$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 2.3\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; $V_{DD} = 15\text{ V}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

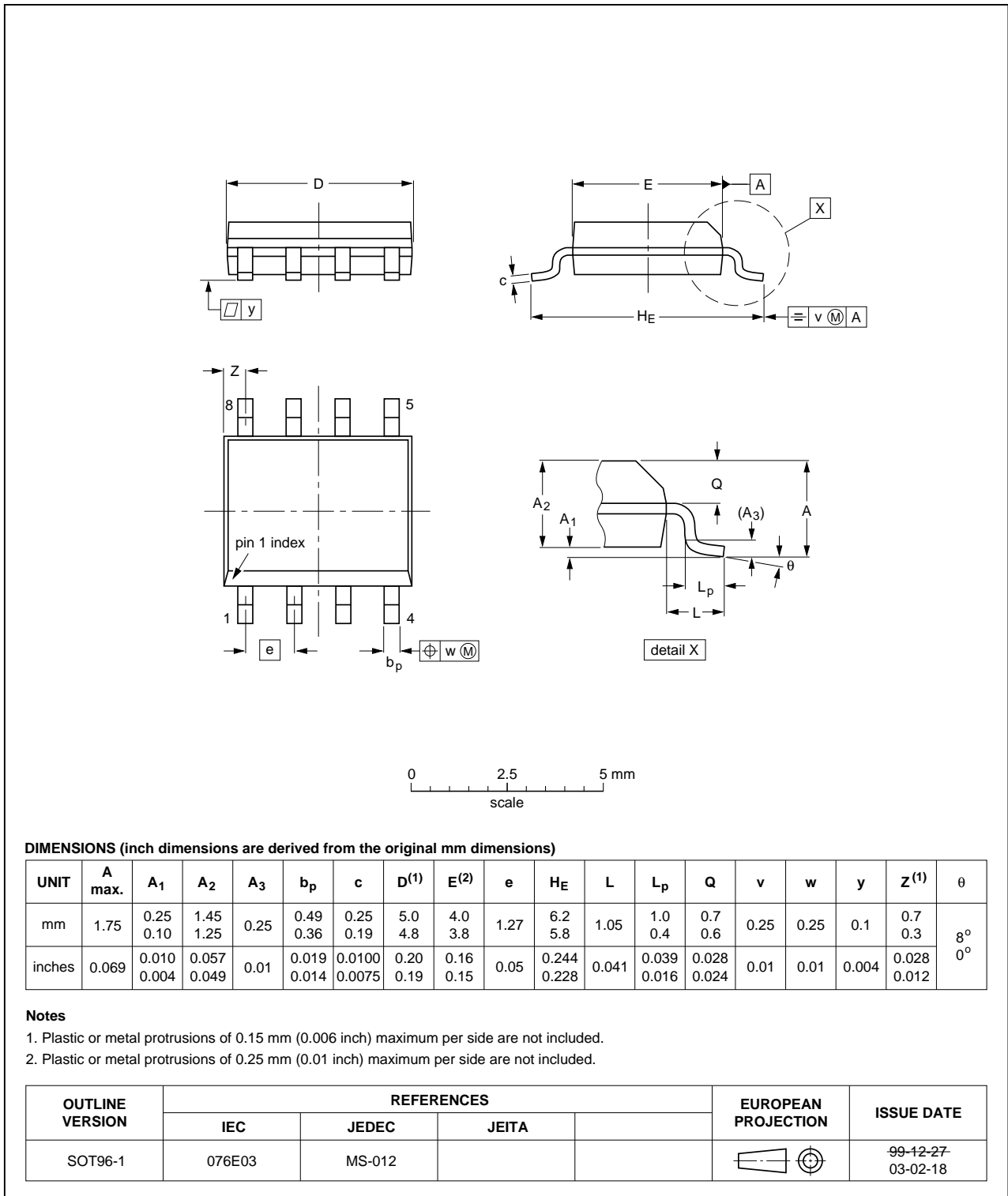


Fig 16. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHN210T v.2	20101215	Product data sheet	-	PHN210T v.1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.			
PHN210T v.1	19990301	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 15 December 2010

Document identifier: PHN210T