



PSMN6R0-30YLB

N-channel 30 V 6.5 mΩ logic level MOSFET in LPAK using NextPower technology

Rev. 2 — 24 October 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

1.4 Quick reference data

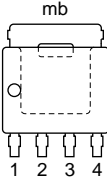
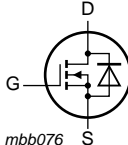
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	-	71	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	58	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12	-	6.9	8.1	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12	-	5.5	6.5	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; see Figure 14 ; see Figure 15	-	2.6	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; see Figure 14 ; see Figure 15	-	9	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK; Power-SO8)

3. Ordering information

Table 3. Ordering information

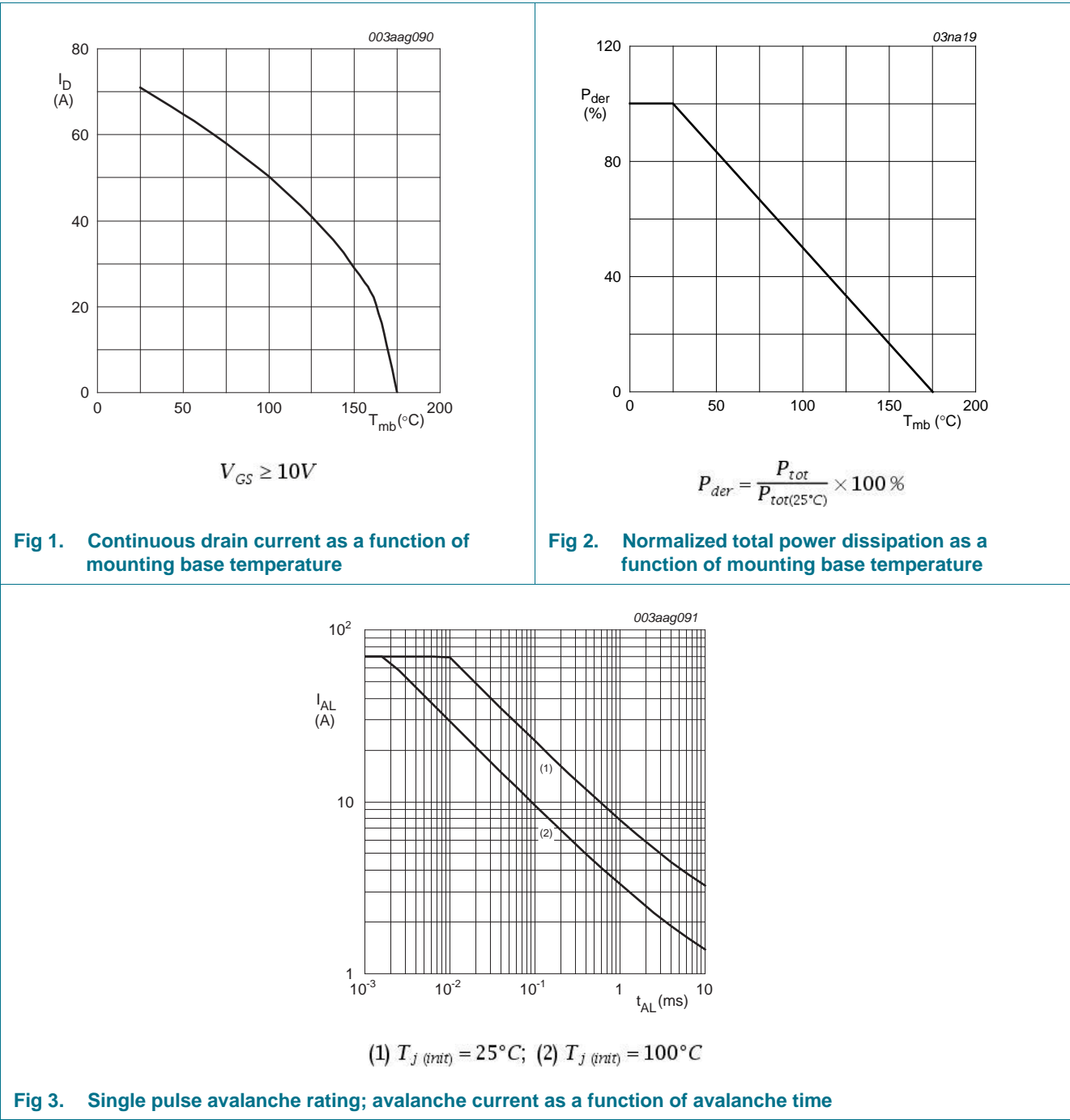
Type number	Package		Version
	Name	Description	
PSMN6R0-30YLB	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

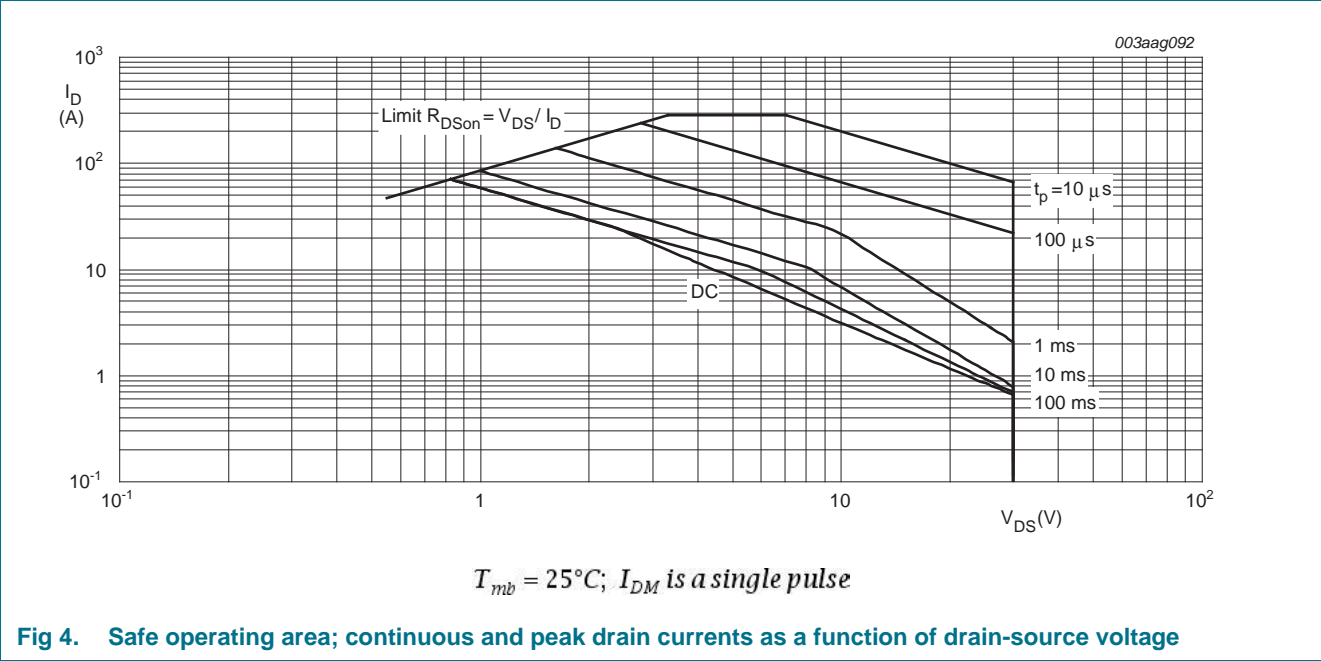
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	71	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	50	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 4	-	283	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	58	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	210	-	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	53	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	283	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 71\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; see Figure 3	-	13	mJ





5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	2.35	2.57	K/W

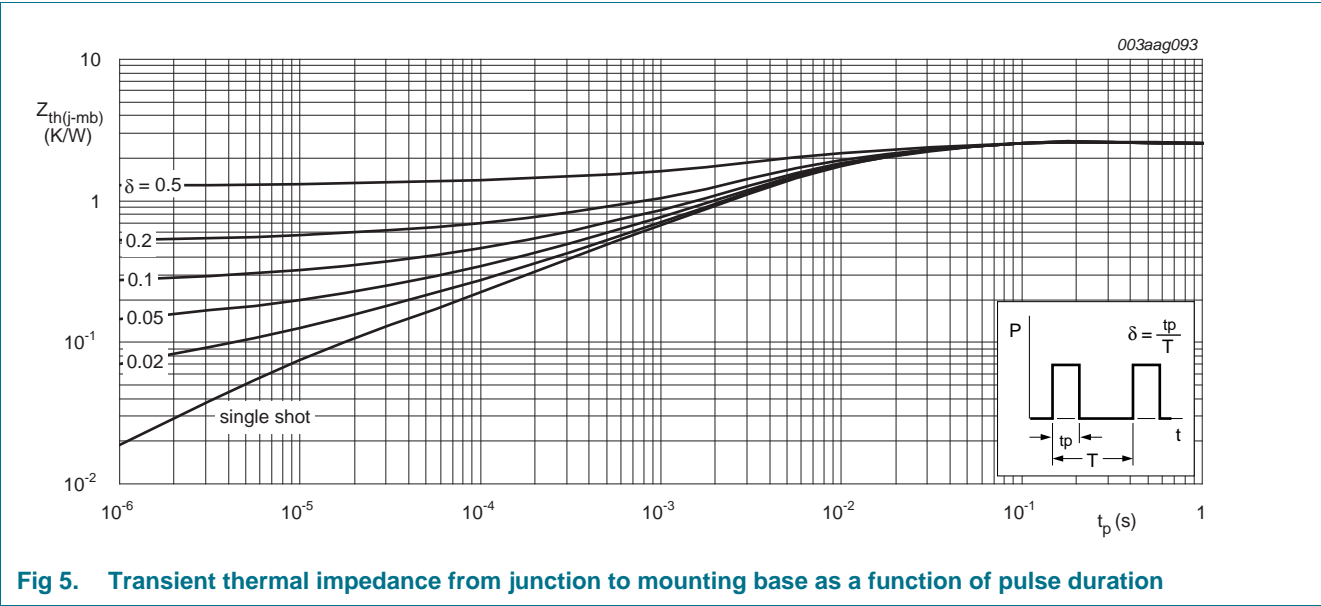


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	30	-	-	V
		$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$; $T_j = -55\ ^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ\text{C}$; see Figure 10 ; see Figure 11	1.05	1.48	1.95	V
		$I_D = 10\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = 150\ ^\circ\text{C}$	0.5	-	-	V
		$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; $T_j = -55\ ^\circ\text{C}$	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$; $T_j = 150\ ^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16\ \text{V}$; $V_{DS} = 0\ \text{V}$; $T_j = 25\ ^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}$; $I_D = 20\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 12	-	6.9	8.1	mΩ
		$V_{GS} = 4.5\ \text{V}$; $I_D = 20\ \text{A}$; $T_j = 150\ ^\circ\text{C}$; see Figure 12 ; see Figure 13	-	-	13.4	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 20\ \text{A}$; $T_j = 25\ ^\circ\text{C}$; see Figure 12	-	5.5	6.5	mΩ
		$V_{GS} = 10\ \text{V}$; $I_D = 20\ \text{A}$; $T_j = 150\ ^\circ\text{C}$; see Figure 12 ; see Figure 13	-	-	10.7	mΩ
R_G	gate resistance	$f = 1\ \text{MHz}$	-	1.62	3.24	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 20\ \text{A}$; $V_{DS} = 15\ \text{V}$; $V_{GS} = 10\ \text{V}$; see Figure 14 ; see Figure 15	-	19	-	nC
		$I_D = 20\ \text{A}$; $V_{DS} = 15\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 14 ; see Figure 15	-	9	-	nC
		$I_D = 0\ \text{A}$; $V_{DS} = 0\ \text{V}$; $V_{GS} = 10\ \text{V}$; see Figure 15	-	17	-	nC
Q_{GS}	gate-source charge	$I_D = 20\ \text{A}$; $V_{DS} = 15\ \text{V}$; $V_{GS} = 4.5\ \text{V}$; see Figure 14 ; see Figure 15	-	2.6	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.6	-	nC
Q_{GD}	gate-drain charge		-	2.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 20\ \text{A}$; $V_{DS} = 15\ \text{V}$; see Figure 14 ; see Figure 15	-	2.39	-	V
C_{iss}	input capacitance	$V_{DS} = 15\ \text{V}$; $V_{GS} = 0\ \text{V}$; $f = 1\ \text{MHz}$; $T_j = 25\ ^\circ\text{C}$; see Figure 16	-	1088	-	pF
C_{oss}	output capacitance		-	278	-	pF
C_{rss}	reverse transfer capacitance		-	78	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\ \text{V}$; $R_L = 0.6\ \Omega$; $V_{GS} = 4.5\ \text{V}$; $R_{G(ext)} = 4.7\ \Omega$	-	16	-	ns
t_r	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	29	-	ns
t_f	fall time		-	9	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$	-	7.2	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.85	1.1	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A/}\mu\text{s}$;	-	25.5	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$	-	15	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}$; $I_S = 20\text{ A}$;	-	15.9	-	ns
t_b	reverse recovery fall time	$di_S/dt = -100\text{ A/}\mu\text{s}$; $V_{DS} = 15\text{ V}$; see Figure 18	-	9.6	-	ns

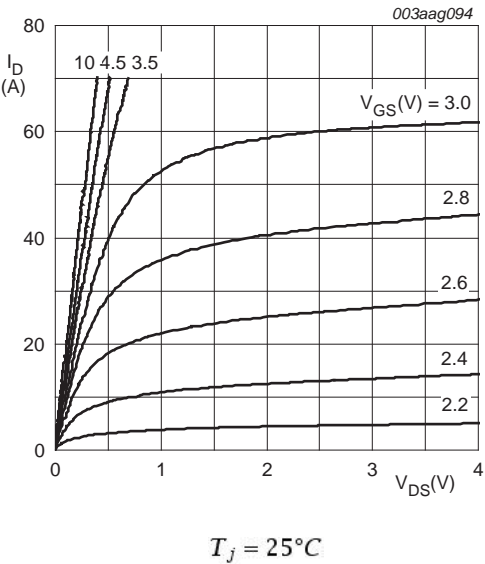


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

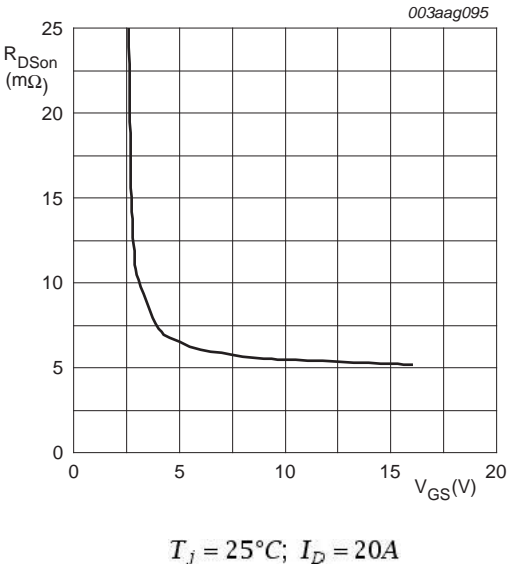
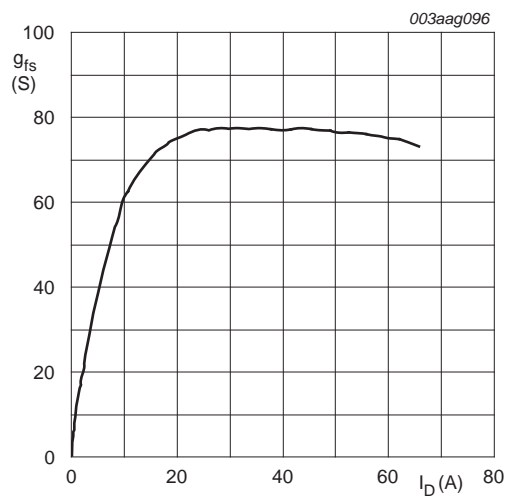
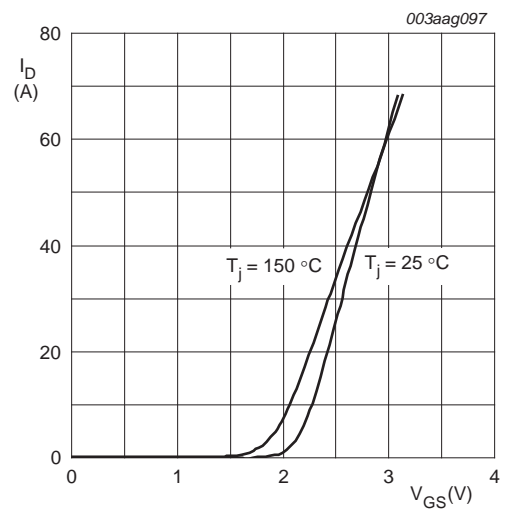


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



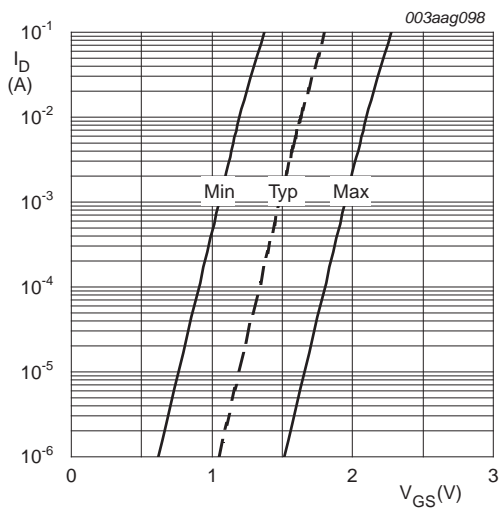
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values



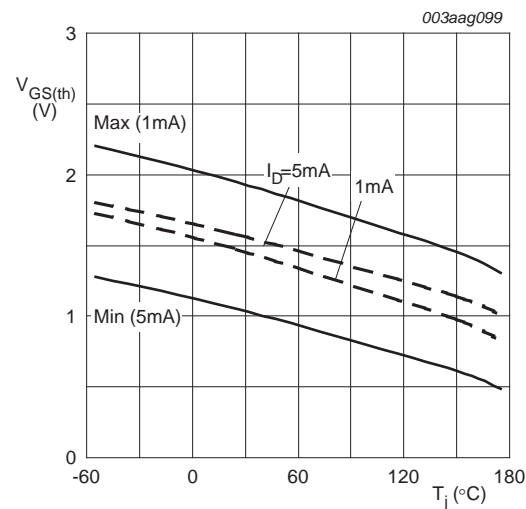
$V_{DS} = 10\text{V}$

Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature

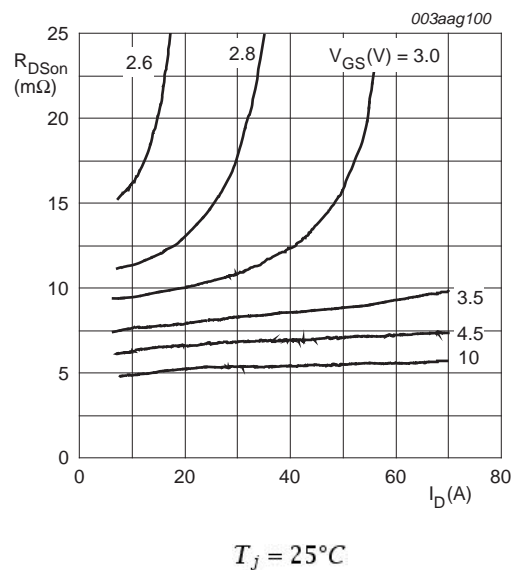


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

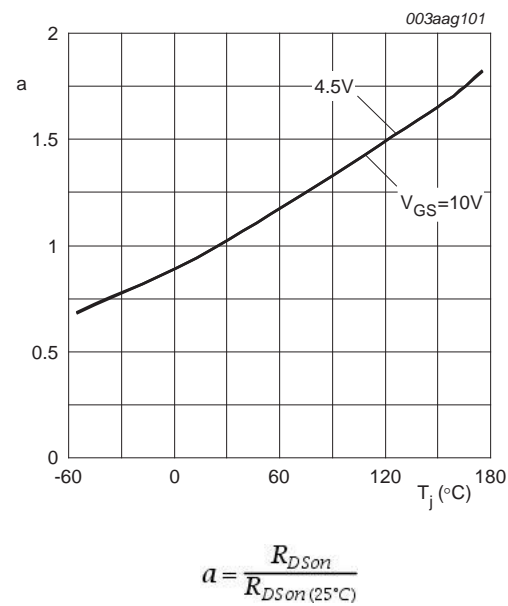


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

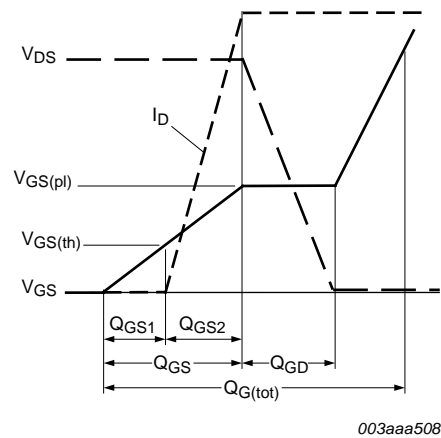


Fig 14. Gate charge waveform definitions

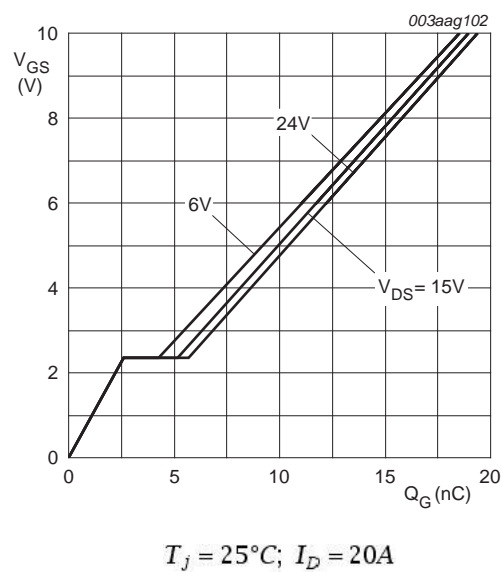


Fig 15. Gate-source voltage as a function of gate charge; typical values

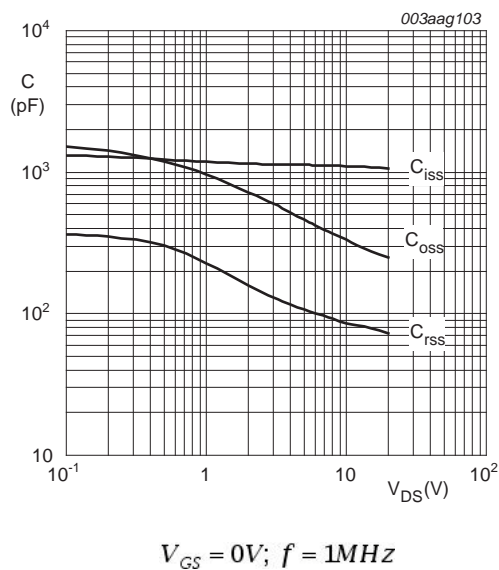


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

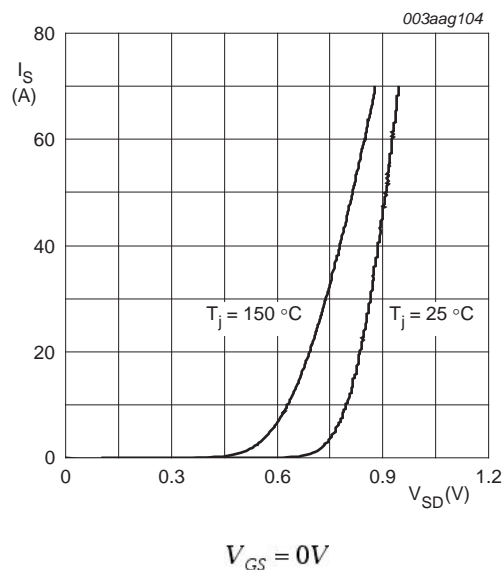


Fig 17. Source current as a function of source-drain voltage; typical values

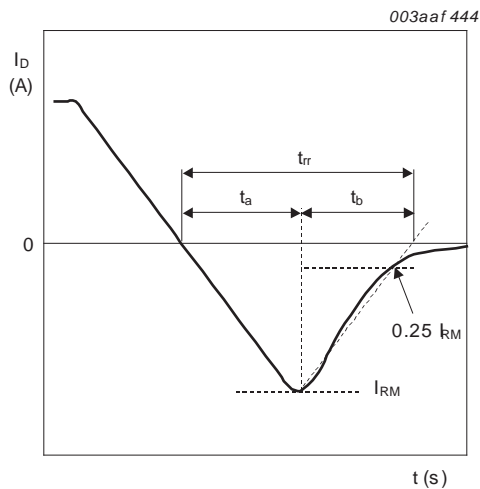


Fig 18. Reverse recovery timing definition

7. Package outline

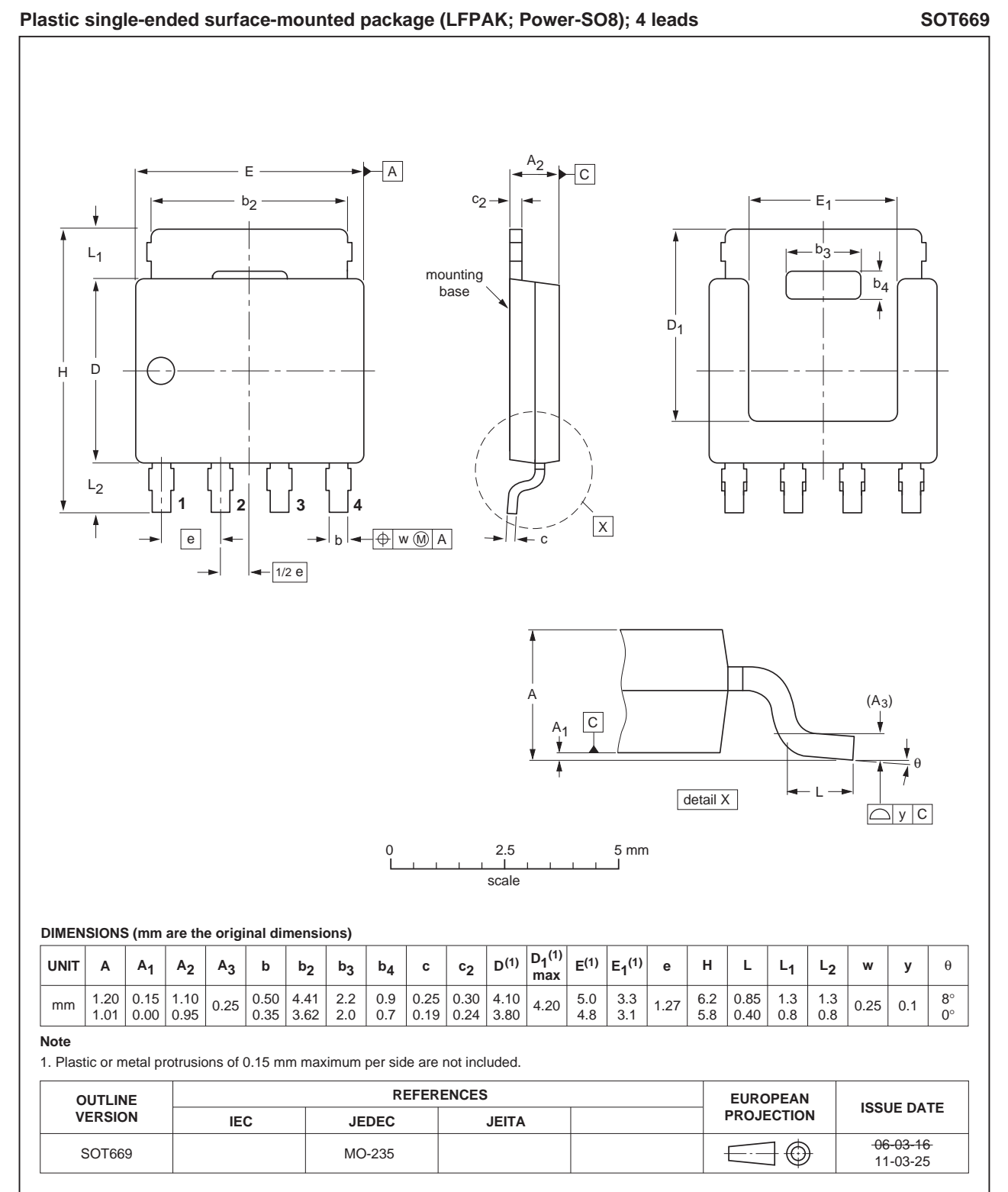


Fig 19. Package outline SOT669 (LPAK; Power-SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN6R0-30YLB v.2	20111024	Product data sheet	-	PSMN6R0-30YLB v.1
Modifications:	<ul style="list-style-type: none">• Status changed from preliminary to product.• Various changes to content.			
PSMN6R0-30YLB v.1	20110908	Preliminary data sheet	-	-

9. Legal information

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Document status ^{[1] [2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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