

PSMN8R0-30YLC

N-channel 30 V 7.9 m $\!\Omega$ logic level MOSFET in LFPAK using NextPower technology

Rev. 2 — 1 September 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching

Synchronous buck regulator

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	-	30	V
I _D	drain current	$T_{mb} = 25 ^{\circ}\text{C}; V_{GS} = 10 \text{V};$ see Figure 1	-	-	54	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	-	42	W
Tj	junction temperature		-55	-	175	°C
Static cha	racteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 12}}{\text{ or } 12}$	-	8.5	10	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_i = 25 \text{ °C}; \text{ see } \frac{12}{12}$	-	6.7	7.9	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic c	haracteristics					
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A};$ $V_{DS} = 15 \text{ V}; \text{ see } \frac{\text{Figure } 14}{\text{Figure } 15};$ see Figure 15	-	2.3	-	nC
Q _{G(tot)}	total gate charge	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A};$ $V_{DS} = 15 \text{ V}; \text{ see } \frac{\text{Figure } 14}{\text{Figure } 15};$ see $\frac{\text{Figure } 15}{\text{Figure } 15}$	-	7	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source	mb	D
3	S	source		G (EX)
4	G	gate	[9]	
mb	D	mounting base; connected to drain	1 2 3 4	mbb076 S
			SOT669 (LFPAK; Power-SO8)	

3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PSMN8R0-30YLC	LFPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669		

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Mode of }}$	-	54	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; see <u>Figure 1</u>	-	38	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; see Figure 4	-	216	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>	-	42	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	190	-	V
Source-drain	n diode				
Is	source current	T _{mb} = 25 °C	-	38	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$	-	216	Α
Avalanche re	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 54 A; $V_{sup} \le 30$ V; R_{GS} = 50 Ω; unclamped; see <u>Figure 3</u>	-	12	mJ

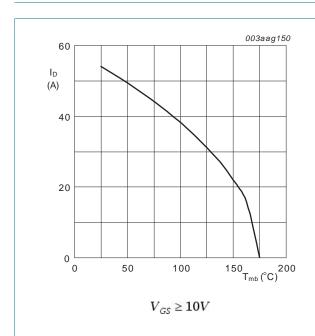
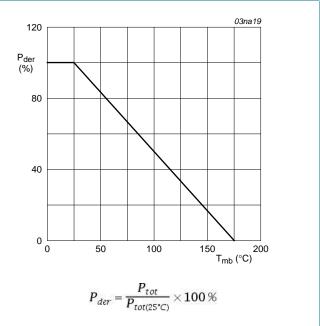


Fig 1. Continuous drain current as a function of mounting base temperature



g 2. Normalized total power dissipation as a function of mounting base temperature

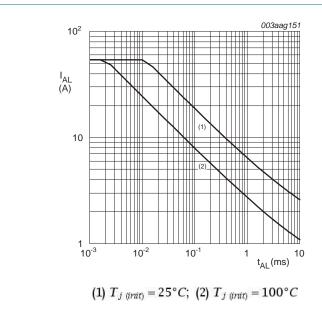
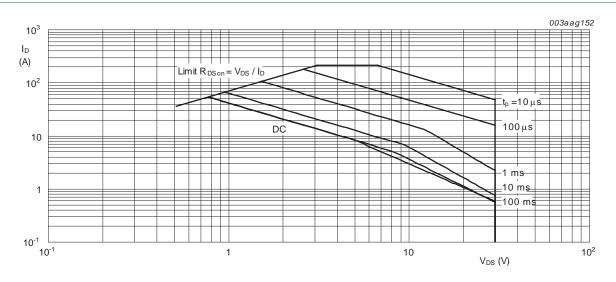


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



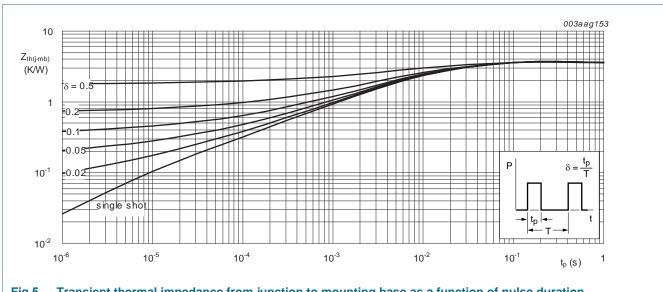
 $T_{mb} = 25$ °C; I_{DM} is a single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

Thermal characteristics

Table 5. **Thermal characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	3.38	3.61	K/W



Transient thermal impedance from junction to mounting base as a function of pulse duration

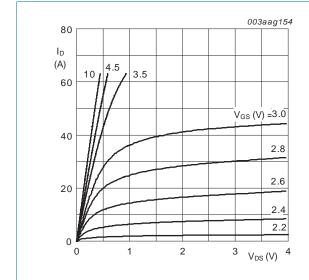
6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 25$ °C; see Figure 10	1.05	1.59	1.95	V
		I_D = 10 mA; V_{DS} = V_{GS} ; T_j = 150 °C; see <u>Figure 11</u>	0.5	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see Figure 11	-	-	2.25	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 ^{\circ}\text{C}$	-	-	100	μΑ
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 12	-	8.5	10	mΩ
	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 150 °C;$ see <u>Figure 12</u> ; see <u>Figure 13</u>	-	-	16.6	mΩ	
	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 12	-	6.7	7.9	mΩ	
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 \text{ °C};$ see Figure 12; see Figure 13	-	-	13.2	mΩ
R_G	gate resistance	f = 1 MHz	-	2.2	4.4	Ω
Dynamic	characteristics					
$Q_{G(tot)}$	total gate charge	I_D = 15 A; V_{DS} = 15 V; V_{GS} = 10 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	15	-	nC
		I_D = 15 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	7	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	13	-	nC
Q _{GS}	gate-source charge	$I_D = 15 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 4.5 \text{ V}$;	-	2.1	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	see <u>Figure 14;</u> see <u>Figure 15</u>	-	1.5	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	0.6	-	nC
Q _{GD}	gate-drain charge		-	2.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 15 A; V_{DS} = 15 V; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	2.6	-	V
C _{iss}	input capacitance	$V_{DS} = 15 \text{ V; } V_{GS} = 0 \text{ V; } f = 1 \text{ MHz;}$	-	848	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 16</u>	-	207	-	pF
C _{rss}	reverse transfer capacitance		-	70	-	pF

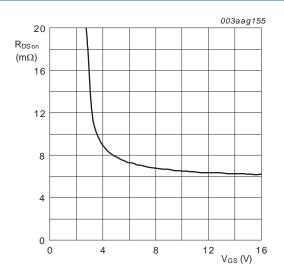
 Table 6.
 Characteristics ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{d(on)}	turn-on delay time	V_{DS} = 15 V; R_L = 1 Ω ; V_{GS} = 4.5 V;	-	15	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	11	-	ns
t _{d(off)}	turn-off delay time		-	19	-	ns
t _f	fall time		-	7	-	ns
Q _{oss}	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	5	-	nC
Source-drain	n diode					
V _{SD}	source-drain voltage	$I_S = 15 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see Figure 17	-	0.85	1.1	V
t _{rr}	reverse recovery time	$I_S = 15 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	21	-	ns
Q _r	recovered charge	V _{DS} = 15 V	-	13	-	nC
ta	reverse recovery rise time	$V_{GS} = 0 \text{ V}; I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$ $V_{DS} = 15 \text{ V}; \text{ see } \frac{\text{Figure } 18}{}$	-	12	-	ns
t _b	reverse recovery fall time		-	9	-	ns



 $T_j = 25^{\circ}C$

Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values



$$T_j = 25^{\circ}C; \ I_D = 15A$$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

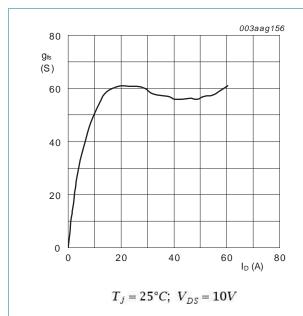


Fig 8. Forward transconductance as a function of drain current; typical values

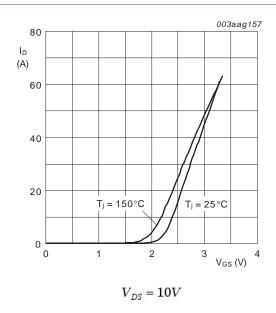


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

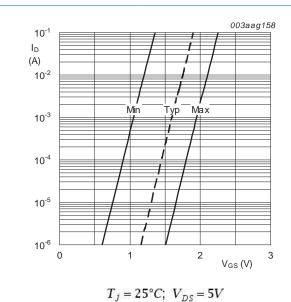


Fig 10. Sub-threshold drain current as a function of gate-source voltage

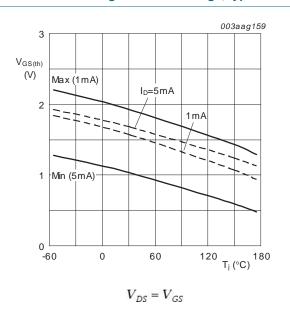


Fig 11. Gate-source threshold voltage as a function of junction temperature

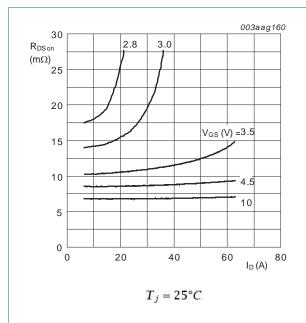


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

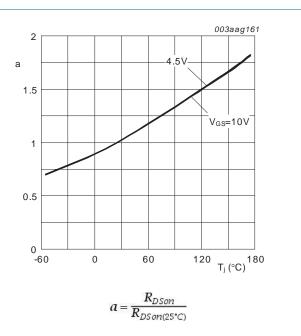


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

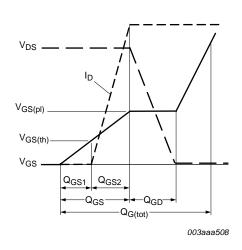


Fig 14. Gate charge waveform definitions

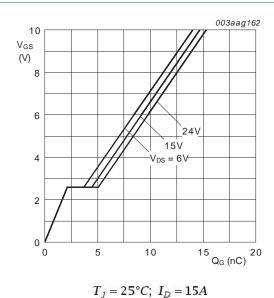


Fig 15. Gate-source voltage as a function of gate charge; typical values

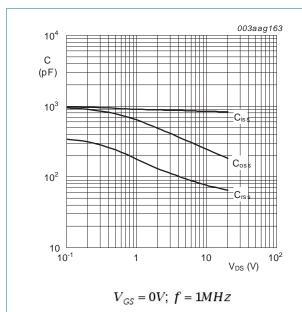


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

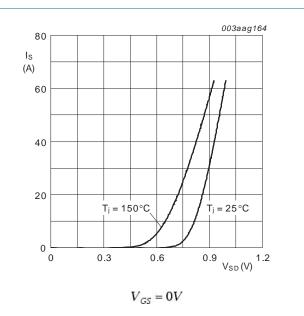


Fig 17. Source current as a function of source-drain voltage; typical values

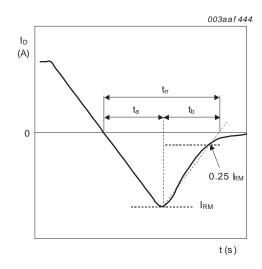
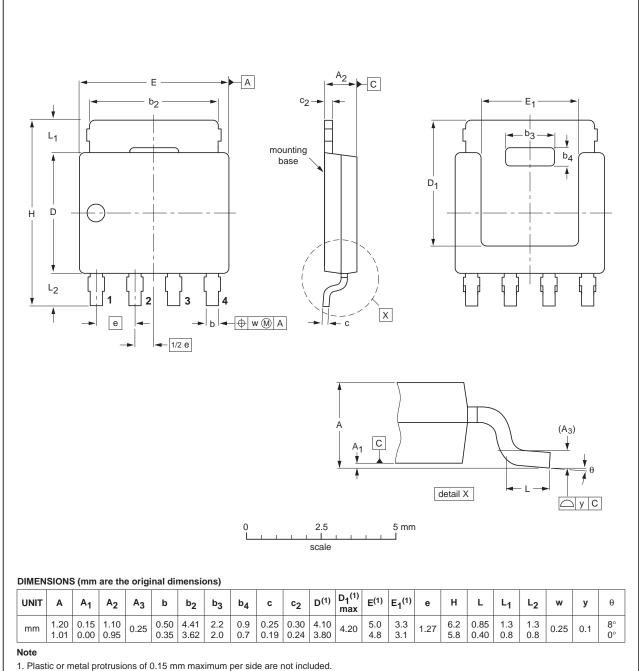


Fig 18. Reverse recovery timing definition

Package outline

Plastic single-ended surface-mounted package (LFPAK; Power-SO8); 4 leads

SOT669



OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	1330E DATE
SOT669		MO-235				06-03-16 11-03-25

Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

PSMN8R0-30YLC

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8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
PSMN8R0-30YLC v.2	20110901	Product data sheet	-	PSMN8R0-30YLC v.1		
Modifications:	Modifications: • Data sheet status changed from objective to product.					
PSMN8R0-30YLC v.1	20110712	Objective data sheet	-	-		

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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11. Contents

1	Product profile
1.1	General description
1.2	Features and benefits
1.3	Applications
1.4	Quick reference data1
2	Pinning information
3	Ordering information2
4	Limiting values3
5	Thermal characteristics5
6	Characteristics6
7	Package outline
8	Revision history12
9	Legal information13
9.1	Data sheet status
9.2	Definitions13
9.3	Disclaimers
9.4	Trademarks14
10	Contact information

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