PSMN9R0-30KL

N-channel 30 V 9 mΩ logic-level MOSFET in SO8

Rev. 01 — 14 April 2011 Objective data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode MOSFET in SO8 package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and power supply equipment

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- High performance replacement for legacy SO8 designs
- Suitable for logic level gate drive
- Suitable for wave and reflow soldering

1.3 Applications

- DC-to-DC converters
- Li-ion battery applications
- Load switching
- Portable equipment

1.4 Quick reference data

Table 1. Quick reference data

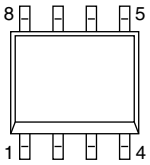
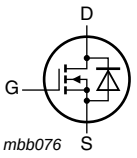
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	30	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	-	-	16	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	4	W
T_j	junction temperature		-55	-	150	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 5$ A; $T_j = 25$ °C; see Figure 12	-	11.1	13	mΩ
		$V_{GS} = 10$ V; $I_D = 5$ A; $T_j = 25$ °C; see Figure 12	-	7.7	9	mΩ

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 5 A; V_{DS} = 15 V; see Figure 14; see Figure 15	-	3.2	-	nC
$Q_{G(tot)}$	total gate charge		-	19.2	-	nC
		V_{GS} = 4.5 V; I_D = 5 A; V_{DS} = 15 V; see Figure 14; see Figure 15	-	9.3	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 16 A; $V_{sup} \leq$ 30 V; unclamped; R_{GS} = 50 Ω	-	-	77	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT96-1 (SO8)	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN9R0-30KL	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	30	V
V_{DGR}	drain-gate voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	11	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1	-	16	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C; see Figure 3	-	64	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	4	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	16	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C	-	64	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 16 A; $V_{sup} \leq 30$ V; unclamped; R_{GS} = 50 Ω	-	77	mJ

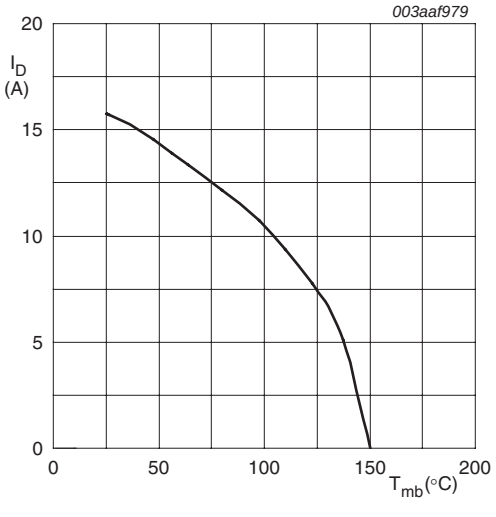


Fig 1. Continuous drain current as a function of mounting base temperature

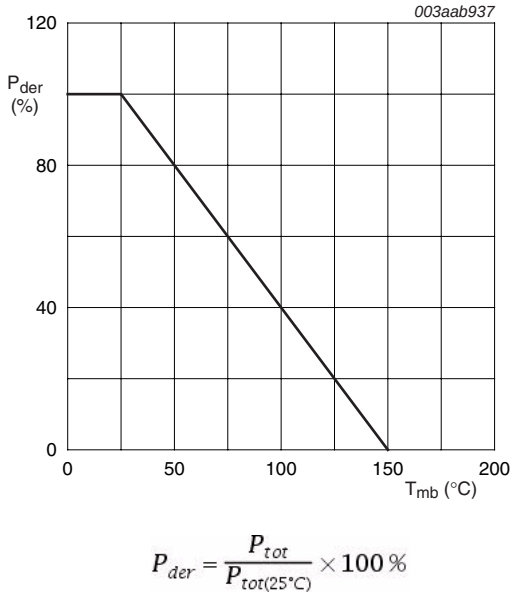
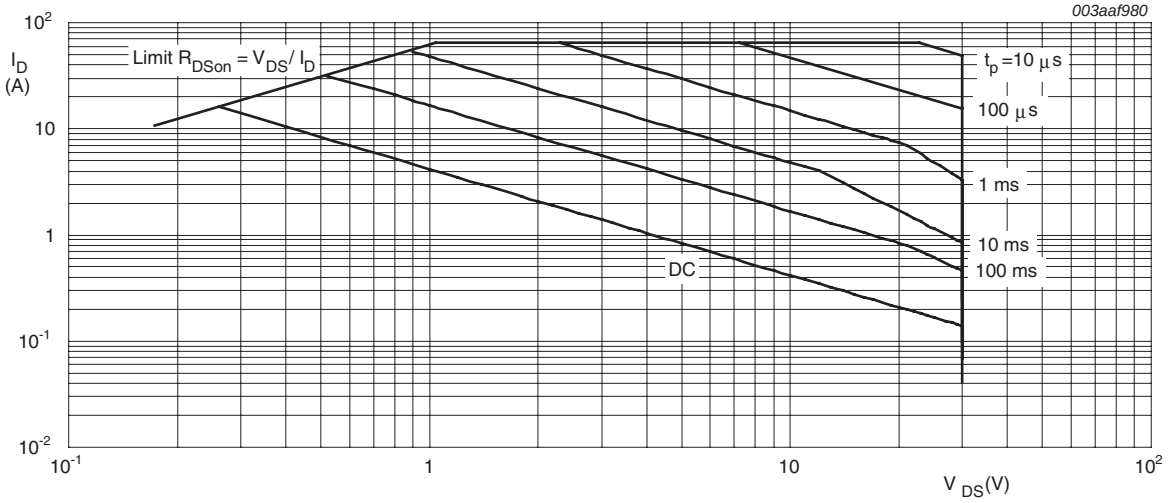


Fig 2. Normalized total power dissipation as a function of solder point temperature



T_{mb} = 25°C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	24	30	K/W

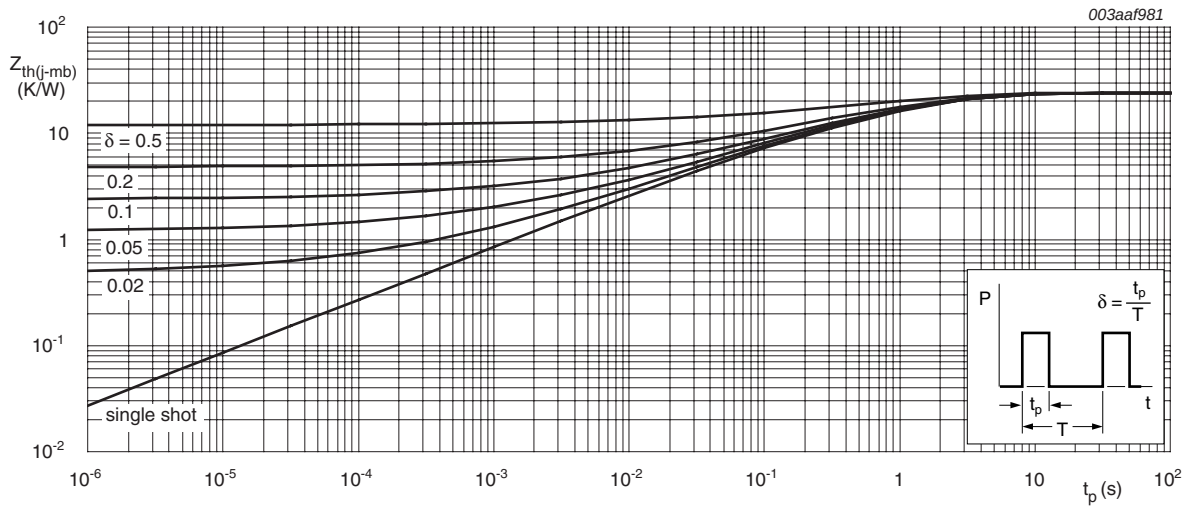


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

6. Characteristics

Table 6. Characteristics

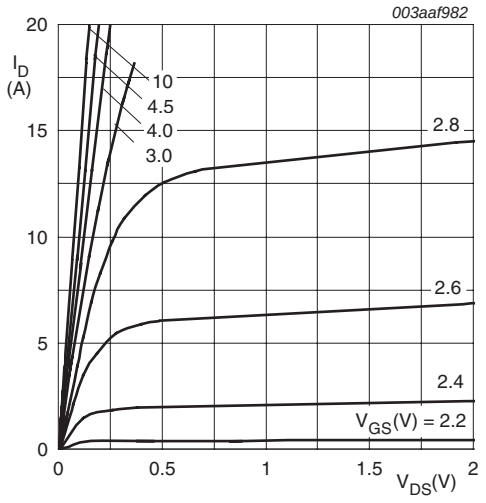
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	1.3	1.7	2.15	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11	-	-	2.55	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 11	0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	0.1	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 125 °C	-	-	50	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 5 A; T_j = 25 °C; see Figure 12	-	11.1	13	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 100 °C; see Figure 12; see Figure 13	-	-	12.4	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 150 °C; see Figure 12; see Figure 13	-	13.8	16.2	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; see Figure 12	-	7.7	9	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz	-	1.34	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 15 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	19.2	-	nC
		I_D = 5 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see Figure 14; see Figure 15	-	9.3	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V	-	16.9	-	nC
Q_{GS}	gate-source charge	I_D = 5 A; V_{DS} = 15 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	2.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.7	-	nC
Q_{GD}	gate-drain charge		-	3.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 5 A; V_{DS} = 15 V; see Figure 14; see Figure 15	-	2.5	-	V
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	1128	-	pF
C_{oss}	output capacitance		-	220	-	pF
C_{rss}	reverse transfer capacitance		-	105	-	pF

Table 6. Characteristics *...continued*

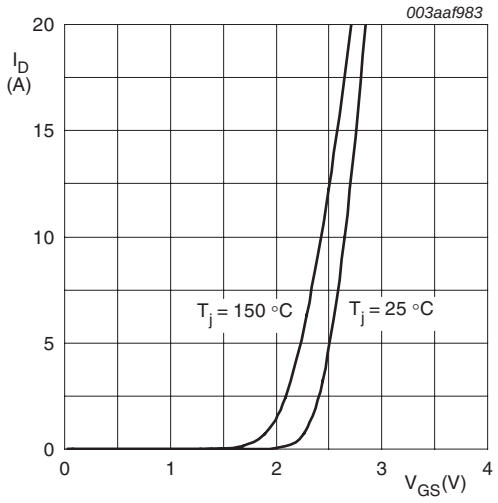
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω; T_j = 25 °C	-	15	-	ns
t_r	rise time		-	27	-	ns
$t_{d(off)}$	turn-off delay time		-	17	-	ns
t_f	fall time		-	8	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 17	-	0.79	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V	-	20	-	ns
Q_r	recovered charge		-	14	-	nC



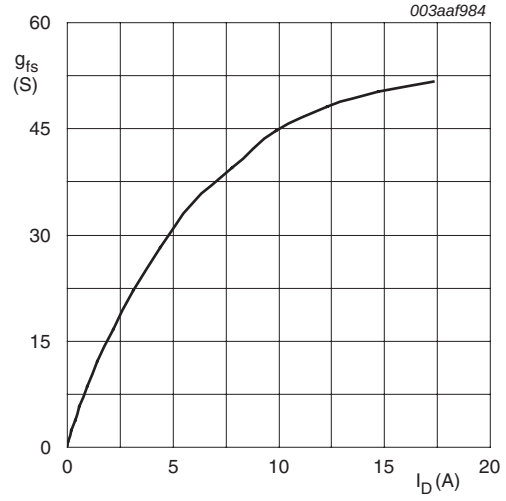
T_j = 25°C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



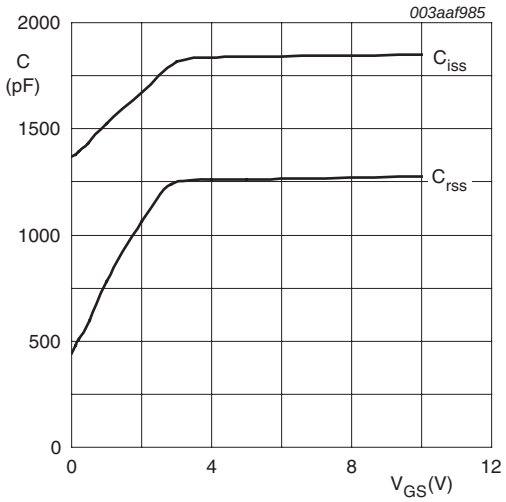
V_{DS} = 10 V

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



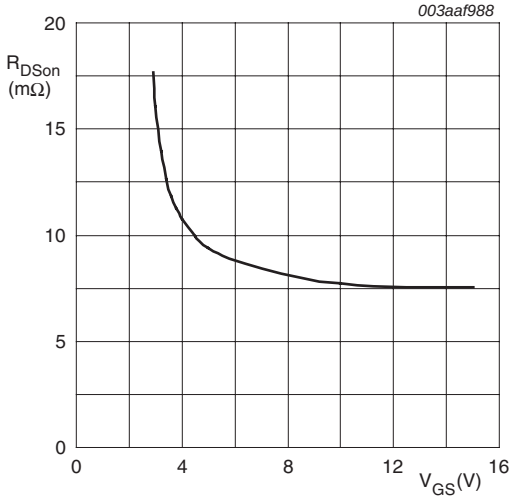
T_j = 25°C; V_{DS} = 10 V

Fig 7. Forward transconductance as a function of drain current; typical values



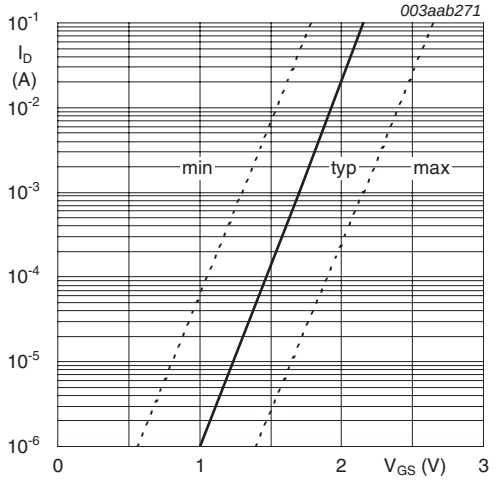
V_{DS} = 0 V; f = 1 MHz

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



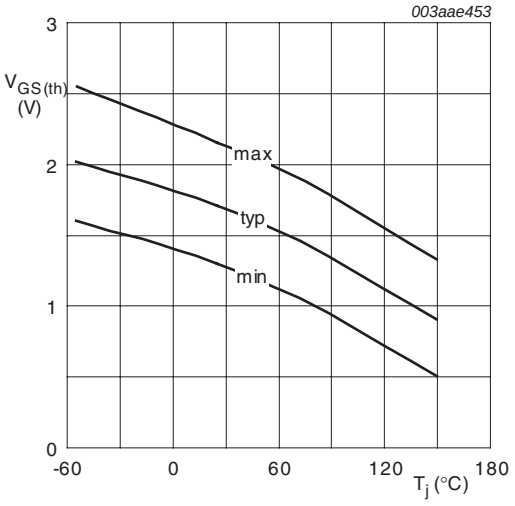
T_j = 25°C; I_D = 5 A

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



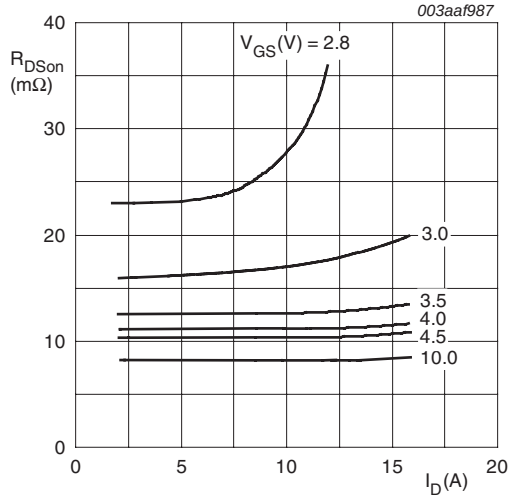
$T_j = 25\,°C; V_{DS} = 5V$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



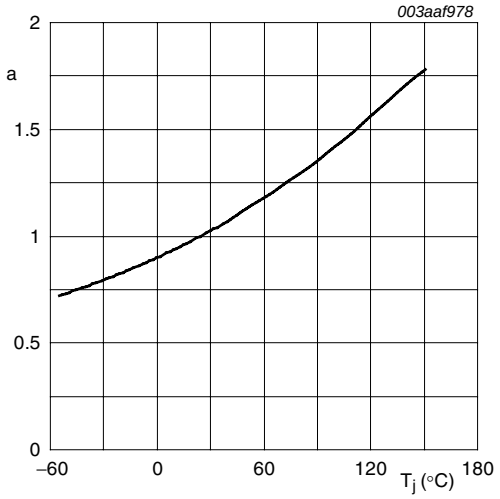
I_D = 1 mA; V_{DS} = V_{GS}

Fig 11. Gate-source threshold voltage as a function of junction temperature



T_j = 25°C

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

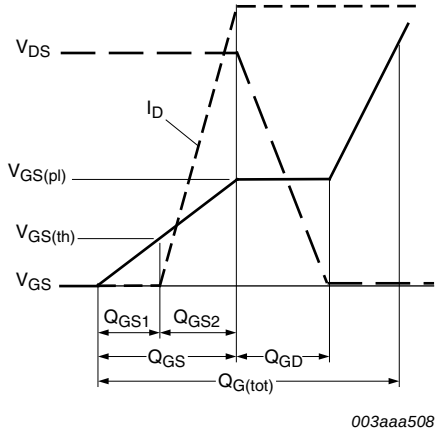
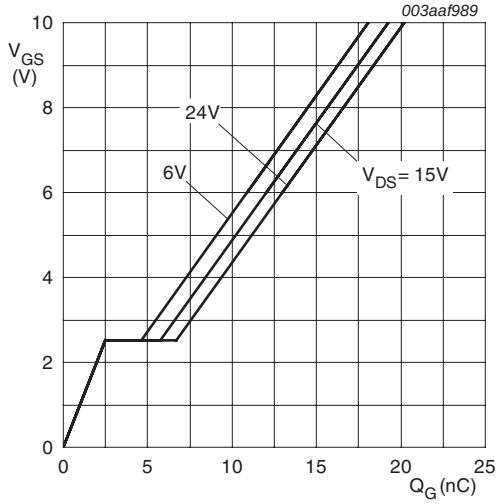
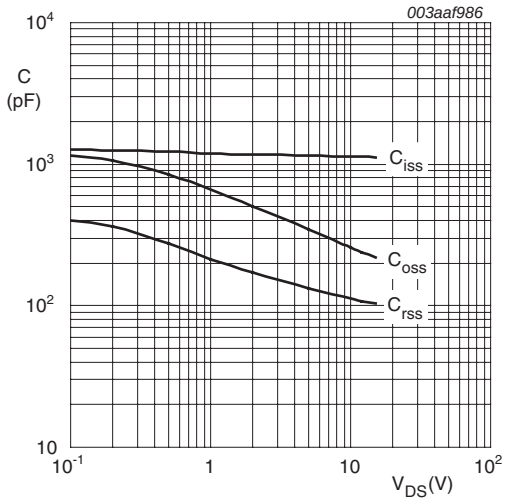


Fig 14. Gate charge waveform definitions



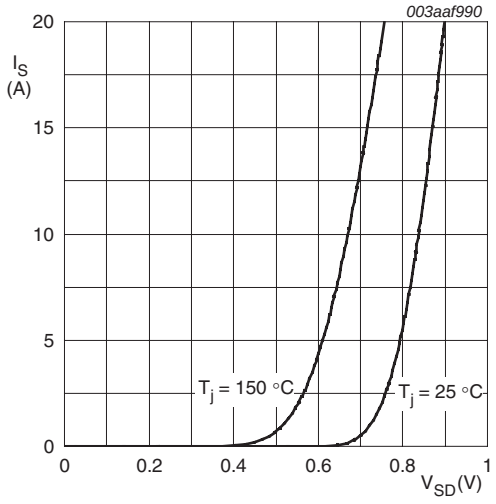
T_j = 25°C and I_D = 5 A

Fig 15. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V, f = 1 MHz

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

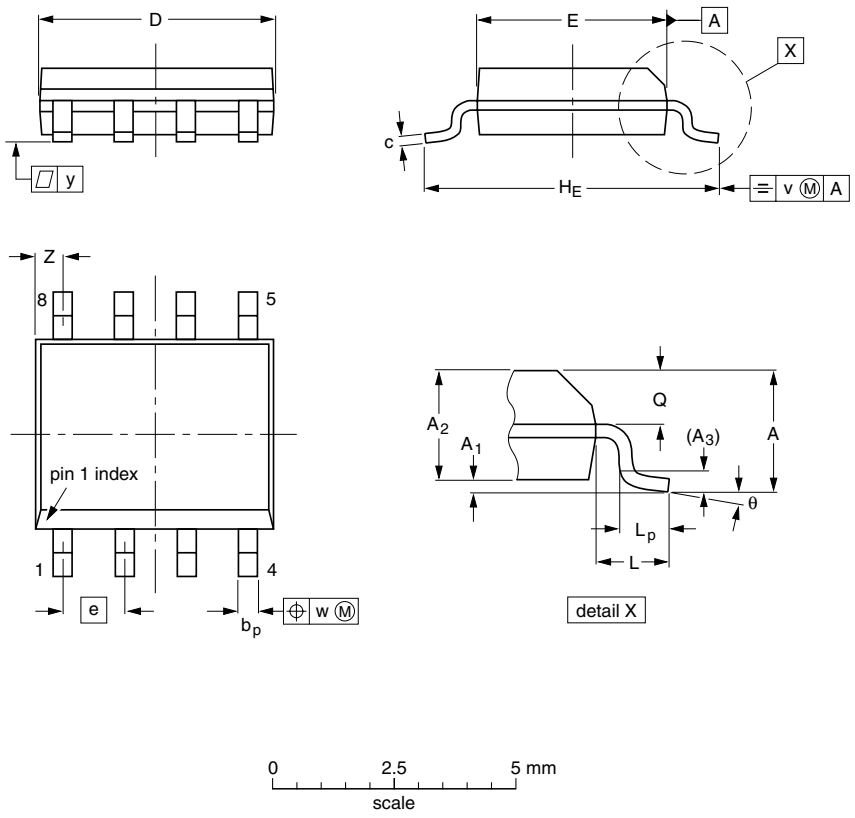


V_{GS} = 0 V

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN9R0-30KL v.1	20110414	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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10. Contact information

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