SAA7154E; SAA7154H

Multistandard video decoder with comb filter, component input and RGB output

Rev. 02 — 6 December 2007 Product data sheet

1. General description

The SAA7154E; SAA7154H is a high-quality multistandard video decoder supporting 10-bit Analog-to-Digital Converter (ADC), enhanced PAL/NTSC comb filtering, more versatile Vertical Blanking Interval (VBI) data processing, high-definition component video and picture improvement processing facilities.

It targets a variety of performance-conscious applications like e.g. Personal Video Recording (PVR), Set-Top Boxes (STB), LCD projectors, LCD TVs and DVD recordable players.

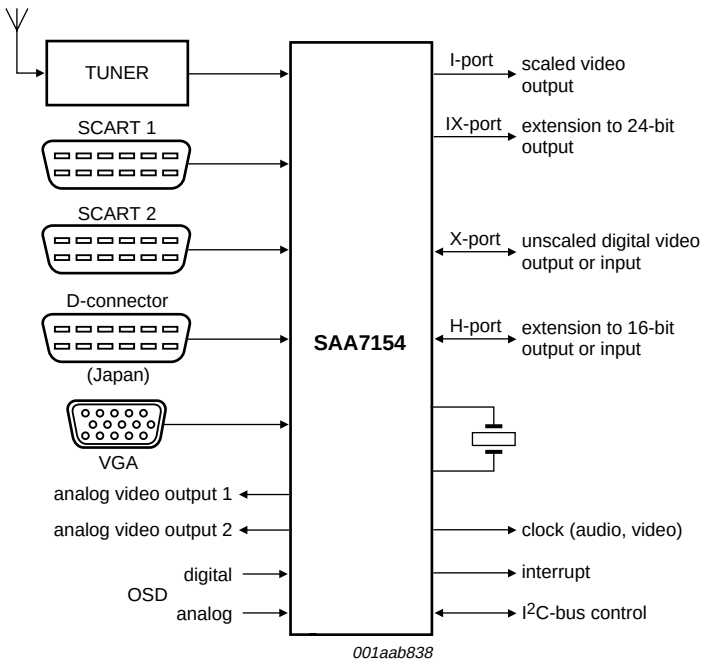


Fig 1. System block diagram

A video decoder decodes PAL/NTSC/SECAM signals into baseband component video. This video decoder includes adaptive 2-dimensional luminance and chrominance separation; in addition, e.g. baseband component type input signals can be connected directly (RGB or Y-P_B-P_R, interlaced or progressive).

The decoded video (the digitized component video, respectively) can be output on an 8-bit or 10-bit wide *ITU-656* expansion port (X-port); alternatively decoded video can be fed to a versatile video scaler to the Image port (I-port), which can be 8-bit, 16-bit or 24-bit wide. An analog On-Screen Display (OSD) interface allows to mix OSD data on the I-port and X-port video data; the digital OSD allows to add OSD data to the I-port video data.

2. Features

2.1 General

- Sixteen analog input pins, allowing for multiple combinations of composite, s-video and component video
- Eight 3-level capable sensor pins for D-connector or SCART AV- and RGB-switch signals (three of these can be active simultaneously); one **fast blanking** input
- Four studio-quality 10-bit CMOS ADCs at four-fold *ITU-656* oversampling (54 MHz)
- I^2C-bus read back of digital Automatic Gain Control (AGC) gain factor
- Two buffered analog CVBS outputs, e.g. to drive teletext decoder or VCR recorder
- Several D-terminal and SCART configurations possible
- Level sensitive **fast blanking** (RGB switch control)
- Multistandard video decoder PAL/SECAM/NTSC and their sub-standards
- Automatic detection of any supported color standard, including 480p, 576p, 720p and 1080i component video
- Optional digitizing of VGA (640×480) computer graphics with H-sync and V-sync (supports only 60 Hz vertical sync)
- Detection of copy protected input signals according to the Macrovision standard, indicating level of protection, including progressive signals 480p and 576p
- High-performance super-adaptive $^2/_4$-line comb filter for 2-dimensional chrominance/luminance separation
- HD0 component video input and output; detection of HD0/HD1 signals
- Horizontal and vertical down-scaling and up-scaling to randomly sized windows; variable from zoom to $^1/_{64}$ size (icon); the transfer data rates limit H-zoom and V-zoom:
  - Conversion to **square pixel** format
  - Vertical scaling with linear phase interpolation and accumulating filter for anti-aliasing (6-bit phase accuracy)
  - EDge-Guided vertical Interpolation (EDGI) used for zooming up to progressive line counts
- Versatile Brightness-Contrast-Saturation (BCS) adjustment
- Programmable picture improvements:
  - **Blue stretching**
  - **Green enhancement**
  - Automatic **skin tone correction**
  - Color Transient Improvement (CTI)
  - **Black and white stretching** by histogram evaluation
  - Luminance sharpness control
- RMS noise level estimation possible
- Blue screen output in case of absent input signals

- Versatile VBI data decoder, slicer, clock regeneration and byte synchronization
  - I²C-bus read back of most decoded data types (Closed Caption (CC), Gemstar1x, Gemstar2x, WSS625, WSS525 (CGMS), XDS and V-chip)
  - Optionally, raw data with dedicated gain and offset adjustment is available for software decoding
- On-chip Line-Locked Clock (LLC) generation according to *ITU-601* (standard definition) or *SMPTE-293M/ITU-R BT.1358* (HD0)
- Frame locked audio clock generation
- CMOS 3.3 V (input/output) and 1.8 V (core) device; digital inputs and I/O ports are not 5 V tolerant
- Support for programming through serial I²C-bus, full read back ability by an external controller, bit rate up to 400 kbit/s and auto increment
- Software controlled power saving standby modes
- Boundary scan test circuit complies to the *IEEE Std. 1149.b1 -1994*
- Analog OSD input
- Two package options: LBGA156 and QFP160
- Lead-free LBGA156 package available

2.2 Improvements over SAA7119

- Advanced 24-bit RGB output
- De-interlacing for progressive displays: EDGI
- Programmable cropping and scaling to TFT panel format and resolution
- Support of **panorama scaling** and keystone correction
- YUV to RGB matrix
- Digital OSD input
- Additional analog output; configurable to add of Y and C component input

3. Applications

- PC-video capture and editing
- Personal Video Recorders (PVR, time shifting)
- Cable, terrestrial and satellite Set-Top Boxes (STB)
- Internet terminals
- Flat-panel monitors
- LCD projectors
- LCD TV
- DVD recordable players
- AV-ready hard-disk drivers
- Digital televisions/scan conversion
- Video surveillance/security
- Video editing/post production
- Video phones
- Video projectors
- Digital VCRs

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAA7154E/V2/G	LBGA156	plastic low profile ball grid array package; 156 balls; body 15 × 15 × 1.05 mm	SOT700-1
SAA7154H/V2	QFP160	plastic quad flat package; 160 leads (lead length 1.6 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT322-2

5. Block diagram

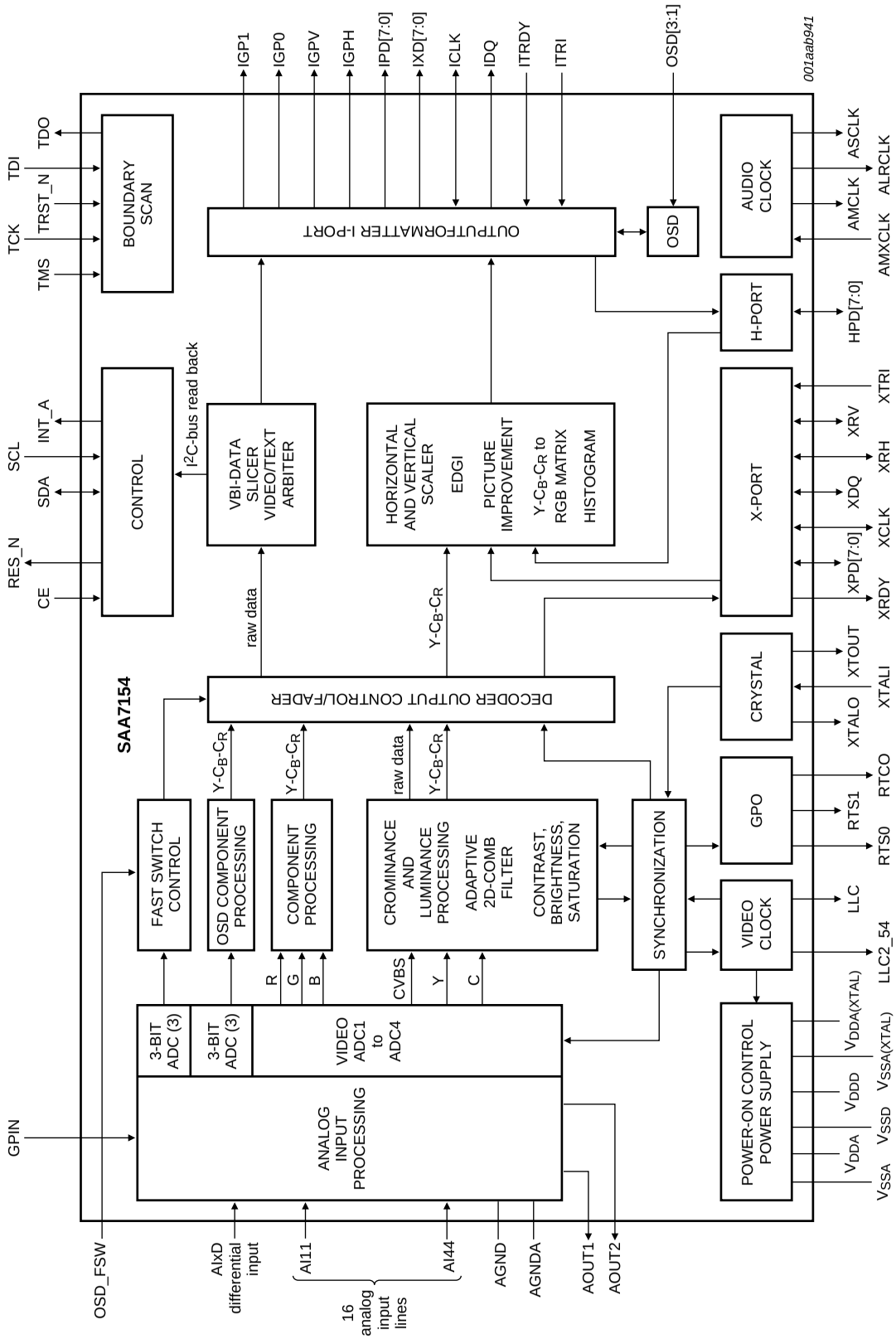


Fig 2. Block diagram

6. Pinning information

6.1 Pinning

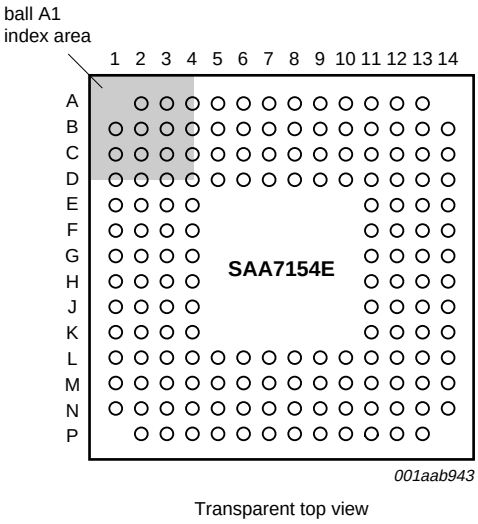


Fig 3. Pin configuration (LBGA156)

Table 2. Pin allocation table LBGA156 package[1]

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
A2	XTOUT	A3	XTALO	A4	$V_{SSA(XTAL)}$	A5	TDO
A6	XRDY	A7	XCLK	A8	XPD0	A9	XPD2
A10	XPD4	A11	XPD6	A12	OSD3	A13	IXD1
Row B							
B1	AI41	B2	i.c.	B3	$V_{DDA(XTAL)}$	B4	XTALI
B5	TDI	B6	TCK	B7	XDQ	B8	XPD1
B9	XPD3	B10	XPD5	B11	XTRI	B12	IXD0
B13	IXD2	B14	IXD3	-	-	-	-
Row C							
C1	V_{SSA4}	C2	AGND	C3	n.c.	C4	n.c.
C5	V_{DDD13}	C6	TRST_N	C7	XRH	C8	V_{DDD12}
C9	V_{DDD11}	C10	V_{DDD10}	C11	XPD7	C12	IXD5
C13	IXD4	C14	IXD6	-	-	-	-
Row D							
D1	AI43	D2	AI42	D3	AI4D	D4	V_{DDA4}
D5	V_{SSD13}	D6	TMS	D7	V_{SSD12}	D8	XRV
D9	V_{SSD11}	D10	V_{SSD10}	D11	V_{SSD9}	D12	V_{DDD9}
D13	IXD7	D14	HPD0	-	-	-	-

Table 2. Pin allocation table LBGA156 package[1] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row E							
E1	AI44	E2	V_{DDA4A}	E3	AI31	E4	V_{SSA3}
E11	HPD1	E12	HPD3	E13	HPD2	E14	HPD4
Row F							
F1	AI3D	F2	AI32	F3	AI33	F4	V_{DDA3}
F11	V_{SSD8}	F12	V_{DDD8}	F13	HPD5	F14	HPD6
Row G							
G1	AI34	G2	V_{DDA3A}	G3	AI22	G4	AI21
G11	V_{SSD7}	G12	IPD1	G13	HPD7	G14	IPD0
Row H							
H1	AI2D	H2	AI23	H3	V_{SSA2}	H4	V_{DDA2}
H11	IPD2	H12	V_{DDD7}	H13	IPD4	H14	IPD3
Row J							
J1	V_{DDA2A}	J2	AI11	J3	AI24	J4	V_{SSA1}
J11	V_{SSD6}	J12	V_{DDD6}	J13	IPD6	J14	IPD5
Row K							
K1	AI12	K2	AI13	K3	AI1D	K4	V_{DDA1}
K11	IPD7	K12	IGPH	K13	IGP1	K14	IGPV
Row L							
L1	V_{DDA1A}	L2	AGNDA	L3	AI14	L4	V_{SSD1}
L5	V_{SSD2}	L6	i.c.	L7	i.c.	L8	V_{SSD3}
L9	V_{SSD4}	L10	RTCO	L11	V_{SSD5}	L12	ITRI
L13	IDQ	L14	IGP0	-	-	-	-
Row M							
M1	AOUT1	M2	V_{SSA0}	M3	V_{DDA0}	M4	V_{DDD1}
M5	V_{DDD2}	M6	i.c.	M7	i.c.	M8	V_{DDD3}
M9	V_{DDD4}	M10	RTS0	M11	V_{DDD5}	M12	AMXCLK
M13	OSD_FSW	M14	ICLK	-	-	-	-
Row N							
N1	AOUT2	N2	V_{DDA_C18}	N3	i.c.	N4	CE
N5	LLC2_54	N6	i.c.	N7	i.c.	N8	i.c.
N9	SCL	N10	RTS1	N11	ASCLK	N12	ITRDY
N13	OSD1	N14	n.c.	-	-	-	-
Row P							
P2	V_{DDA_A18}	P3	GPIN	P4	LLC	P5	RES_N
P6	i.c.	P7	i.c.	P8	i.c.	P9	INT_A
P10	SDA	P11	AMCLK	P12	ALRCLK	P13	OSD2

[1] i.c.: internally connected; leave open. n.c.: not connected.

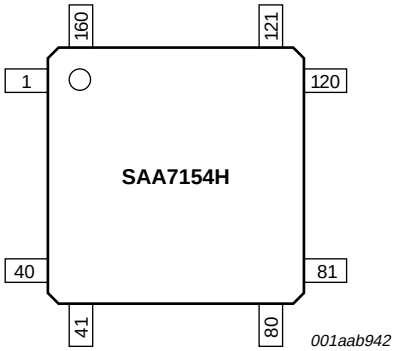


Fig 4. Pin configuration (QFP160)

Table 3. Pin allocation table QFP160 package[1]

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	i.c.	41	V_{DDA_A18}	81	n.c.	121	n.c.
2	AI41	42	i.c.	82	n.c.	122	n.c.
3	AGND	43	GPIN	83	OSD_FSW	123	IXD1
4	V_{SSA4}	44	CE	84	ICLK	124	IXD0
5	AI42	45	V_{DDD1}	85	IDQ	125	OSD3
6	AI4D	46	LLC	86	ITRI	126	XTRI
7	AI43	47	V_{SSD1}	87	IGP0	127	XPD7
8	V_{DDA4}	48	LLC2_54	88	V_{SSD5}	128	XPD6
9	V_{DDA4A}	49	RES_N	89	IGP1	129	V_{SSD9}
10	AI44	50	V_{DDD2}	90	IGPV	130	XPD5
11	AI31	51	V_{SSD2}	91	IGPH	131	XPD4
12	V_{SSA3}	52	i.c.	92	IPD7	132	V_{DDD10}
13	AI32	53	i.c.	93	IPD6	133	V_{SSD10}
14	AI3D	54	i.c.	94	IPD5	134	XPD3
15	AI33	55	i.c.	95	V_{DDD6}	135	XPD2
16	V_{DDA3}	56	i.c.	96	V_{SSD6}	136	V_{DDD11}
17	V_{DDA3A}	57	i.c.	97	IPD4	137	V_{SSD11}
18	AI34	58	i.c.	98	IPD3	138	XPD1
19	AI21	59	V_{DDD3}	99	IPD2	139	XPD0
20	V_{SSA2}	60	i.c.	100	IPD1	140	XRV
21	AI22	61	i.c.	101	V_{DDD7}	141	XRH
22	AI2D	62	i.c.	102	IPD0	142	V_{DDD12}
23	AI23	63	V_{SSD3}	103	HPD7	143	XCLK
24	V_{DDA2}	64	INT_A	104	V_{SSD7}	144	XDQ
25	V_{DDA2A}	65	V_{DDD4}	105	HPD6	145	V_{SSD12}
26	AI24	66	SCL	106	V_{DDD8}	146	XRDY
27	AI11	67	V_{SSD4}	107	HPD5	147	TRST_N
28	V_{SSA1}	68	SDA	108	V_{SSD8}	148	TCK

Table 3. Pin allocation table QFP160 package[1] *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
29	AI12	69	RTS0	109	HPD4	149	TMS
30	AI1D	70	RTS1	110	HPD3	150	TDO
31	AI13	71	RTCO	111	HPD2	151	V_{DDD13}
32	V_{DDA1}	72	AMCLK	112	HPD1	152	TDI
33	V_{DDA1A}	73	V_{DDD5}	113	HPD0	153	V_{SSD13}
34	AI14	74	ASCLK	114	V_{DDD9}	154	$V_{SSA(XTAL)}$
35	AGNDA	75	ALRCLK	115	IXD7	155	XTALI
36	AOUT1	76	AMXCLK	116	IXD6	156	XTALO
37	V_{DDA0}	77	ITRDY	117	IXD5	157	$V_{DDA(XTAL)}$
38	V_{SSA0}	78	OSD2	118	IXD4	158	XTOUT
39	AOUT2	79	OSD1	119	IXD3	159	n.c.
40	V_{DDA_C18}	80	n.c.	120	IXD2	160	n.c.

[1] i.c.: internally connected; leave open. n.c.: not connected.

6.2 Pin description

Pins sorted by functions.

Table 4. Pin description

Symbol	Pin		Type[1]	Description
	QFP160	LBGA156		
Supplies (analog)				
AGND	3	C2	P	analog signal ground
AGNDA	35	L2	P	analog signal ground
V_{DDA0}	37	M3	P	analog supply voltage (3.3 V)
V_{DDA1}	32	K4	P	analog supply voltage for analog inputs AI1x (3.3 V)
V_{DDA1A}	33	L1	P	analog supply voltage for analog inputs AI1x (3.3 V)
V_{DDA2}	24	H4	P	analog supply voltage for analog inputs AI2x (3.3 V)
V_{DDA2A}	25	J1	P	analog supply voltage for analog inputs AI2x (3.3 V)
V_{DDA3}	16	F4	P	analog supply voltage for analog inputs AI3x (3.3 V)
V_{DDA3A}	17	G2	P	analog supply voltage for analog inputs AI3x (3.3 V)
V_{DDA4}	8	D4	P	analog supply voltage for analog inputs AI4x (3.3 V)
V_{DDA4A}	9	E2	P	analog supply voltage for analog inputs AI4x (3.3 V)
$V_{DDA(XTAL)}$	157	B3	P	crystal analog supply voltage (1.8 V)
V_{DDA_A18}	40	N2	P	analog supply voltage (1.8 V)
V_{DDA_C18}	41	P2	P	analog supply voltage (1.8 V)
V_{SSA0}	38	M2	P	analog ground
V_{SSA1}	28	J4	P	ground for analog inputs AI1x
V_{SSA2}	20	H3	P	ground for analog inputs AI2x
V_{SSA3}	12	E4	P	ground for analog inputs AI3x
V_{SSA4}	4	C1	P	ground for analog inputs AI4x
$V_{SSA(XTAL)}$	154	A4	P	crystal analog ground

Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	QFP160	LBGA156		
Supplies (digital)				
V_{DDD1}	45	M4	P	digital supply voltage 1 (peripheral cells, 3.3 V)
V_{DDD2}	50	M5	P	digital supply voltage 2 (core, 1.8 V)
V_{DDD3}	59	M8	P	digital supply voltage 3 (peripheral cells, 3.3 V)
V_{DDD4}	65	M9	P	digital supply voltage 4 (core, 1.8 V)
V_{DDD5}	73	M11	P	digital supply voltage 5 (peripheral cells, 3.3 V)
V_{DDD6}	95	J12	P	digital supply voltage 6 (peripheral cells, 3.3 V)
V_{DDD7}	101	H12	P	digital supply voltage 7 (core, 1.8 V)
V_{DDD8}	106	F12	P	digital supply voltage 8 (core, 1.8 V)
V_{DDD9}	114	D12	P	digital supply voltage 9 (peripheral cells, 3.3 V)
V_{DDD10}	132	C10	P	digital supply voltage 10 (core, 1.8 V)
V_{DDD11}	136	C9	P	digital supply voltage 11 (peripheral cells, 3.3 V)
V_{DDD12}	142	C8	P	digital supply voltage 12 (core, 1.8 V)
V_{DDD13}	151	C5	P	digital supply voltage 13 (peripheral cells, 3.3 V)
V_{SSD1}	47	L4	P	digital ground 1 (peripheral cells)
V_{SSD2}	51	L5	P	digital ground 2 (core; connects to substrate)
V_{SSD3}	63	L8	P	digital ground 3 (peripheral cells)
V_{SSD4}	67	L9	P	digital ground 4 (core; connects to substrate)
V_{SSD5}	88	L11	P	digital ground 5 (peripheral cells)
V_{SSD6}	96	J11	P	digital ground 6 (core; connects to substrate)
V_{SSD7}	104	G11	P	digital ground 7 (peripheral cells)
V_{SSD8}	108	F11	P	digital ground 8 (core)
V_{SSD9}	129	D11	P	digital ground 9 (peripheral cells)
V_{SSD10}	133	D10	P	digital ground 10 (core)
V_{SSD11}	137	D9	P	digital ground 11 (peripheral cells)
V_{SSD12}	145	D7	P	digital ground 12 (core; connects to substrate)
V_{SSD13}	153	D5	P	digital ground 13 (peripheral cells)
Analog inputs (see Section 7.14.1)				
AI11	27	J2	AI	analog input 11
AI12	29	K1	AI	analog input 12
AI13	31	K2	AI	analog input 13
AI14	34	L3	AI	analog input 14
AI21	19	G4	AI	analog input 21
AI22	21	G3	AI	analog input 22; alternatively analog OSD
AI23	23	H2	AI	analog input 23
AI24	26	J3	AI	analog input 24
AI31	11	E3	AI	analog input 31 (either video or D1/SCART sensor)
AI32	13	F2	AI	analog input 32 (either video or D1/SCART sensor or analog OSD)
AI33	15	F3	AI	analog input 33 (either video or D1/SCART sensor)

Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	QFP160	LBGA156		
AI34	18	G1	AI	analog input 34 (either video or D1/SCART sensor)
AI41	2	B1	AI	analog input 41 (either video or D1/SCART sensor)
AI42	5	D2	AI	analog input 42 (either video or D1/SCART sensor or analog OSD)
AI43	7	D1	AI	analog input 43 (either video or D1/SCART sensor)
AI44	10	E1	AI	analog input 44 (either video, D1/SCART sensor or analog OSD)
AI1D	30	K3	AI	differential input for ADC channel 1 (pins AI14 to AI11)
AI2D	22	H1	AI	differential input for ADC channel 2 (pins AI24 to AI21)
AI3D	14	F1	AI	differential input for ADC channel 3 (pins AI31 to AI34)
AI4D	6	D3	AI	differential input for ADC channel 4 (pins AI41 to AI44)
Analog outputs (see Section 7.14.1)				
AOUT1	36	M1	AO	analog video output 1
AOUT2	39	N1	AO	analog video output 2
Audio clock (see Section 7.14.2)				
ALRCLK	75	P12	O/st/pd	audio left/right clock output[2][3]
AMCLK	72	P11	O	audio master clock output
ASCLK	74	N11	O	audio serial clock output
AMXCLK	76	M12	I	audio master external clock input
I^2C-bus				
SCL	66	N9	I/O	serial clock input (I^2C-bus) with inactive output path
SDA	68	P10	I/O/od	serial data input/output (I^2C-bus)
INT_A	64	P9	O/od	interrupt flag (LOW if any enabled status bit has changed)
General control				
GPIN	43	P3	I/pu	general purpose input (with internal pull-up)
CE	44	N4	I/pu	chip enable or reset input (with internal pull-up)
RES_N	49	P5	O	reset output (active LOW)
OSD input (see Section 7.14.5.2)				
OSD1	79	N13	I/O	digital OSD input 1 (output in test mode, only)
OSD2	78	P13	I/pd	digital OSD input 2
OSD3	125	A12	I	digital OSD input 3
OSD_FSW	83	M13	I/pd	switch control of digital OSD port or alternatively legacy FSW function of SAA7118 (with internal pull-down); see Section 7.14.5.2
Image port 1 (I-port)				
IPD7	92	K11	O	MSB of image port data 1 output
IPD6	93	J13	O	bit 6 of image port data 1 output

Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	QFP160	LBGA156		
IPD5	94	J14	O	bit 5 of image port data 1 output
IPD4	97	H13	O	bit 4 of image port data 1 output
IPD3	98	H14	O	bit 3 of image port data 1 output
IPD2	99	H11	O	bit 2 of image port data 1 output
IPD1	100	G12	O	bit 1 of image port data 1 output
IPD0	102	G14	O	LSB of image port data 1 output
ICLK	84	M14	I/O	clock output signal for image port or optional asynchronous back-end clock input
IDQ	85	L13	O	output data qualifier for image port (optional: gated clock output)
IGP1	89	K13	O	general purpose output signal 1 of image port
IGP0	87	L14	O	general purpose output signal 0 of image port
IGPH	91	K12	O	multipurpose horizontal reference output signal of image port
IGPV	90	K14	O	multipurpose vertical reference output signal of image port
ITRDY	77	N12	I/pu	target ready input for image port data
ITRI	86	L12	I	image port output control signal, affects all input port pins and pin ICLK, enable and active polarity is under software control
Image I-port 2 (IX-port)				
IXD7	115	D13	O	MSB of image port data 2
IXD6	116	C14	O	bit 6 of image port data 2
IXD5	117	C12	O	bit 5 of image port data 2
IXD4	118	C13	O	bit 4 of image port data 2
IXD3	119	B14	O	bit 3 of image port data 2
IXD2	120	B13	O	bit 2 of image port data 2
IXD1	123	A13	O	bit 1 of image port data 2
IXD0	124	B12	O	LSB of image port data 2
Expansion port (X-port; see Section 7.14.4.1 and Section 7.14.4.2)				
XPD7	127	C11	I/O	MSB of expansion port data
XPD6	128	A11	I/O	bit 6 of expansion port data
XPD5	130	B10	I/O	bit 5 of expansion port data
XPD4	131	A10	I/O	bit 4 of expansion port data
XPD3	134	B9	I/O	bit 3 of expansion port data
XPD2	135	A9	I/O	bit 2 of expansion port data
XPD1	138	B8	I/O	bit 1 of expansion port data
XPD0	139	A8	I/O	LSB of expansion port data
XCLK	143	A7	I/O	clock I/O expansion port
XDQ	144	B7	I/O	data qualifier for expansion port or source-select (pixelwise switch between X-port input/decoder output)

Table 4. Pin description *...continued*

Symbol	Pin		Type[1]	Description
	QFP160	LBGA156		
XRDY	146	A6	O	task flag or ready signal from scaler, I^2C-bus controlled
XRH	141	C7	I/O	horizontal reference I/O expansion port
XRV	140	D8	I/O	vertical reference I/O expansion port
XTRI	126	B11	I	X-port output control signal, affects all X-port pins (XPD7 to XPD0, XRH, XRV, XDQ and XCLK), enable and active polarity is under software control
Host port (H-port; see Section 7.14.4.1)				
HPD7	103	G13	I/O	MSB of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD6	105	F14	I/O	bit 6 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD5	107	F13	I/O	bit 5 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD4	109	E14	I/O	bit 4 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD3	110	E12	I/O	bit 3 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD2	111	E13	I/O	bit 2 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD1	112	E11	I/O	bit 1 of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
HPD0	113	D14	I/O	LSB of host port data I/O, extended C_B-C_R input for expansion port, extended C_B-C_R output for image port
Real-time clock (see Section 7.14.3 and Section 7.14.4.2)				
RTCO	71	L10	O/st/pd	real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence[2][4]
RTS1	70	N10	O	real-time status or sync information, controlled by subaddresses 11h and 12h
RTS0	69	M10	O	real-time status or sync information, controlled by subaddresses 11h and 12h
Clocks (see Section 7.14.3)				
LLC	46	P4	O	line-locked system clock output (27 MHz nominal)
LLC2_54	48	N5	O	line-locked $\frac{1}{2}$ clock output (13.5 MHz nominal) or ADC clock 54 MHz, selectable through I^2C-bus
XTALI	155	B4	I	input terminal for 24.576 MHz (32.11 MHz) crystal oscillator or connection of external oscillator
XTALO	156	A3	O	24.576 MHz (32.11 MHz) crystal oscillator output; do not connect if clock input XTALI is used
XTOUT	158	A2	O	crystal oscillator output signal; auxiliary signal
Boundary scan test				
TCK	148	B6	I/pu	test clock for boundary scan test[5]
TDI	152	B5	I/pu	test data input for boundary scan test[5]

Table 4. Pin description *…continued*

Symbol	Pin		Type[1]	Description
	QFP160	LBGA156		
TDO	150	A5	O	test data output for boundary scan test[5]
TMS	149	D6	I/pu	test mode select input for boundary scan test or scan test[5]
TRST_N	147	C6	I/pu	test reset input (active LOW), for boundary scan test (with internal pull-up)[5][6][7]
Pins not in use				
i.c.	1	B2	-	internally connected; leave open
i.c.	42	N3	-	internally connected; leave open
i.c.	52	N6	-	internally connected; leave open
i.c.	53	P6	-	internally connected; leave open
i.c.	54	M6	-	internally connected; leave open
i.c.	55	L6	-	internally connected; leave open
i.c.	56	N7	-	internally connected; leave open
i.c.	57	P7	-	internally connected; leave open
i.c.	58	L7	-	internally connected; leave open
i.c.	60	M7	-	internally connected; leave open
i.c.	61	P8	-	internally connected; leave open
i.c.	62	N8	-	internally connected; leave open
n.c.	80	N14	-	not connected
n.c.	81	-	-	not connected
n.c.	82	-	-	not connected
n.c.	121	-	-	not connected
n.c.	122	-	-	not connected
n.c.	159	C3	-	not connected
n.c.	160	C4	-	not connected

[1] A = analog, I = input, O = output, P = power, st = strapping, pu = pull-up, pd = pull-down, od = open-drain.

[2] Pin strapping is done by connecting the pin to the supply through a 4.7 kΩ resistor. During the power-up reset sequence the corresponding pins are switched to input mode to read the strapping level. For the default setting, no strapping resistor is necessary (internal pull-down).

[3] Pin ALRCLK operates as crystal selector during power-up; ALRCLK strapped to logic 0 for a 24.576 MHz crystal (default); ALRCLK strapped to logic 1 for a 32.110 MHz crystal.

[4] Pin RTCO operates as I^2C-bus slave address selector during power-up; RTCO strapped to logic 0 for slave addresses 42h/43h and 4Ah/4Bh (default); RTCO strapped to logic 1 for slave address 40h/41h and 48h/49h.

[5] In accordance with the *IEEE1149.1* standard the pads TDI, TMS, TCK and TRST_N are input pads with an internal pull-up transistor and TDO is a 3-state output pad.

[6] For board design without boundary scan implementation connect the TRST_N pin to ground.

[7] This pin provides easy initialization of the Boundary Scan Test (BST) circuit. TRST_N can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

7. Functional description

7.1 Analog front-end

7.1.1 Features

The SAA7154E; SAA7154H offers sixteen analog signal inputs which supply the signals to four analog main channels with source switches, clamp circuits, analog amplifiers and 10-bit CMOS ADCs with decimation filters. The SAA7154E; SAA7154H has some auxiliary inputs which can be utilized to detect 3-level configuration signals common on SCART- or D-connector (see Section 7.1.1.1 and Section 11.3).

Features:

- Automatic Gain Control (AGC) for the selected CVBS or Y/C channel or manually adjustable gain for all signal types
- Automatic clamp control for CVBS, Y/C and component video
- I^2C-bus read back of digital AGC gain factor
- Supporting fast channel switching
- Automatic detection of activity on **fast blanking** (RGB-switch control); see Section 7.4
- Seamless **fast blanking** between CVBS input and synchronous RGB-SCART input
- Support for D-terminal or up to two SCART connectors
- Buffered analog video output, e.g. to connect CVBS to a peripheral teletext decoder
- RMS noise level estimation.

Another set of four 3-bit ADCs have the function to convert analog RGB signals carrying menu or teletext overlay signals, e.g. from a teletext decoder like SAA5264/65.

Figure 5 shows the principle usage of the analog video inputs in an application with SCART and its connections to digital blocks: AV-detect, Fast SWitch (FSW), video decoder and component processing.

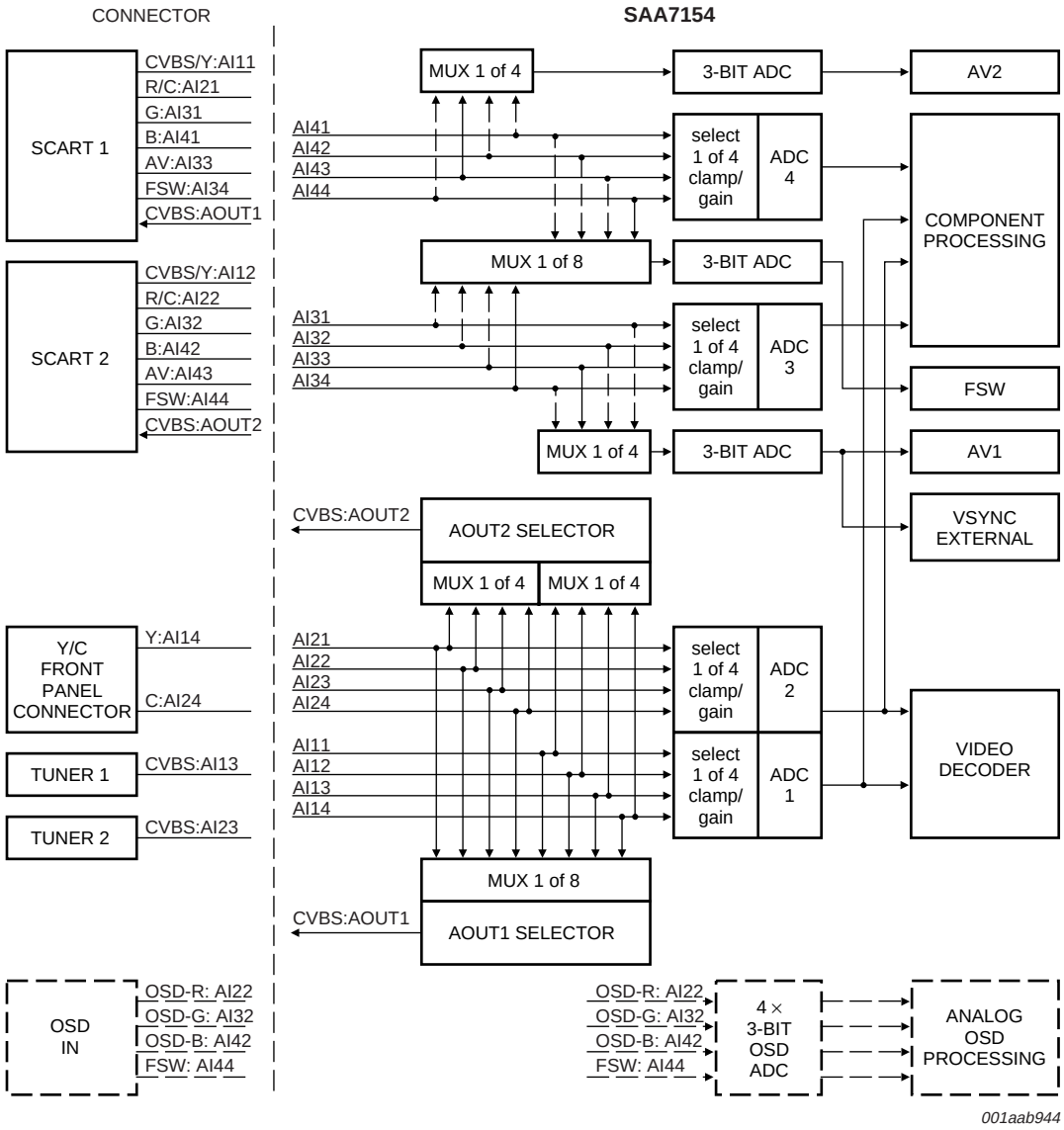


Fig 5. Analog front-end

7.1.1.1 D-terminal and SCART configuration

Configuration signals of SCART-connector and D-connector: Three pins are sensitive to a 3-level signal (see Section 11.3). So, if used in context with a D-connector three different levels can be distinguished. (As an option pin GPIN of SAA7118 can act as **plug insert detect** when tied to ground).

If used in context with a SCART-connector, two of these pins will be needed to distinguish the three different levels for **AV control** and to act as a 3-bit ADC for **RGB switch control**, also known as **fast switching**.

Fast blanking (RGB switch control): The RGB switch control selects on a pixel-by-pixel basis either a CVBS or a RGB signal (which is usually menu information or teletext synchronized with CVBS). Since the switch control signal is generally at a different clock rate than the system clock (although both are line-locked), the sampling instance for this signal sometimes might show some uncertainties if a standard bi-level input is used.

The SAA7154E; SAA7154H digitizes the switching signal with 3-bit at a 54 MHz system clock, thus reproducing its transient exactly; the digitized information is used to control a digital fader, resulting in a correctly weighted CVBS and RGB portion at every switching point.

Activity on the **fast blanking** signal is monitored continuously and reflected in a dedicated I^2C-bus status bit; the SAA7154E; SAA7154H recognizes even short switch pulses that can occur during text overlay,

7.1.1.2 Buffered analog output

The existing SAA7118 provides one out of four selected input signals (used for further digital processing) at a buffered output, but the SAA7154E; SAA7154H is also able to point to any two out of eight analog inputs (which the digital processing unit accepts, if necessary). Additionally, the second buffered output signal might be the summation of an input Y and C signal, thus easily converting these signals to CVBS.

For example this buffered output signal can be fed to a teletext decoder such as the SAA5264/65 or it can serve as a CVBS monitoring signal to a video recorder.

7.1.2 Analog input control

The Analog Input Control (AIC) has the following key features:

- Fully autonomous video gain and clamp control, based on analog (coarse) gain pre-scaling and digital (fine) gain control in CVBS mode
- Adaptive (**master-slave**) mode: manual gain control for Y/C input signals
- Component input signals (sync RGB, Y-C_B-C_R) based on manual gain control
- Access to various special controls like status signals for debugging (**expert mode**)
- SAA7118 backward-compatible input mode table with user presets
- Clamp: gain correction of input signals containing Macrovision copy protection
- Gain correction for compressed-sync (**white peak**) events
- Integrated decimation filters for 4 : 1 (SDTV) and 2 : 1 (HDTV) oversampling modes.

7.1.2.1 Block description

The SAA7154E; SAA7154H provides sixteen analog signal inputs, four analog main channels with source switch, clamp circuit, analog amplifier and video 10-bit CMOS ADC.

The gain control circuit receives the static gain levels for the four analog amplifiers (through the I^2C-bus) or controls one of these amplifiers automatically through a built-in Automatic Gain Control (AGC) as part of the Analog Input Control (AIC). This AGC for luminance is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. It is not possible to apply AGC to component input signals, therefore the gain of these signals has to be set manually using the corresponding control registers.

Decimation filtering is required to remove aliasing artifacts that can result from 4-fold oversampling of SDTV signals (54 MHz sampling frequency and 13.5 MHz pixel rate) and 2-fold oversampling of HDTV signals.

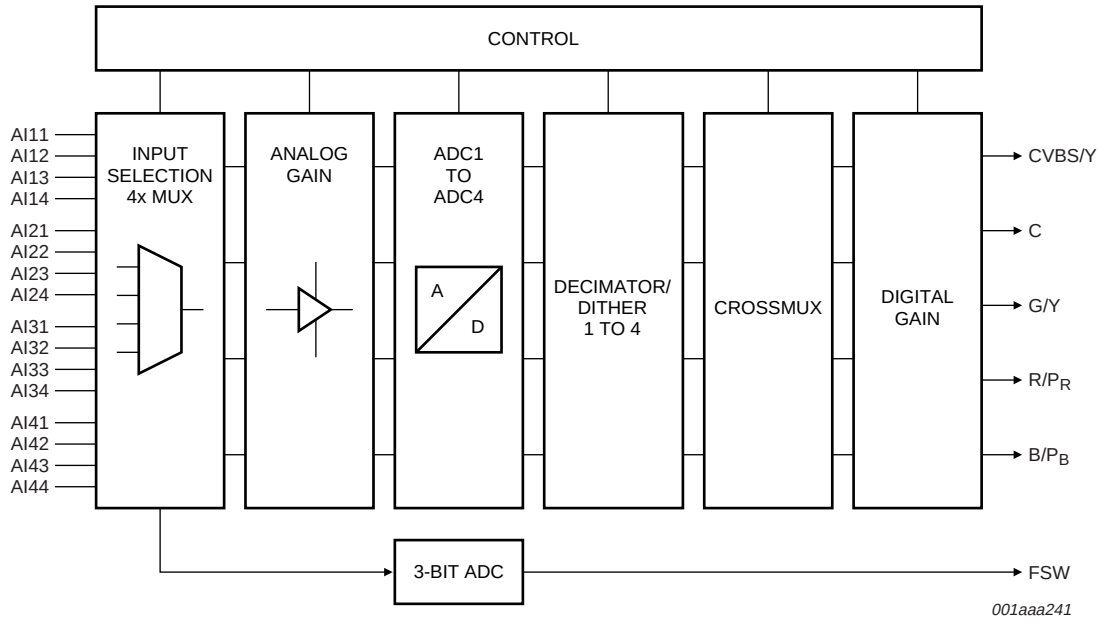


Fig 6. Analog video inputs and analog input control

7.1.2.2 Basic functional modes

These are the basic operation modes implemented in the AIC:

- CVBS modes: working as fully autonomous AGC (default); can be changed to manual gain control by setting bits GAFIXA = 1b and GAFIXD = 1b
- S-video adaptive modes: Y channel acts as autonomous AGC and C channel follows with its digital gain value; can be changed to manual gain control by setting bit GAFIXD = 1b
- S-video fixed-gain modes: Y channel running in AGC mode and C channel forced to manual gain control; bits GAFIXA and GAFIXD have influence on Y channel only
- Component signal (sync RGB, Y-C_B-C_R) modes: sync running in AGC mode, forced manual gain control for the component channels; bits GAFIXA and GAFIXD have influence on sync channel only.

7.1.2.3 I^2C-bus read back of digital AGC gain factor

For certain applications with known and stable signal amplitude, AGC can be set to manual. A single I^2C-bus read back on a channel in use will provide the necessary digital gain factor for this channel, which can be stored by the system controller. Afterwards, immediate gain setting is achieved by just restoring the measured value whenever the related channel is active.

7.2 Video decoder

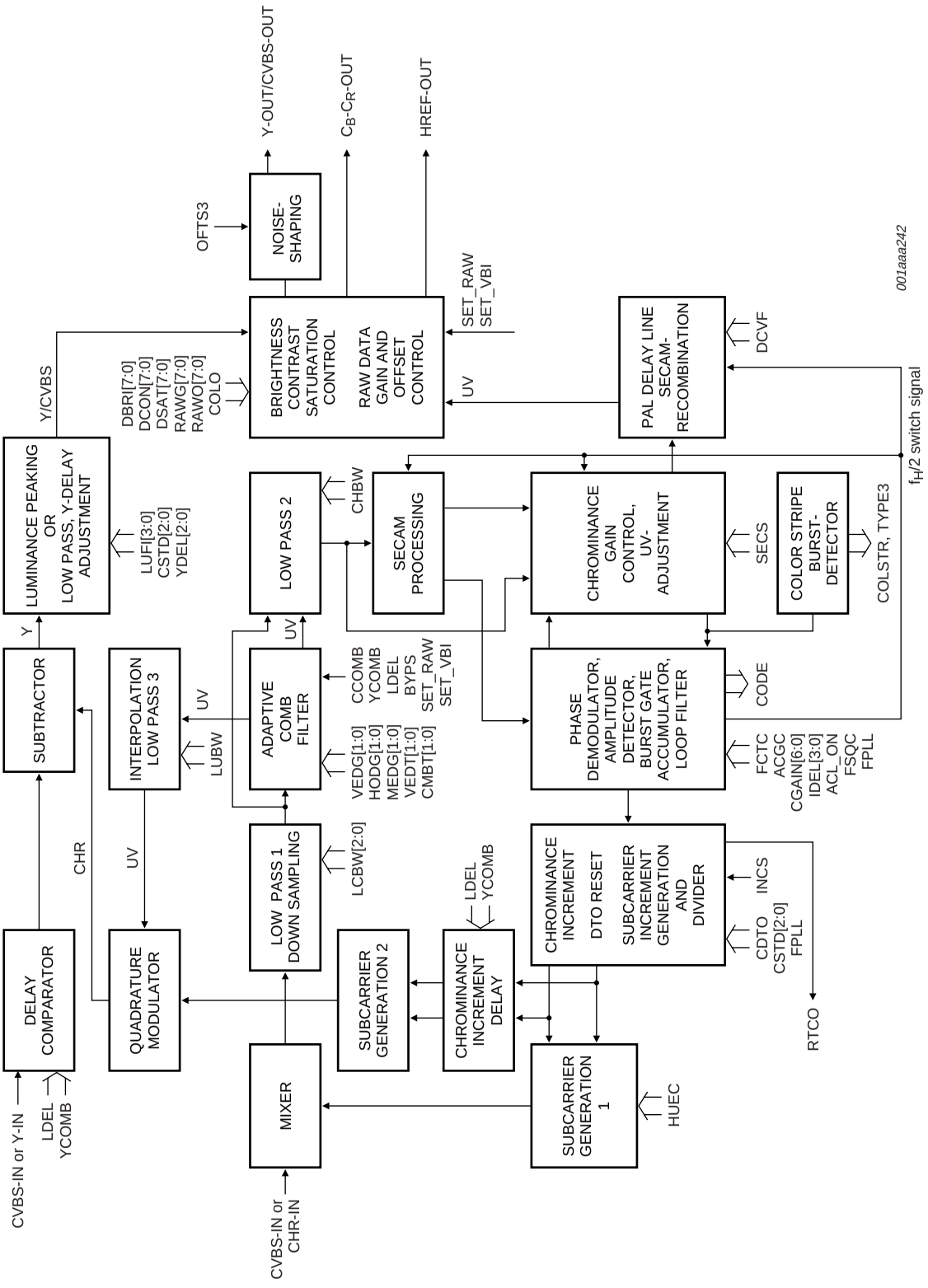


Fig 7. Chrominance and luminance processing, adaptive comb filter

7.2.1 Comb filter operation

Super-adaptive $^{2}/_{4}$-line comb filter for two dimensional chrominance and luminance separation for:

- Increased luminance and chrominance bandwidth for all PAL and NTSC standards
- Reduced cross-color and cross-luminance artifacts, even with critical color patterns.

The decision logic of the 2-dimensional comb filter in the SAA7154E; SAA7154H is improved in order to reduce residual artifacts (namely cross-color and cross-luminance (dots)). The bandwidth of the combed luminance and chrominance signals are kept (compared to the SAA7118), such that the overall performance is significantly enhanced.

7.2.2 Automatic color standard detection

The result of the automatic color standard detection can be read through I^2C-bus read access; the level of detail of the respective status bits includes subcarrier frequency, line frequency and field frequency.

Thus all PAL, NTSC and SECAM standards including sub-standards can be distinguished:

- PAL BGDHIN
- Combination-PAL N
- PAL M
- NTSC M/NTSC-Japan
- NTSC 4.43
- SECAM.

Remark: For NTSC-Japan there is no detection of black level offset through color standard detection.

7.2.3 Easy CVBS versus Y/C discrimination

The SAA7154E; SAA7154H checks respective channels (under control of firmware) for the actual burst amplitude and writes the result to dedicated I^2C-bus status bits. Comparing the actual amplitudes enables the system firmware to determine either a CVBS or s-video input.

7.2.4 Stability of vertical synchronization

Stability of vertical synchronization has been improved considerably:

- Automatic detection of signals from consumer grade VTRs
- Improved lock stability for non-standard sources, e.g. more reliable odd/even detection.

Deteriorated signals from VCR tapes might upset the vertical synchronization, resulting in vertical jumping of the displayed picture during pause or even during playback mode.

When switching from playback mode to fast forward, the output picture is sensitive to scrolling which requires a certain time until it is stable again.

To avoid these undesired effects, the recognition of the vertical synchronization pulse has been improved. A reference for the improved synchronization behavior is the selected tape material.

The odd/even field detection has been made more robust. The detection signal is low-pass filtered by a field-count programmable flywheel to exclude all noise peaks of weak VCR signals.

RMS noise on sync pulse tips is measured and a status bit is set when the calculated signal-to-noise ratio passes the 20 dB threshold.

7.3 Component processing

The SAA7154E; SAA7154H supports Y-P_B-P_R or RGB component inputs according to:

- 480i and 576i (standard definition and interlaced)
- 480p and 576p (HD0, double scan rate) at two-fold oversampling (54 MHz)
- 1080i and 720p (HD1), downsampled to 27 MHz pixel rate.

The SAA7154E; SAA7154H processes Y-P_B-P_R component video input in double scan representation, also known as 480p or 576p progressive video, at its natural pixel rate of 27 MHz. The SAA7154E; SAA7154H digitizes High Definition video (HD1), known as 1080i and 720p, at 54 MHz and samples it down to a pixel rate of 27 MHz. The SAA7154E; SAA7154H detects HD0 and HD1 signals (separate for 480p, 576p, 1080i, 720p) and sets I^2C-bus status bits. The SAA7154E; SAA7154H performs all necessary internal adjustments to support these standards.

HD0 signals can be output after the scaler (I-port) either at their natural resolution and bandwidth, e.g. as in *ITU-656* on 8 lines at 54 MHz clock rate or in *SMPTE293M* format (16 lines (Y-C_B -C_R) and 24 lines (RGB) at 27 MHz clock rate. Or they can be scaled to meet the particular requirements of the following signal processing or display, e.g. downscale to half the number of input lines. HD1 signals (720p, 1080i) can be output after the scaler (I-port) with reduced horizontal resolution.

7.4 Analog OSD processing

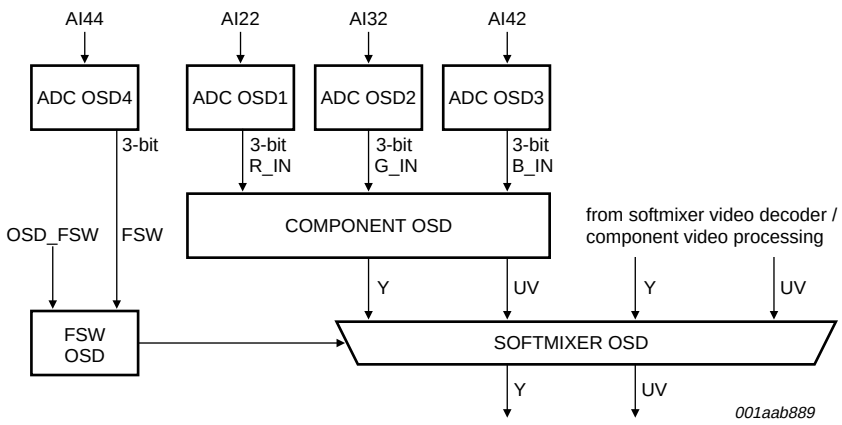


Fig 8. Functional overview of OSD

The OSD processing (see Figure 8) mixes the main video signal with an analog RGB OSD signal provided by an external device (e.g. teletext decoder SAA5697). Three ADCs (OSD1, OSD2 and OSD3) convert the three analog RGB inputs AI22, AI32 and AI42 into 3-bit digital streams.

The corresponding FSW signal is also converted from the analog input AI44 to a 3-bit digital signal by the separate ADC OSD4. The block FSW OSD processes the 3-bit FSW signal to a 9-bit alpha value, that indicates the ratio to mix the OSD signal with the main video.

7.5 Decoder output control and fader

When any valid input signal is missing, a blue screen signal can be inserted under software control in order to get a valid output signal. The function blue screen can be enabled by setting bit BSCR (extended register address 72h). I^2C-bus status bits provide criteria like horizontal or vertical lock.

7.6 Picture improvement and scaler

7.6.1 Picture improvement

All the picture improvement functions are available for all types of input signals including a digital Y-C_B-C_R applied to the X-port as an input.

7.6.1.1 Color improvement

The gravity functions take place in the C_B-C_R color domain. Colors in the vicinity of a specified color (e.g. **skin tone** for **skin tone correction** or green for **green enhancement**) are enhanced to be closer to the desired color value (see Figure 9). This gravity function is implemented three times and can be used for **skin tone correction**, **green enhancement** or **red apple** in any order. Only the **blue stretch function** is fixed since here a different algorithm is necessary.

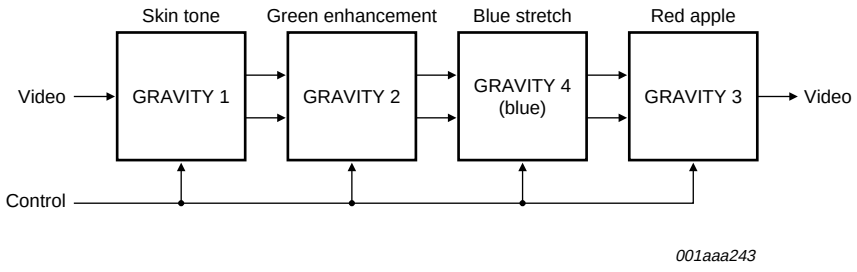


Fig 9. Simplified block diagram of gravity functions

A center of gravity in C_B-C_R space is defined. The range defines the zone of gravity impact. Further, the gravity weighting can be forced in four different steps. The strength of gravity is a function of the difference between the center of gravity and the actual C_B-C_R pixel.

Blue stretching: This **blue stretch** circuit is intended to shift color close to white with sufficient contrast towards more blue to obtain a brighter impression of the picture. The **blue stretch** gravity block works slightly different to the gravity block described above. The center of gravity here is not the same as the center of the programmable range. The center of range is fixed with $C_B = C_R = 0h$ whereas the center of gravity is blue.

To every C_B-C_R color vector falling into a range close to $C_B = C_R = 0h$ and accompanied by a relative luminance of at least 80 %, a certain portion of C_B color component is added. The range and strength of this operation is programmable.

Green enhancement: **Green enhancement** makes pictures with green content more vivid. All color vectors whose angles are within a predefined value for green hue are amplified around a center of gravity by a certain amount.

The position of the center of gravity, range and strength of this operation is programmable.

Adjustable skin tone correction: Automatic **skin tone correction**, also known as color trek or flesh tone correction, continuously evaluates the angle of the vector in the C_B-C_R color plane. Whenever particular pixel fall into a **skin tone** area, their vector is rotated (eventually stretched or squeezed in length), thus pointing into the direction of a programmable target angle and saturation around a center of gravity.

The position of the center of gravity, range and strength of this operation is programmable.

7.6.1.2 Color transient improvement

Color Transient Improvement (CTI) after the scaler block evaluates transients in the C_B-C_R domain and, depending on their amplitude, these transients are made steeper without generating overshoot. For a particular high-pass filter, center frequencies of approximately $0.125 \times f_{clk(o)(SC)}$ and $0.17 \times f_{clk(o)(SC)}$ can be selected ($f_{clk(o)(SC)}$ is the frequency of the scaler output clock, normally the clock at pin ICLK); thus the degree of slope improvement is proportional to the output (display) clock $f_{clk(o)(SC)}$. A higher subjective impression of sharpness is achieved especially for SECAM originated test signals.

7.6.1.3 Luminance sharpness control

The sharpness control (luminance peaking), also used in the SAA7118, is located after the video decoder block and a more versatile sharpness control has been added to part of the I-port processing chain.

Center frequencies of approximately $0.2 \times f_{clk(o)(SC)}$, $0.25 \times f_{clk(o)(SC)}$ and $0.3 \times f_{clk(o)(SC)}$ can be selected as shown in Figure 10; thus, the actual frequencies depend on the output (display) clock $f_{clk(o)(SC)}$. The amount of luminance peaking can be set from 0 dB to 12 dB in 8 steps.

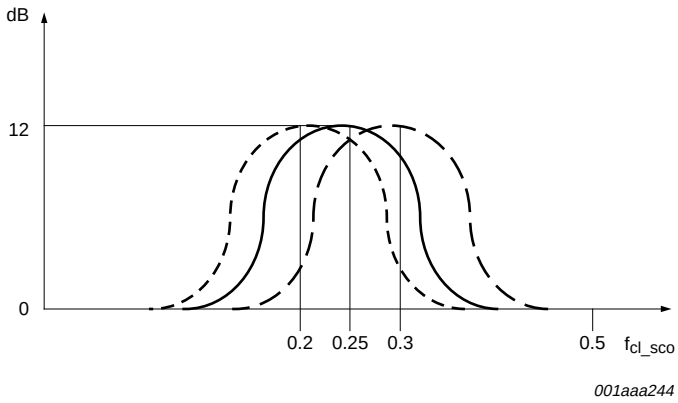


Fig 10. Center frequencies of luminance sharpness control

7.6.1.4 Histogram collection

The histogram collection provides the following features:

- Histogram adaption by means of three programmable Look-Up Tables (LUT) for:
  - Adaptive **black stretch**
  - **White stretch**
  - Dynamic Contrast Improvement (DCI)
- **Black and white stretching** by histogram evaluation.

Three programmable LUTs (each having 17 × 8-bit entries) after the scaler block can realize piecewise (16 segments) linear transfer characteristics for Y-C_B-C_R components. Evaluation of the statistical appearance of luminance sample codes over a programmable observation window (maximum of 2 interlaced video fields) by the system microcontroller can be utilized to load values s0 to s16 for the segments of the LUTs accordingly (see Figure 11); the remaining LUT entries are calculated automatically. The histogram result is readable as one byte through the I^2C-bus, where the mantissa and exponent values are each represented by 8-bit.

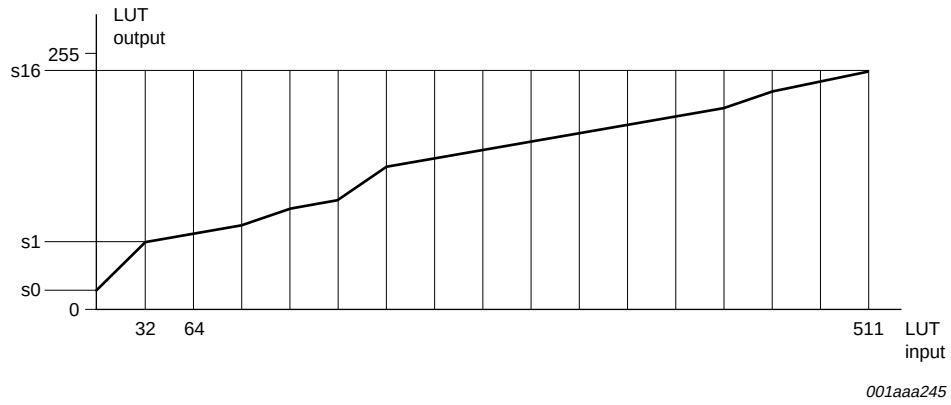


Fig 11. Programmable LUT characteristics

7.6.2 Scaler

The high-performance video scaler offers non-linear horizontal scaling, thus enabling e.g. optimized zooming of 4 : 3 sources to a 16 : 9 display (**panorama scaling**). An intrafield de-interlacer (no external memory needed) converts interlaced sources to progressive format, suitable for direct display on LCD panels. An on-chip display and raster generator enables direct driving of LCD panels.

The scaler has the following major blocks (see Figure 12):

- Acquisition control (horizontal and vertical timer) and task handling (region/field/frame based processing)
- Prescaler, for horizontal down-scaling by an integer factor, combined with appropriate band limiting filters, especially anti-aliasing for CIF format
- Brightness, saturation, contrast control to adjust scale-dependent amplification
- Line buffer, with asynchronous read and write, to support vertical up-scaling (e.g. for videophone application, converting 240 into 288 lines, Y-C_B-C_R 4 : 2 : 2)
- Vertical scaling, with phase accurate Linear Phase Interpolation (LPI) for zoom and downscale or phase accurate Accumulation Mode (ACM) for large downscaling ratios and better alias suppression
- A secondary vertical scaling unit, for EDGI, used for zooming up to progressive line counts
- Arithmetic unit, which does the calculations needed to support **panorama scaling** and keystone compensation
- Picture improvement processing (scaler post processing) containing simple peaking functions to improve the sharpness impression in luminance and chrominance, YUV to RGB or RGB to YUV conversions (including 16 segment curves) to support contrast/saturation and color manipulations
- Variable Phase Delay (VPD) operates as horizontal phase accurate interpolation for arbitrary non-integer scaling ratios. VPD supports conversion between **square pixel** sampling and rectangular pixel sampling, **panorama scaling** and keystone compensation.

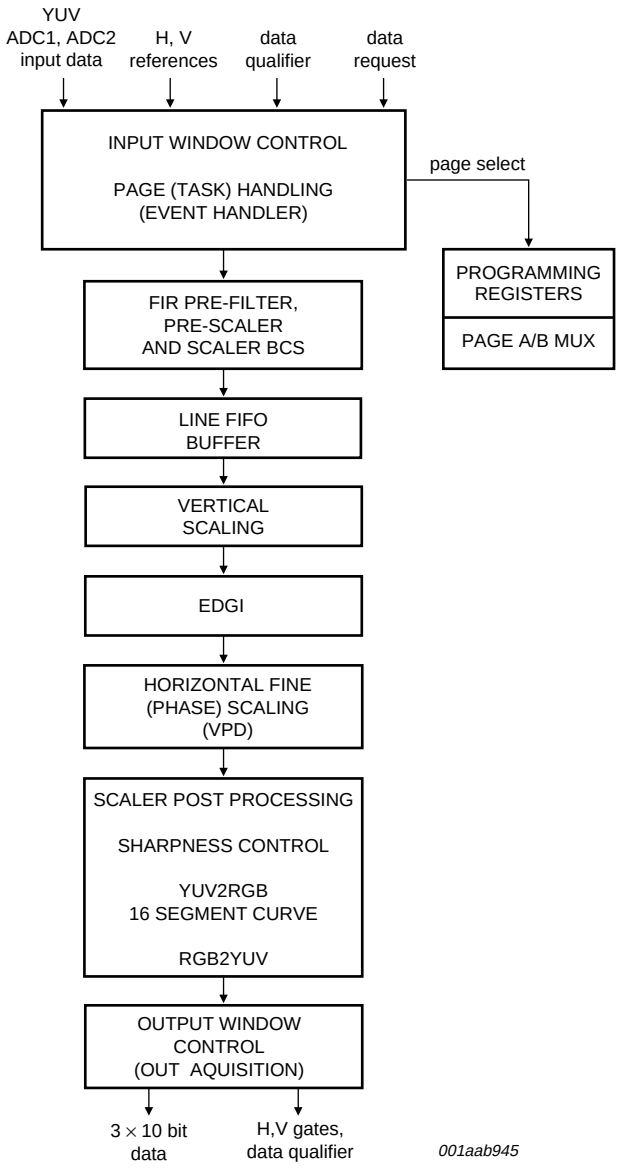


Fig 12. Functional block diagram of the scaler data path

The input/output data relation limits overall H and V zooming.

The video scaler receives its input signal from the video decoder or from the expansion port (X-port). It gets 16-bit Y-C_B-C_R 4 : 2 : 2 input data at a continuous rate of 13.5 MHz or 27 MHz from the decoder. A discontinuous data stream can be accepted from the expansion port (X-port), normally 8-bit wide *ITU-656* like Y-C_B-C_R data, accompanied by a pixel qualifier on pin XDQ.

The scaler operation is defined by two programming pages A and B, representing two different tasks, that can be applied field alternating or to define two regions in a field (e.g. with different scaling range, factors and signal source during odd and even fields).

Each programming page contains control for:

- Signal source selection and formats
- Task handling and trigger conditions
- Input and output acquisition window definition
- H-prescaler, V-scaler and H-phase scaling.

Raw VBI data is handled as specific input format and needs its own programming page (equals own task).

7.7 VBI data decoder and capture

The SAA7154E; SAA7154H contains a versatile VBI data decoder and the option of reading back sliced VBI data for low bit rate standards. All sliced VBI data are transported through the I-port and are mixed with the data from the scaler data path.

7.7.1 Versatile VBI data decoder

Versatile VBI data decoder, slicer, clock regeneration and byte synchronization e.g. for:

- WST525/WST625 (Chinese Character System Teletext (CCST))
- VPS
- US/European Closed Caption (CC), including XDS and V-chip
- WSS525, including Copy Generation Management System (CGMS)
- WSS625
- Line 41 CGMS of 480p (HD0) component video
- US NABTS
- VITC525/VITC625
- Gemstar1x
- Gemstar2x
- Moji.

7.7.2 I^2C-bus read back

I^2C-bus read back of the following decoded data types:

- US Close Caption (CC), including XDS and V-chip
- European Close Caption (CC)
- WSS525 (including CGMS)
- WSS625
- Gemstar1x
- Gemstar2x.

7.7.3 VBI data slicer

This circuitry recovers the actual clock phase during the clock run-in period, slices the data bits with the selected data rate and groups them into bytes. The bits are sliced in the order of their occurrence, so that normally the first bit becomes the LSB of the collected bytes. Especially for WSS625, the 6 bits, which represent a single symbol, are packed into

separate bytes (where the hardware sets the upper bits to 00b). For transfer over I-port the result is buffered into a dedicated VBI data FIFO with a capacity of 2 × 56 bytes (2 × 14 double words).

The programming registers 40h to 5Fh control the VBI data slicing and data transfer. Registers 40h and 58h control the slicing process itself. The Line Control Registers (LCR) define the data type (VBI data standard) to be decoded. The assignment of the LCR registers to the CVBS input lines depends on the parameter VOFF.

Table 5 shows the supported VBI standards for 60 Hz/525 lines signals (see Table 6 for 50 Hz/625 lines signals).

Table 5. 60 Hz/525 lines VBI data types supported by the data slicer block

Data type	60 Hz/525 lines VBI data standards			
	Description	Data rate (Mbit/s)	Framing code	Hamming check
Data types for SDTV input (subaddress 48h/4Ah address 09h control bit SEL_HD = 0b)				
0h	do not acquire (active video)	-	-	-
1h	US teletext (WST525)	5.7272	27h	always
2h	NABTS	5.7272	programmable	optional
3h	Moji	5.7272	programmable[1]	-
4h	US Closed Caption (CC 525 and Line 21)[2]	0.503	001b	-
5h	US Wide Screen Signalling (WSS525 and CGMS)	0.447443	10b	-
6h	VITC525	1.7898	10b	-
7h	Gemstar2x	1.007	4EDh	-
8h	Gemstar1x	0.503	001b	-
9h	reserved	-	-	-
Ah	Open1	5	programmable	-
Bh	Open2	5.7272	programmable	-
Ch	reserved	-	-	-
Dh	do not acquire (RAW)	-	-	-
Eh	do not acquire (test)	-	-	-
Fh	do not acquire (active video)	-	-	-
Data types for HDTV input (subaddress 48h/4Ah address 09h control bit SEL_HD = 1b)				
0h	do not acquire (active video)	-	-	-
1h to 4h	not supported	-	-	-
5h	CGMS-A	-	-	-
6h to Ch	not supported	-	-	-
Dh to Fh	do not acquire (active video)	-	-	-

[1] Should be set to 47h for Moji.

[2] Including eXtended Data Service (XDS), respectively V-chip.

Table 6. 50 Hz/625 Lines VBI data types supported by the data slicer block

Data type	50 Hz/625 lines VBI data standards			
	Description	Data rate (Mbit/s)	Framing code	Hamming check
Data types for SDTV input (subaddress 48h/4Ah address 09h control bit SEL_HD = 0b)				
0h	do not acquire (active video)	-	-	-
1h	European teletext (WST 625) and Chinese teletext (CCST 625)	6.9375	27h	always
2h	Euro teletext with programmable Framing Code	6.9375	programmable	optional
3h	reserved	-	-	-
4h	Euro Closed Caption (CC625)	0.500	001b	-
5h	Euro Wide Screen Signalling (WSS625)	5	1E 3C1Fh	-
6h	VITC625	1.8125	10b	-
7h	VPS	5	9951h	-
8h	reserved	-	-	-
9h	reserved	-	-	-
Ah	open1	5	programmable	-
Bh	open2	5.7272	programmable	-
Ch	reserved	-	-	-
Dh	do not acquire (RAW)	-	-	-
Eh	do not acquire (test)	-	-	-
Fh	do not acquire (active video)	-	-	-

7.8 Image port output interface

The output interface consists of an output formatter, a FIFO for video and for sliced text data, an arbitration circuit which controls the mixed transfer of video and sliced text data over the I-port and a decoding and multiplexing unit which generates the 8-bit or 16-bit wide output data stream and the accompanied reference and supporting information.

The clock for the output interface can be derived from an internal clock (decoder or X-port), from the second internal PLL set (registers PLL2 and CGC2) or from an externally provided clock which is appropriate for e.g. VGA and frame buffer. The clock can be up to 54 MHz.

The scaler provides the following video related timing reference events (signals) through pins IPG0, IGP1, IGPH, IGPV and IDQ:

- Output field ID
- Start and end of vertical active video range
- Start and end of active video line
- Data qualifier or gated clock (only for **DMSD2-legacy mode**, bits ICKS[3:2]; see Table 17)
- Actually activated programming page (if CONLH is used)
- Threshold controlled FIFO filling flags (empty, full, filled)
- Sliced data marker.

The data stream at the scaler output is accompanied by a data valid flag (or data qualifier).

The discontinuous output data after the scaling process can be output as they occur or the data may be packed to continuous output lines by means of a trigger mechanism, which is controlled by a separate sync generator.

Clock cycles with invalid data on the I-port data bus (including pins HPD[7:0] in 16-bit output mode) can be handled in two different ways (controlled by bit INS80). As before, invalid cycles may be marked with 00h, but additionally a blanking value insertion (80h and 10h) is implemented as required by *ITU-656*.

The output interface also arbitrates the transfer between scaled video data and sliced text data over the I-port output. The bits SLDOM and VITX control the arbitration.

As a further operation the serialization of the internal double pixel double words to 8-bit, 16-bit or 24-bit output, as well as the insertion of the extended *ITU-656* codes (SAV/EAV for video data, ANC or SAV/EAV codes for sliced text data) are done here. Setting bit ICODE = 1b activates the leading/trailing sequences. For 16-bit and 24-bit output modes (bits ICKS[3:2] = 00b) the leading/trailing sequences occur on each 8-bit wide port as a serial byte pattern.

When any valid input signal is missing, a blue screen signal can be inserted under software control in order to get a valid output signal. I^2C-bus status bits provide criteria like horizontal or vertical lock.

7.9 Digital OSD

The SAA7154E; SAA7154H can perform overlay of On-Screen-Display (OSD) information in display (panel) raster timing by using the digital OSD function. For the digital OSD function, a separate combined input port (3-bit data, 1-bit switch control) is available behind the scaler, programmable color mapping of the data bits is provided. Appropriate OSD controllers can insert menu overlay and the like, unaffected of any scaling ratio, thus providing optimum readability.

When any valid input signal is missing, a blue screen signal can be inserted under software control in order to get a valid RGB output signal. I^2C-bus status bits provide criteria like horizontal or vertical lock. The SAA7154E; SAA7154H can perform overlay of On-Screen-Display (OSD) information for RGB output signals on I-port. The OSD information runs in display panel raster timing. For an application example Figure 24.

7.10 Interrupt control

The SAA7154E; SAA7154H is able to generate an interrupt (pin INT_A, open-drain, active LOW) from up to 16 important internal status signals (see Table 7). The usage of these status signals for the interrupt generation must be enabled by writing the interrupt mask registers at 2Dh to 2Fh from the first I^2C-bus slave address, except PRDON, which is always enabled. By default all interrupts are disabled (except PRDON). An interrupt will be deasserted once the status register containing the corresponding status bit is read.

The status information read after an interrupt will always be the **latest** state, therefore the status is not **frozen** when an interrupt is generated. If there is a delay in reading an interrupt status, the interrupt condition may be superseded by the next other one.

The exception to the above is the VBI interrupt bit whose status is frozen when a VBI event occurs. It is set only if its mask bit is set and an **end of VBI** event occurs. An additional **interrupt lost** signal is available for software to check whether all VBI data has been read. It is asserted if the VBI interrupt bit is still set when the next **end of VBI** event occurs.

Remark: if a new interrupt condition occurs at the **same** time (at clock enable) as a status is being read, the flag will **not** be cleared.

Table 7. List of status signals for which an interrupt can be initiated

Status	Description	Address	Active edge
RDCAP	ready for capture (all internal loops locked) for SDTV signals	42h/40h - 1Fh	both edges
COPRO	copy protected source detected according to Macrovision version up to 7.01 (SDTV)	42h/40h - 1Fh	both edges
COLSTR	Macrovision encoded color stripe burst detected (any type)	42h/40h - 1Fh	both edges
TYPE3	Macrovision encoded color stripe burst type 3 (4 line version) detected (SDTV)	42h/40h - 1Fh	both edges
FIDT	identification bit for detected field frequency (SDTV)	42h/40h - 1Fh	both edges
HLVLN	status bit for horizontal and vertical loop (SDTV)	42h/40h - 1Fh	both edges
INTL	status bit for interlace detection (SDTV)	42h/40h - 1Fh	both edges
DCSTD[1:0]	detected color standard (SDTV)	42h/40h - 1Eh	both edges
HLCK	status bit for locked horizontal frequency (SDTV)	42h/40h - 1Eh	both edges
NFLD	status bit for field length (SDTV)	42h/40h - 1Eh	both edges
ERROF	error output formatter scaler	42h/40h - 8Fh	rising edge
VBI_IRQ	end of VBI region interrupt (no status, this bit will only be set if the corresponding mask bit is set and the event occurs)	42h/40h - 8Fh	falling edge
PRDON	power-down status signal	42h/40h - 8Fh	falling edge
HD_COPRO	copy protected HDTV source detected according to Macrovision version up to 7.01	4Ah/48h - 1Fh	both edges
HD_RDCAP	ready for capture (all internal loops locked) (HDTV)	4Ah/48h - 1Fh	both edges
HD_HL	horizontal lock flag (HDTV)	4Ah/48h - 1Fh	both edges

7.11 Clock generation

A first Clock Generation Circuit (CGC) receives a synthesized reference signal which is line-locked to the active incoming analog video. It acts like an analog tracking filter in order to remove residual jitter from the sampling clock.

In a similar way, a second clock generator is capable to output video data in **square pixel** formats:

- PAL video line is output with 768 active video pixel at 29.5 MHz **square pixel** clock frequency
- NTSC Video line is output with 640 active video pixel at 24.54 MHz **square pixel** clock frequency.

An other option is to use the second CGC for jitter removal from the frame-locked audio clock generated inside the SAA7154E; SAA7154H.

Supported audio clock frequencies of the low jitter frame locked audio clock from the audio master clock are (with f_s = 32 kHz, 44.1 kHz or 48 kHz):

- $256 \times f_s$
- $384 \times f_s$
- $512 \times f_s$.

7.12 I²C-bus slave transmitter

Due to the number of new functions in the SAA7154E; SAA7154H, two I²C-bus slave addresses are required for full control of all registers. In order to auto control two decoder devices independently, pin RTCO = logic 0 enables slave addresses (write) 42h and 4Ah and pin RTCO = logic 1 enables slave addresses (write) 40h and 48h. For a read access, addresses are incremented by one as usual.

Do not connect the output pin RTCO directly to ground or power supply. Use a pull-down or pull-up resistor of 4.7 kΩ instead.

7.13 Power and reset control

7.13.1 Power-on reset and chip enable input

A missing XTAL clock, insufficient digital or analog V_{DD} supply voltages (below 2.0 V for nominal 3.3 V pins and below 1.2 V for nominal 1.8 V supply pins) will start the reset sequence. All outputs are forced to 3-state. The indicator output pin RES_N = logic 0 for approximately 2000 XTAL cycles after the internal reset and can be applied to reset other circuits of the digital TV system. The reset will release if the supply increases above 1.4 V (for 1.8 V supply) and 2.5 V (3.3 V supply).

It is possible to force a reset by pulling the chip enable input (pin CE) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2_54 and SDA return from 3-state to active, while the other signals have to be activated through programming.

With this procedure the order of applying the different voltages is not important:

- Set CE = logic 1
- Apply all supplies
- Wait for 5 ms
- Set CE = logic 0
- Wait for 1 µs
- Set CE = logic 1
- Wait for 1 ms
- Start I²C-bus initialization.

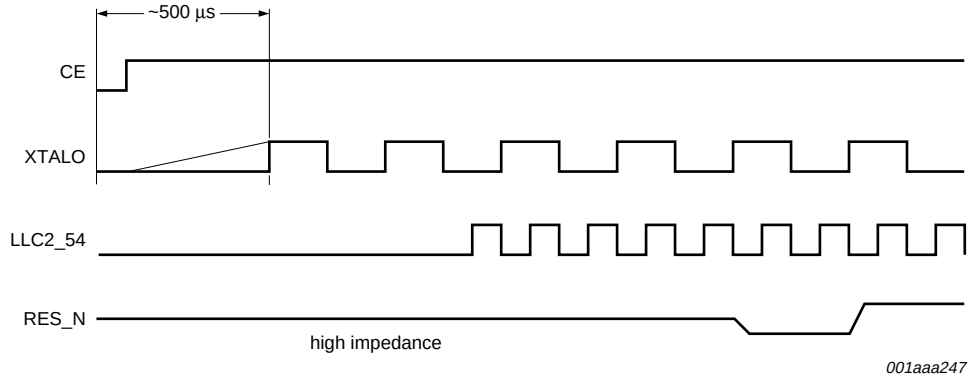


Fig 13. Timing diagram of reset sequence

7.13.2 Initial programming sequence after power-on

After power-on a sequence of register changes needs to be performed, due to internal dependencies on the clock generation:

1. The first programming of the device needs to be done with slave address 42h/40h, bits XPE[1:0] = 01b
2. Program slave address 42h/40h, bit CG1EN = 0b and afterwards set bit CG1EN = 1b
3. If the X-port is not needed, program slave address 42h/40h, bits XPE[1:0] = 00b
4. To activate the I-port output program slave address 42h/40h, bit SWRST = 0b and afterwards set bit SWRST = 1b.

7.13.3 Power-down

Follow this procedure to initiate the power-down mode:

- Set MODE[5:0] = 24h
- Set pin CE = logic 0.

7.14 Input and output interfaces and ports

The SAA7154E; SAA7154H has nine different I/O interfaces:

- Analog video input interface, for analog CVBS and/or Y and C input signals and/or component video signals
- Analog OSD input interface
- Digital OSD input interface
- Audio clock port
- Digital real-time signal port (RT-port)
- Digital video expansion port (X-port), for unscaled digital video input and output
- Digital image port (I-port) for scaled video data output
- Digital host port (H-port) for extension of the image port or expansion port from 8-bit to 16-bit
- Digital I-port extension bus (IX-port) for expansion of the data output to 24-bit.

7.14.1 Analog terminals

The SAA7154E; SAA7154H has 16 analog inputs AI41 to AI44, AI31 to AI34, AI21 to AI24 and AI11 to AI14 for composite video CVBS or s-video Y/C signal pairs or component video input signals RGB plus separate sync (or Y-P_B-P_R plus separate sync).

Component signals with e.g. sync-on-Y or sync-on-green are also supported; they are fed to two ADC channels, one for the video content, the other for sync conversion. Additionally, there are four differential reference inputs which must be connected to ground through a capacitor equivalent to the decoupling capacitors at the 16 inputs. There are no peripheral components required other than these decoupling capacitors and termination resistors, one set per connected input signal.

When using the OSD feature in combination with the SAA5697HL, the analog pins AI22, AI32, AI42 and AI44 are reserved for analog OSD and can not be used for other input sources.

Clamp and gain control for the four ADCs are also integrated. Two analog video outputs (pins AOUT1 and AOUT2) are provided. They can be used for analog output for one of the input signals. In addition, pin AOUT2 can output the sum of two analog input signals. This can be used for CVBS generation from an Y/C signal.

Table 8. Analog pin description

Pin	I/O	Description	Control through
AI11 to AI14	I	analog video signal inputs, e.g. 16 CVBS signals or eight Y/C pairs or four RGB plus separate sync (or Y-P_B-P_R plus separate sync) signal groups can be connected simultaneously to this device; many combinations are possible	MODE[5:0]
AI21 to AI24			
AI31 to AI34			
AI41 to AI44			
AOUT1	O	analog video output 1	AOSL1[3:0]
AOUT2	O	analog video output 2	AOSL2[1:0], AOSL2A[1:0] and AOSL2B[1:0]
AI1D, AI2D, AI3D and AI4D	I	analog reference pins for differential ADC operation; connect to ground through 47 Ω/22 nF	-

7.14.2 Audio clock signals

The SAA7154E; SAA7154H also synchronizes the audio clock and sampling rate to the video frame rate through a very slow PLL. This ensures that multimedia capture and compression processes always gather the same predefined number of samples per video frame.

An audio master clock AMCLK and two divided clocks ASCLK and ALRCLK are generated:

- ASCLK: can be used as audio serial clock
- ALRCLK: audio left/right channel clock.

The ratios are programmable.

Table 9. Audio clock pin description

Pin	I/O	Description	Control through
AMCLK	O	audio master clock output	ACPF[17:0] and ACNI[21:0]
AMXCLK	I	external audio master clock input for the clock division circuit; can be directly connected to output AMCLK for standard applications	-
ASCLK	O	serial audio clock output; can be synchronized to rising or falling edge of AMXCLK	SDIV[5:0] and SCPH
ALRCLK	O[1]	audio channel (left/right) clock output; can be synchronized to rising or falling edge of ASCLK	LRDIV[5:0] and LRPH

[1] See Table 4.

7.14.3 Clock and real-time synchronization signals at the RT-port

The generation of the line-locked video clock LLC (pixel clock) and of the frame-locked audio serial bit clock requires a crystal accurate frequency reference. An oscillator is built-in for fundamental or third harmonic crystals (the SAA7154E; SAA7154H supports crystals with 32.11 MHz or 24.576 MHz). Alternatively, pin XTALI can be driven from an external single-ended oscillator.

The crystal oscillation can propagate as a clock to other ICs in the system through pin XTOUT.

The Line-Locked Clock (LLC) is the double pixel clock of the nominal 27 MHz in case of SDTV signals (pixel clock for HDTV). It is locked to the selected video input, generating baseband video pixel according to *ITU recommendation 601*. In order to support interfacing circuits, a direct pixel clock (LLC2) for SDTV-signals is also provided.

The pins for line and field timing reference signals are RTCO, RTS1 and RTS0. Various real-time status information can be selected for the RTS pins. The signals are always available (output) and reflect the synchronization operation of the decoder part in the SAA7154E; SAA7154H.

Table 10. Clock and real-time synchronization signals

Pin	I/O	Description	Control through
Crystal oscillator			
XTALI	I	input for crystal oscillator or reference clock	-
XTALO	O	output of crystal oscillator	-
XTOUT	O	reference (crystal) clock output drive (optional)	XTOUTE
Real-time signals (RT-port)			
LLC	O	line-locked clock, nominal 27 MHz, double pixel clock locked to the selected video input signal (pixel clock in case of HDTV)	-
LLC2_54	O	line-locked pixel clock, nominal 13.5 MHz; or ADC clock 54 MHz; selectable through I^2C-bus	SLLC2

Table 10. Clock and real-time synchronization signals *...continued*

Pin	I/O	Description	Control through
RTCO	O[1]	real-time control output, transfers real-time status information supporting RTC level 3.1	-
RTS0	O	real-time status information line 0, can be programmed to carry various real-time information	RTSE0[3:0]
RTS1	O	real-time status information line 1, can be programmed to carry various real-time information	RTSE1[3:0]

[1] See Table 4.

7.14.4 Video expansion port through the X-port

7.14.4.1 General

The expansion port (X-port) can be used either to output 8-bit or 10-bit video from the comb filter decoder or component path directly or to receive video data from other external digital video sources such as a MPEG decoder for output at the image port (I-port). The X-port output is only capable of delivering SDTV signals; HDTV output is only possible through I-port and H-port.

The input and output direction is switched under the control of bits XPE[2:0] and pin XTRI:

- Output mode:
  - 8-bit dithered (noise shaped) or 10-bit data output of component video Y-C_B-C_R 4 : 2 : 2, i.e. in C_B-Y-C_R-Y, sequence
  - The SAV and EAV codes can be inserted optionally for data output, controlled by bit OFTS[3:0]
  - In 10-bit wide video mode the two data LSBs are output on the XRH and XRV signal lines
  - Clock, synchronization and auxiliary I/O signals accompany the data stream.
- Input mode:
  - 8-bit data input of component video Y-C_B-C_R 4 : 2 : 2, i.e. C_B-Y-C_R-Y, byte serial
  - In input mode, optionally the data bus can be extended to 16-bit by pins HPD[7:0]. In this mode, pins XPD[7:0] carry the luminance data and pins HPD[7:0] carry the chrominance data
  - The SAV and EAV codes can be applied optionally for data input, selected by bit XCODE
  - Clock, synchronization and auxiliary I/O signals accompany the data stream.

Remark: The I-port configuration controls the enable of the H-port. Table 11 lists the possible I/O configurations.

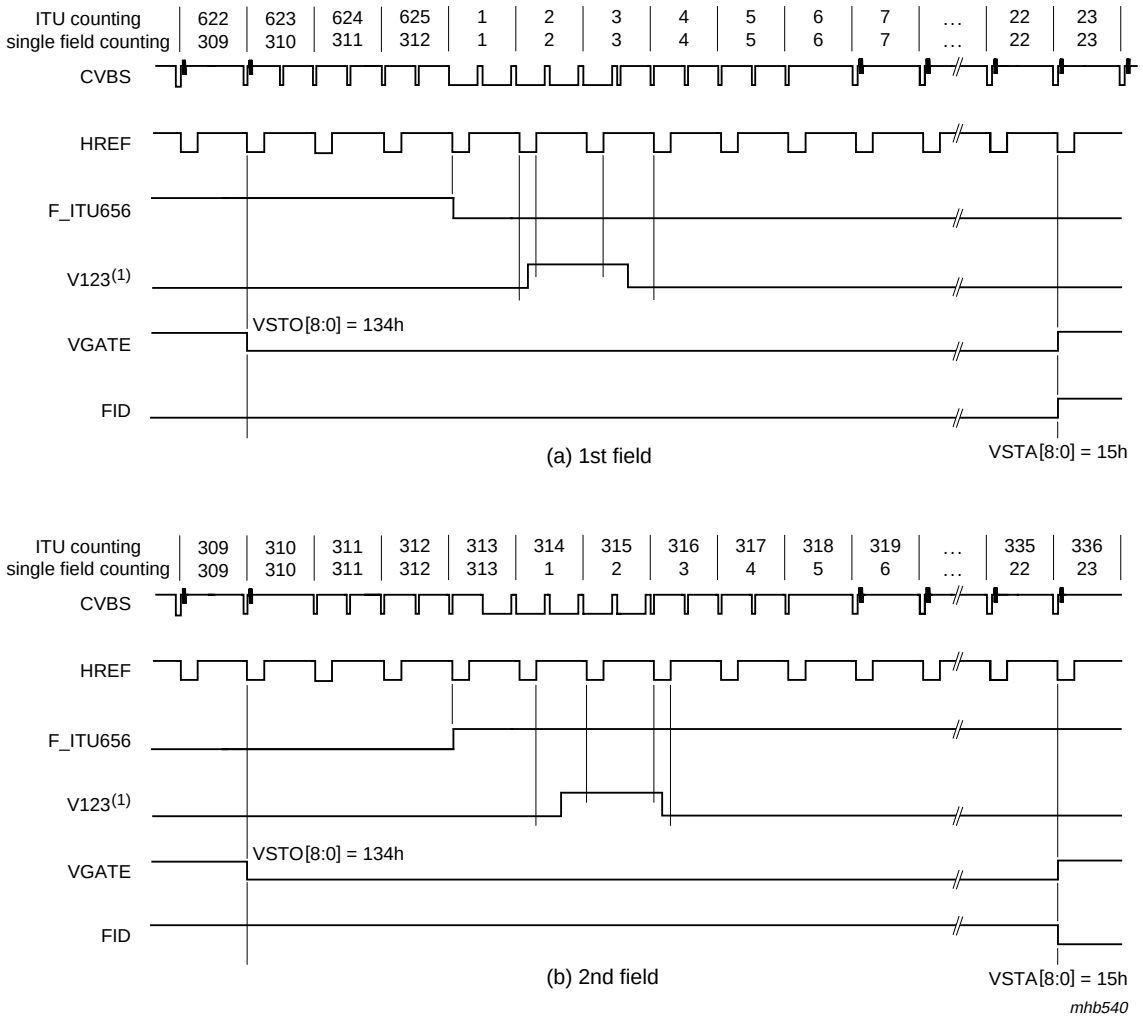
Table 11. Signals dedicated to the expansion port

Pin	I/O	Description	Control through
XPD7 to XPD0	I/O	X-port data: in output mode controlled by decoder section; in input mode Y-C_B-C_R 4 : 2 : 2 serial input data or luminance part of a 16-bit Y-C_B-C_R 4 : 2 : 2 data stream	OFTS[3:0], CONLV, HLDFV, SCSRC[1:0], SCRQE and FSC[2:0]
HPD7 to HPD0	I/(O)	H-port data: with the X-port, these signals are used as input only, for 16-bit Y-C_B-C_R 4 : 2 : 2 video data. In this case HPD[7:0] carries chrominance data. The output enable is controlled through the output configuration as defined by FSI and SWAPO	ICKS[3:0], SCSRC[1:0], FSI[2:0] and SWAPO
XCLK	I/O	clock at expansion port: if output, then copy of LLC; as input normally a double pixel clock of up to 32 MHz or a gated clock (clock gated with a qualifier)	XCKS
XDQ	I/O	data valid flag of the expansion port input (qualifier): if output, then decoder (HREF and VGATE) gate	-
XRDY	O	data request flag to ready to receive, to work with optional buffer in external device, to prevent internal buffer overflow; second function: input related task flag A/B	XRQT
XRH	I/O	horizontal reference signal for the X-port: as output: HREF, HS or HVGATE from the decoder; optionally bit 1 of X-port 10-bit decoder output; as input: a reference edge for horizontal input timing and a polarity for input field ID detection can be defined	OFTS[3:0], XRHS[1:0], XFDH and XDH
XRV	I/O	vertical reference signal for the X-port: as output: V123 or field ID from the decoder (see Figure 14 and 15); optionally bit 0 of X-port 10-bit decoder output; as input: a reference edge for vertical input timing and for input field ID detection can be defined	OFTS[3:0], XRVS[1:0], XFDV and XDV[1:0]
XTRI	I	port control: switches X-port input 3-state	XPE[2:0]

7.14.4.2 Timing

Table 12. Availability of control signals for 50 Hz/625 and 60 Hz/525 line systems

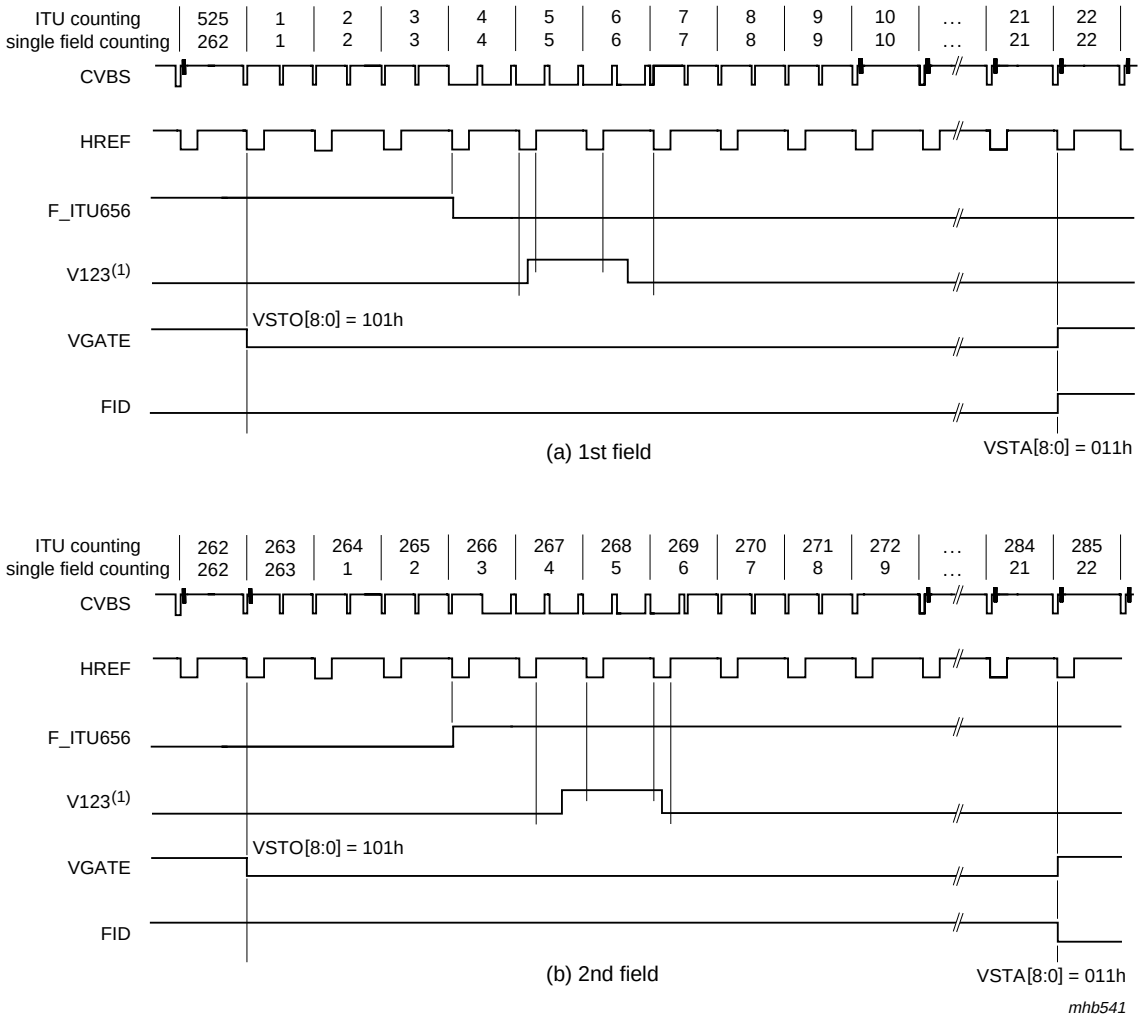
Control signal	Pin			
	RTS0	RTS1	XRH	XRV
HREF	X	X	X	-
F_ITU656	-	-	-	X
V123	X	X	-	X
VGATE	X	X	-	-
FID	X	X	-	-
HS	X	X	X	-
CREF2	X	X	-	-
CREF	X	X	-	-



(1) The signal HREF at the negative edge of signal V123 indicates whether this field is odd or even. If HREF is logic 1, the field is odd (field 1) and if HREF is logic 0, the field is even.

The control signals are available on the pins listed in Table 12. The polarity of the signals HREF, HS, CREF2 and CREF can be inverted by bits RTP0 or RTP1.

Fig 14. Vertical timing diagram for 50 Hz/625 line systems



(1) The signal HREF at the negative edge of signal V123 indicates whether this field is odd or even. If HREF is logic 1, the field is odd (field 1) and if HREF is logic 0, the field is even.

The control signals are available on the pins listed in Table 12. The polarity of the signals HREF, HS, CREF2 and CREF can be inverted by bits RTP0 or RTP1.

Fig 15. Vertical timing diagram for 60 Hz/525 line systems

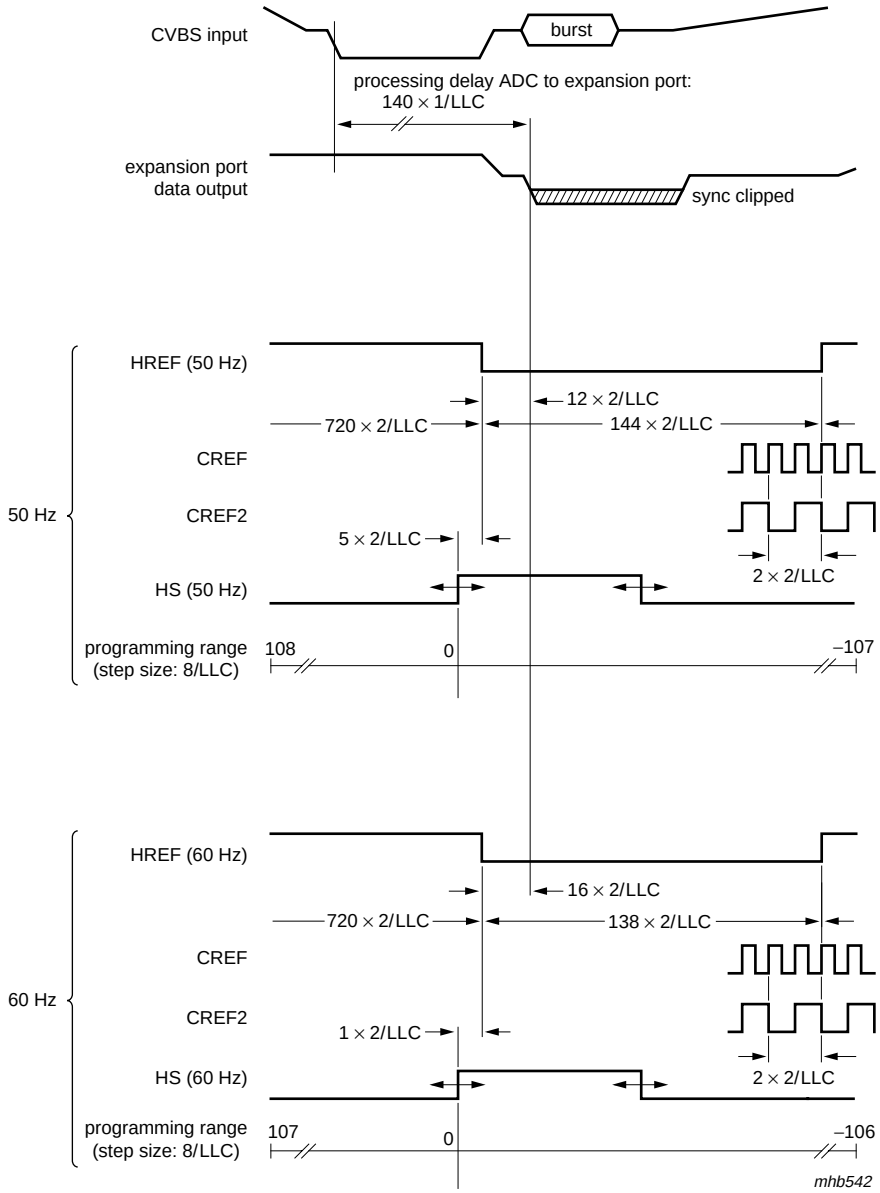


Fig 16. Horizontal timing diagram (50 Hz/60 Hz)

7.14.4.3 X-port configured as output

If data output is enabled at the expansion port, then the data stream from the decoder is presented. The data format of the 8-bit/10-bit data bus is dependent on the chosen data type, selectable by the line control registers LCR2 to LCR24. In contrast to the image port, the sliced data format is not available on the expansion port. Instead, raw CVBS samples are always transferred if any sliced data type is selected. Currently only SDTV-signals can be transmitted. HDTV transmission is only possible through I-port and H-port.

7.14.4.4 X-port configured as input

If data input mode is selected at the expansion port, then the scaler can choose its input data stream from the on-chip video decoder or from the expansion port (controlled by bits SCSRC[1:0]). Byte serial or 16-bit wide Y-C_B-C_R 4 : 2 : 2 or subsets for other sampling schemes or raw samples from an external ADC may be input (bits FSC[2:0]; see Table 17), where the H-port serves as the port for the chrominance input path. Optionally, pixelwise switching between video from the decoder and expansion port (X-port) input is also used (special configuration controlled by XPE).

As the output configuration (8-bit, 16-bit or 24-bit) has priority and controls the H-port enable, 16-bit input is only supported for 8-bit wide output through the I-port.

The input stream must be accompanied by an external clock (pin XCLK), qualifier XDQ and reference signals XRH and XRV. Instead of the reference signal, embedded SAV and EAV codes according to *ITU-656* are also accepted. The protection bits are not evaluated.

For using the raster generator or PLL2 on the X-port input stream the pins XRH and XRV must be applied with sync signals.

7.14.5 Image port and digital OSD

7.14.5.1 Image port

The Image port (I-port) transfers data from the scaler as well as from the VBI data slicer, if selected (maximum 54 MHz). The reference clock is available at the ICLK pin, as an output or as an input (maximum 54 MHz). As output, ICLK is derived from the line-locked decoder, 2nd PLL or expansion port input clock. The data stream from the scaler output is normally discontinuous. Therefore valid data during a clock cycle is accompanied by a data qualifying (data valid) flag on pin IDQ. In the so called **DMSD2-legacy mode** (ICKS[3:2] = 10b) the IDQ pin carries a gated clock signal.

The data formats at the image port are defined in double pixel double words, such as the related internal FIFO structures. However, the physical data stream at the image port is only 24-bit, 16-bit or 8-bit wide. In 16-bit mode, data pins HPD[7:0] are used for chrominance data. In 24-bit mode, pins IPD[7:0], IXD[7:0] and HPD[7:0] can be used to output Y-C_B-C_R 4 : 4 : 4 or R-G-B 4 : 4 : 4 data.

Available formats are as follows:

- Y-C_B-C_R 4 : 2 : 2 with 8-bit or 16-bit
- Y-C_B-C_R 4 : 1 : 1 with 8-bit
- Y-C_B-C_R 4 : 4 : 4 with 24-bit
- R-G-B 4 : 4 : 4 with 24-bit
- Raw samples
- Decoded VBI data.

For handshake with the receiving VGA controller or other memory or bus interface circuitry, F, H and V reference signals and programmable FIFO flags are provided. The information is provided on pins IGP0, IGP1, IGPH and IGPV. I^2C-bus registers control the functionality of these pins.

Table 13. Signals dedicated to the image port

Pin	I/O	Description	Control through
IPD7 to IPD0	O	I-port data: serial 8-bit YUV 4 : 2 : 2 or luminance (Y) component or green (G) component	ICODE, ISWP[1:0] and IPE[1:0]
HPD7 to HPD0	I/O	H-port data: used in output mode with the I-port, this is the 16-bit extension for digital output (chrominance component (serial UV) or the U or blue (B) component in 4 : 4 : 4 output mode); the output configuration, defined by FSI and SWAPO, controls the output enable	FSI[2:0], ICKS[1:0], IPE[1:0] and SWAPO
IXD7 to IXD0	O	extended I-port data: used in output mode with the I-port, this is the 24-bit extension of the digital output (the V or red (R) component in 4 : 4 : 4 output mode), output only	FSI[2:0], ICKS[1:0], IPE[1:0] and SWAPO
ICLK	I/O	continuous reference clock at I-port, can be input or output, as output decoder LLC, 2nd PLL clock or XCLK from X-port	ICKS[1:0] and IPE[1:0]
IDQ	O	data valid flag at image port, qualifier, with programmable polarity; secondary function: gated clock	ICKS2, IDQP and IPE[1:0]
IGPH	O	horizontal reference output signal, copy of the H-gate signal of the scaler, with programmable polarity; alternative function: HRESET pulse	IDH[1:0], IRHP and IPE[1:0]
IGPV	O	vertical reference output signal, copy of the V-gate signal of the scaler, with programmable polarity; alternative function: VRESET pulse	IDV[1:0], IRVP and IPE[1:0]
IGP1	O	general purpose output signal for I-port	IDG1[2], IDG1[1:0], IG1P and IPE[1:0]
IGP0	O	general purpose output signal for I-port	IDG0[2], IDG0[1:0], IG0P and IPE[1:0]
ITRDY	I[1]	target ready input signals	-
ITRI	I	port control, switches I-port into 3-state	IPE[1:0]

[1] See Table 4.

7.14.5.2 Digital OSD

It is possible to insert OSD-information into the I-port video signal. This can be done with an external OSD controller, which is connected to the IPORT clock (ICLK), the I-port sync signals (IGPH and IGPV) and the OSD control pins (OSD[3:0]).

Table 14. Digital OSD

Symbol	I/O	Description	Control through
OSD_FSW	I[1]	digital OSD on/off	OSD_LUT and OSD_CONTROL
OSD3 to OSD1	I[1]	digital OSD selection of OSD bank	OSD_LUT and OSD_CONTROL

[1] See Table 4.

7.15 I²C-bus registers

7.15.1 Register overview of basic functions

Access the registers from Table 15 through the slave write address 42h/40h.

Table 15. I²C-bus basic functions overview

Address	Basic register function	Reference
00h	chip version part	Table 16
01h to 1Fh	video decoder part	Table 17
20h to 2Fh	component processing and interrupt masking	Table 18
30h to 3Fh	audio clock generator	Table 19
40h to 7Fh	general purpose VBI data slicer	Table 20
X-port, I-port and scaler		
8h0 to 8Fh	task independent global settings 1	Table 21
9h0 to BFh	task A definition:	Table 22
	basic settings and acquisition window definition	
	FIR filtering and prescaling	
	horizontal phase scaling	
	vertical scaling	
C0h to EFh	task B definition:	Table 23
	basic settings and acquisition window definition	
	FIR filtering and prescaling	
	horizontal phase scaling	
	vertical scaling	

Table 16. Register 00h used by chip version part

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Chip version[1]	00h	0	0	CV[1:0]		CID[3:0]			

[1] Read only.

Table 17. Registers 01h to 1Fh used by the video decoder part

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Increment delay and analog input control 0	01h	DFQBP	WPOFF	PFSL[1:0]		IDEL[3:0]			
Analog input control 1	02h	DF1BP	DF2BP	MODE[5:0]					
Analog Input control 2	03h	XPMODE	MVCEN	0	GAFIXA	HOLDG	GAFIXD	AGA2[2]	AGA1[2]
Analog Input control 3	04h	AGA1[1:0]		DGA1[5:0]					
Analog Input control 4	05h	AGA2[1:0]		DGA2[5:0]					
Horizontal sync start	06h	HSB[7:0]							
Horizontal sync stop	07h	HSS[7:0]							
Sync control	08h	AUFD	FSEL	FOET	HTC[1:0]		HPLL	VNOI[1:0]	
Luminance control	09h	BYPS	YCOMB	LDEL	LUBW	LUFI[3:0]			
Luminance brightness adjustment	0Ah	DBRI[7:0]							
Luminance contrast adjustment	0Bh	DCON[7:0]							
Chrominance saturation adjustment	0Ch	DSAT[7:0]							
Chrominance hue control	0Dh	HUEC[7:0]							
Chrominance control 1	0Eh	CDTO	CSTD[2:0]			DCVF	FCTC	AUTO[0]	CCOMB
Chrominance gain control	0Fh	ACGC/ CGAIN[7]	CGAIN[6:0]						
Chrominance control 2	10h	OFFU[1:0]		OFFV[1:0]		CHBW	LCBW[2:0]		
Mode and delay control	11h	COLO	RTP1	HDEL[1:0]		RTP0	YDEL[2:0]		
RT signal control	12h	RTSE1[3:0]				RTSE0[3:0]			
RT-port and X-port output control	13h	RTCE	XRHS[0]	XRVS[1:0]		HLSEL	OFTS[2:0]		
Analog output control and automatic standard detection	14h	AOSL1[3:0]				XTOUTE	AUTO[1]	0	0
VGATE start, FID change	15h	VSTA[7:0]							
VGATE stop	16h	VSTO[7:0]							
MISC and VGATE MSBs	17h	LLCE	LLC2E	LATY[2:0]			VGPS	VSTO[8]	VSTA[8]

Table 17. Registers 01h to 1Fh used by the video decoder part *…continued*

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Raw data gain	18h	RAWG[7:0]							
Raw data offset	19h	RAWO[7:0]							
Color killer	1Ah	QTHR[3:0]				STHR[3:0]			
MISC and TVVCRDET	1Bh	ATVT[1:0]		CM99	OFTS[3]	VNORST	VNOMAX	ACOL	FSQC
Enhanced comb control 1	1Ch	HODG[1:0]		VEDG[1:0]		MEDG[1:0]		CMBT[1:0]	
MISC and enhanced comb control 2	1Dh	VPLLDIS	XRHS[1]	SLLC2	ASHORT	FPLL	0	VEDT[1:0]	
Status byte decoder 1[1]	1Eh	NFLD	HLCK	AGLMT	AGLMB	DGLMT	DGLMB	DCSTD[1:0]	
Status byte decoder 2[1]	1Fh	INTL	HLVLN	FIDT	STTB	TYPE3	COLSTR	COPRO	RDCAP

[1] Read only.

Table 18. Register 20h to 2Fh used for component processing and interrupt masking

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Fast switch status	20h	0	0	FSWS[5:0]					
Analog input control 5	21h	0	0	0	0	0	EXMCE	AGA4[2]	AGA3[2]
Analog input control 6	22h	AGA3[1:0]		DGA3[5:0]					
Analog input control 7	23h	AGA4[1:0]		DGA4[5:0]					
Fast switch control 1	24h	0	0	0	0	FSRND	FSSHFT[2:0]		
Fast switch control 2	25h	FSLEN[1:0]		FSOFFS[5:0]					
Fast switch control 3	26h	FSWSEL	FSWI	1	FSDEL[4:0]				
Overlay control	27h	0	0	0	0	0	OVMOD[2:0]		
Component dither, peaking, delay	28h	0	0	CDITH[1:0]		CMFI	CPDL[2:0]		
Component uv offset	29h	CUOFF[3:0]				CVOFF[3:0]			
Component brightness control	2Ah	CBRI[7:0]							
Component contrast control	2Bh	CCON[7:0]							
Component saturation control	2Ch	CSAT[7:0]							
Interrupt mask 1	2Dh	M_VBI	M_HD_HL	M_HD_ RDCAP	0	0	0	M_HD_ COPRO	M_ERROF
Interrupt mask 2	2Eh	M_NFLD	M_HLCK	0	0	0	0	M_DCSTD1	M_DCSTD0
Interrupt mask 3	2Fh	M_INTL	M_HLVLN	M_FIDT	0	M_TYPE3	M_COLSTR	M_COPRO	M_RDCAP

Table 19. Registers 30h to 3Fh used by audio clock generator

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Audio master clock cycles per field	30h	ACPF[7:0]							
Audio master clock cycles per field	31h	ACPF[15:8]							
Audio master clock cycles per field	32h	0	0	0	0	0	0	ACPF[17:16]	
Reserved[1]	33h	0	0	0	0	0	0	0	0
Audio master clock nominal increment	34h	ACNI[7:0]							
Audio master clock nominal increment	35h	ACNI[15:8]							
Audio master clock nominal increment	36h	0	0	ACNI[21:16]					
Reserved[1]	37h	0	0	0	0	0	0	0	0
Clock ratio AMXCLK to ASCLK	38h	0	0	SDIV[5:0]					
Clock ratio ASCLK to ALRCLK	39h	0	0	LRDIV[5:0]					
Audio clock generation basic setup	3Ah	UCGC	0	0	0	APLL	AMVR	LRPH	SCPH
CG1-feedback-divider	3Bh	0	CG1FBD[6:0]						
CG1-clock delete, CG1-output-divider	3Ch	CG1 DIVRES	CG1EN	0	CG1_CKDL[2:0]			CG1OD[1:0]	
CG1-PLL-parameters	3Dh	CG1_R[3:0]				CG1_I[3:0]			
CG1-PLL-parameters	3Eh	0	0	0	CG1_P[4:0]				
PLL1 digital/analog status	3Fh	0	0	0	0	0	CG1LOCK	CG1ACT	0

[1] Do not change these values.

Table 20. Registers 40h to 7Fh used by general purpose VBI data slicer

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
AC1	40h	CHKWSS	HAM_N	FCE	HUNT_N	0	0	0	0
LCR2	41h	LCR02[7:0]							
LCR3	42h	LCR03[7:0]							
to	to	to							
LCR23	56h	LCR23[7:0]							
LCR24	57h	LCR24[7:0]							
FC	58h	FC[7:0]							

Table 20. Registers 40h to 7Fh used by general purpose VBI data slicer *…continued*

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
HOFF	59h	HOFF[7:0]							
VOFF	5Ah	VOFF[7:0]							
HVOFF	5Bh	FOFF	0	VEP	VOFF8	0	HOFF[10:8]		
Reserved[1]	5Ch	0	0	0	0	0	0	0	0
Sliced data output mode	5Dh	SLDOM[7:0]							
Sliced data	5Eh	FC8V[2]	FC7V[2]	SDID[5:0]					
GS2 capture control	5Fh	CDTE[3:0]				0	0	CRNER	CSENA
Line flags	60h	LNFO8	LNFO7	LNFO6	LNFO5	LNFO4	LNFO3	LNFO2	reserved
Line flags	61h	LNFO16	LNFO15	LNFO14	LNFO13	LNFO12	LNFO11	LNFO10	LNFO9
Line flags	62h	LNFO24	LNFO23	LNFO22	LNFO21	LNFO20	LNFO19	LNFO18	LNFO17
Line flags	63 h	LNFE8	LNFE7	LNFE6	LNFE5	LNFE4	LNFE3	LNFE2	reserved
Line flags	64h	LNFE16	LNFE15	LNFE14	LNFE13	LNFE12	LNFE11	LNFE10	LNFE9
Line flags	65h	LNFE24	LNFE23	LNFE22	LNFE21	LNFE20	LNFE19	LNFE18	LNFE17
I²C-bus read-back 1 CC-header	66 h	CCH[7:0]							
I²C-bus read-back 2 CC-odd byte 1	67h	CCO1[7:0]							
I²C-bus read-back 3 CC-odd byte 2	68h	CCO2[7:0]							
I²C-bus read-back 4 CC-even byte 1	69h	CCE1[7:0]							
I²C-bus read-back 5 CC-even byte 2	6Ah	CCE2[7:0]							
I²C-bus read-back 6 WSS-header	6Bh	WSSH[7:0]							
I²C-bus read-back 7 WSS-odd byte 1	6Ch	WSSO1[7:0]							
I²C-bus read-back 8 WSS-odd byte 2	6Dh	WSSO2[7:0]							
I²C-bus read-back 9 WSS-odd byte 3	6Eh	WSSO3[7:0]							
I²C-bus read-back 10 WSS-even byte 1	6Fh	WSSE1[7:0]							
I²C-bus read-back 11 WSS-even byte 2	70h	WSSE2[7:0]							
I²C-bus read-back 12 WSS-even byte 3	71h	WSSE3[7:0]							
I²C-bus read-back 13 GS1-header	72h	GS1H[7:0]							
I²C-bus read-back 14 GS1-odd 1	73h	GS1O1[7:0]							
I²C-bus read-back 15 GS1-odd 2	74h	GS1O2[7:0]							
I²C-bus read-back 16 GS1-even 1	75h	GS1E1[7:0]							
I²C-bus read-back 17 GS1-even 2	76h	GS1E2[7:0]							
I²C-bus read-back 18 GS2-header	77h	GS2H[7:0]							

Table 20. Registers 40h to 7Fh used by general purpose VBI data slicer *…continued*

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
I²C-bus read-back 19 GS2-data byte 1	78h	GS2D1[7:0]							
I²C-bus read-back 20 GS2-data byte 2	79h	GS2D2[7:0]							
I²C-bus read-back 21 GS2-data byte 3	7Ah	GS2D3[7:0]							
I²C-bus read-back 22 GS2-data byte 4	7Bh	GS2D4[7:0]							
Reserved[1]	7Ch to 7Eh	reserved							
I²C-bus read-back 26 GS2-error byte	7Fh	GS2ER[7:0]							

[1] Do not change these values.

[2] Read only.

Table 21. Registers 80h to 8Fh used by task independent global settings 1

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Global control 1	80h	CMOD	0	TEB	TEA	ICKS[3:2]		ICKS[1:0]	
I-port control and definitions	81h	ILLV[1:0]		SWAPO	MAP16	HAM	FTIME	V_EAV[1:0]	
Reserved[1]	82h	0	0	0	0	0	0	0	0
X-port I/O delay and enable control	83h	0	0	XPCK[1:0]		XPE[2]	XRQT	XPE[1:0]	
I-port signal definitions	84h	IDG1[1:0]		IDG0[1:0]		IDV[1:0]		IDH[1:0]	
I-port signal polarities	85h	ISWP[1:0]		0	IG1P	IG0P	IRVP	IRHP	IDQP
I-port FIFO flag control and arbitration	86h	IMPAK	VITX	IDG1[2]	IDG0[2]	FFL[1:0]		FEL[1:0]	
I-port I/O delay and enable control	87h	IPCK[3:2]		IPCK[1:0]		0	0	IPE[1:0]	
Power save control	88h	0	0	SWRST	DPROG	SLM3	0	SLM1	SLM0
Reserved[1]	89h	0	0	0	0	0	0	0	0
Panorama-mode and keystone-mode	8Ah	SHGRD[1:0]		SCAMOD[1:0]		PNLMOD	PANMOD[2:0]		
Keystone control 1 left slope	8Bh	GRAD_STA[7:0]							
Keystone control 2 right slope	8Ch	GRAD_SCA[7:0]							
Reserved[1]	8Dh	0	0	0	0	0	0	0	0
Scaler status 2	8Eh	0	0	FFIL	FFOV	0	LLERR	EEBFULL	EFFULL
Scaler status 1	8Fh	XTRI	ITRI	VBILOS	VBIIRQ	PRDON	ERROF	FIDSCI	FIDSCO

[1] Do not change these values.

Table 22. Registers 90h to BFh used for task A definition

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Basic settings and acquisition window definition									
Task handling control	90h	CONLH	OFIDC	FSKP[2:0]			RPTSK	STRC[1:0]	
X-port formats and configuration	91h	CONLV	HLDFV	SCSRC[1:0]		SCRQE	FSC[2:1]		FSC[0]
X-port Input reference signal definition	92h	XFDV	XFDH	XDV[1:0]		XCODE	XDH	XDQ	XCKS
I-port formats and configuration	93h	ICODE	INS80	FYSK	FOI[1:0]		FSI[2:0]		
Horizontal input window start	94h	XO[7:0]							
	95h	0	0	0	0	XO[11:8]			
Horizontal input window length	96h	XS[7:0]							
	97h	0	0	0	0	XS[11:8]			
Vertical input window start	98h	YO[7:0]							
	99h	0	0	0	0	YO[11:8]			
Vertical input window length	9Ah	YS[7:0]							
	9Bh	FMOD	0	0	0	YS[11:8]			
Horizontal output window length	9Ch	XD[7:0]							
	9Dh	0	0	0	0	XD[11:8]			
Vertical output window length	9Eh	YD[7:0]							
	9Fh	0	0	0	0	YD[11:8]			
FIR filtering and prescaling									
Horizontal prescaling	A0h	0	0	XPSC[5:0]					
Accumulation length	A1h	0	0	XACL[5:0]					
Prescaler DC gain and FIR prefilter control	A2h	PFUV[1:0]		PFY[1:0]		XC2_1	XDCG[2:0]		
Reserved[1]	A3h	0	0	0	0	0	0	0	0
Luminance brightness	A4h	BRIG[7:0]							
Luminance contrast	A5h	CONT[7:0]							
Chrominance saturation	A6h	SATN[7:0]							
Reserved[1]	A7h	0	0	0	0	0	0	0	0
Horizontal phase scaling									
Horizontal scaling increment luminance	A8h	XSCY[7:0]							
	A9h	0	0	0	XSCY[12:8]				

Table 22. Registers 90h to BFh used for task A definition *…continued*

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Horizontal phase offset luminance	AAh	XPHY[7:0]							
Reserved[1]	ABh	0	0	0	0	0	0	0	0
Horizontal scaling increment chrominance	ACh	XSCC[7:0]							
	ADh	0	0	0	XSCC[12:8]				
Horizontal phase offset chrominance	AEh	XPHC[7:0]							
Reserved[1]	AFh	0	0	0	0	0	0	0	0
Vertical scaling									
Vertical Scaling Increment	B0h	YSCV[7:0]							
	B1h	YSCV[15:8]							
Edge-guided vertical interpolation scaling increment	B2h	YSCE[7:0]							
	B3h	YSCE[15:8]							
Edge-guided vertical interpolation, vertical scaling mode control	B4h	EDON	EDBYP	0	YMIR	0	0	0	YMODE
Scaler post processing control	B5h	0	0	DICON[1:0]		0	MACON	GACON	CSCON
Luminance improvement control	B6h	LIMOD[1:0]		LIFIL[2]	LIFIL[1:0]		LIWGT[2:0]		
Chrominance improvement control	B7h	CIMOD[1:0]		CIFIL[2]	CIFIL[1:0]		CIWGT[2:0]		
Vertical scaling phase offset 0	B8h	YPV0[7:0]							
Vertical scaling phase offset 1	B9h	YPV1[7:0]							
Vertical scaling phase offset 2	BAh	YPV2[7:0]							
Vertical scaling phase offset 3	BBh	YPV3[7:0]							
Edge-guided vertical interpolation scaling phase offset 0	BCh	YPE0[7:0]							
Edge-guided vertical interpolation scaling phase offset 1	BDh	YPE1[7:0]							
Edge-guided vertical interpolation scaling phase offset 2	BEh	YPE2[7:0]							
Edge-guided vertical interpolation scaling phase offset 3	BFh	YPE3[7:0]							

[1] Do not change these values.

Table 23. Registers C0h to EFh used for task B definition

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Basic settings and acquisition window definition									
Task handling control	C0h	CONLH	OFIDC	FSKP[2:0]			RPTSK	STRC[1:0]	
X-port formats and configuration	C1h	CONLV	HLDFV	SCSRC[1:0]		SCRQE	FSC[2:1]		FSC[0]
Input reference signal definition control	C2h	XFDV	XFDH	XDV[1:0]		XCODE	XDH	XDQ	XCKS
I-port formats and configuration	C3h	ICODE	INS80	FYSK	FOI[1:0]		FSI[2:0]		
Horizontal input window start	C4h	XO[7:0]							
	C5h	0	0	0	0	XO[11:8]			
Horizontal input window length	C6h	XS[7:0]							
	C7h	0	0	0	0	XS[11:8]			
Vertical input window start	C8h	YO[7:0]							
	C9h	0	0	0	0	YO[11:8]			
Vertical input window length	CAh	YS[7:0]							
	CBh	FMOD	0	0	0	YS[11:8]			
Horizontal output window length	CCh	XD[7:0]							
	CDh	0	0	0	0	XD[11:8]			
Vertical output window length	CEh	YD[7:0]							
	CFh	0	0	0	0	YD[11:8]			
FIR filtering and prescaling									
Horizontal prescaling	D0h	0	0	XPSC[5:0]					
Accumulation length	D1h	0	0	XACL[5:0]					
Prescaler DC gain and FIR prefilter control	D2h	PFUV[1:0]		PFY[1:0]		XC2_1	XDCG[2:0]		
Reserved[1]	D3h	0	0	0	0	0	0	0	0
Luminance brightness	D4h	BRIG[7:0]							
Luminance contrast	D5h	CONT[7:0]							
Chrominance saturation	D6h	SATN[7:0]							
Reserved[1]	D7h	0	0	0	0	0	0	0	0
Horizontal phase scaling									
Horizontal scaling increment luminance	D8h	XSCY[7:0]							
	D9h	0	0	0	XSCY[12:8]				

Table 23. Registers C0h to EFh used for task B definition *…continued*

Basic register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Horizontal phase offset luminance	DAh	XPHY[7:0]							
Reserved[1]	DBh	0	0	0	0	0	0	0	0
Horizontal scaling increment chrominance	DCh	XSCC[7:0]							
	DDh	0	0	0	XSCC[12:8]				
Horizontal phase offset chrominance	DEh	XPHC[7:0]							
Reserved[1]	DFh	0	0	0	0	0	0	0	0
Vertical scaling									
Vertical scaling increment	E0h	YSCV[7:0]							
	E1h	YSCV[15:8]							
Edge-guided vertical interpolation scaling increment	E2h	YSCE[7:0]							
	E3h	YSCE[15:8]							
Edge-guided vertical interpolation, vertical scaling mode control	E4h	EDON	EDBYP	0	YMIR	0	0	0	YMODE
Scaler post processing control	E5h	0	0	DICON[1:0]		0	MACON	GACON	CSCON
Luminance improvement control	E6h	LIMOD[1:0]		LIFIL[2]	LIFIL[1:0]		LIWGT[2:0]		
Chrominance improvement control	E7h	CIMOD[1:0]		CIFIL[2]	CIFIL[1:0]		CIWGT[2:0]		
Vertical scaling phase offset 0	E8h	YPV0[7:0]							
Vertical scaling phase offset 1	E9h	YPV1[7:0]							
Vertical scaling phase offset 2	EAh	YPV2[7:0]							
Vertical scaling phase offset 3	EBh	YPV3[7:0]							
Edge-guided vertical interpolation scaling phase offset 0	ECh	YPE0[7:0]							
Edge-guided vertical interpolation scaling phase offset 1	EDh	YPE1[7:0]							
Edge-guided vertical interpolation scaling phase offset 2	EEh	YPE2[7:0]							
Edge-guided vertical interpolation scaling phase offset 3	EFh	YPE3[7:0]							
Reserved[1]	F0h to FFh	0	0	0	0	0	0	0	0

[1] Do not change these values.

7.15.2 Register overview extended functions

Access the registers from Table 24 through the slave write address 4Ah/48h.

Table 24. I²C-bus extended functions overview

Address	Extended register function	Reference
00h to 1Fh	HDTV synchronization	Table 25
20h to 3Fh	Analog Input Control (AIC) expert mode and extended analog input/output functions	Table 26
40h to 4Fh	Analog Input Control (AIC) expert mode status (read only)	Table 27
50h to 59h	color improvement (gravity functions)	Table 28
60h to 78h	OSD	Table 29
80h to 8Bh	edge-guided interpolation	Table 30
8Ch to BFh	scaler post processing look-up tables	Table 31
C0h to CFh	histogram collection	Table 32
D0h to DFh	histogram status	Table 33
E0h to FFh	second PLL/CG (PLL2/CG2) and raster	Table 34

Table 25. Register 00h to 1Fh used by HDTV-synchronization

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Reserved[1]	00h	0	0	0	0	0	0	0	0
Reserved[1]	01h	0	0	0	0	0	0	0	0
MSB horizontal reference stop/start	02h	0	0	HD_HRFF[9:8]		0	0	HD_HRFR[9:8]	
Horizontal reference stop	03h	HD_HRFF[7:0]							
Horizontal reference start	04h	HD_HRFR[7:0]							
MSB horizontal sync start/stop	05h	0	0	HD_HSB[9:8]		0	0	HD_HSS[9:8]	
Horizontal sync start	06h	HD_HSB[7:0]							
Horizontal sync stop	07h	HD_HSS[7:0]							
Sync control	08h	HD_AUFD	HD_FSEL	HD_FOET	HD_HTC[1:0]		HD_HPLL	HD_VNOI[1:0]	
HD_mode	09h	0	0	SEL_ATSC[1:0]		0	SEL_VEXT	SEL_3L	SEL_HD
Reserved[1]	0Ah to 14h	0	0	0	0	0	0	0	0
VGATE start	15h	HD_VSTA[7:0]							
VGATE stop	16h	HD_VSTO[7:0]							
MISC/VGATE MSBs	17h	0	0	HD_VSTO[9:8]		0	HD_VGPS	HD_VSTA[9:8]	
Reserved[1]	18h to 1Dh	0	0	0	0	0	0	0	0
Status byte HD 1[2]	1Eh	HOR_M[1:0]		VER_M[2:0]			reserved		
Status byte HD 2[2]	1Fh	reserved	HD_HL	HD_FIDT	reserved			HD_COPRO	HD_RDCAP[3]

[1] Do not change these values.

[2] Read only.

[3] HL and VL.

Table 26. Registers 20h to 3Fh used by Analog Input Control (AIC) expert mode and extended analog input/output functions

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Bias current analog front-end buffers	20h	CUR4_PREMUX[1:0]		CUR3_PREMUX[1:0]		CUR2_PREMUX[1:0]		CUR1_PREMUX[1:0]	
Target values analog clamping 1	21h	F_ANA1_CL[7:0]							
Target values analog clamping 1, 2	22h	F_ANA2_CL[5:0]						F_ANA1_CL[9:8]	
Target values analog clamping 2, 3	23h	F_ANA3_CL[3:0]				F_ANA2_CL[9:6]			
Target values analog clamping 3, clamp mode, dither disable	24h	DITH_DIS	CLMP_BLCK	F_ANA3_CL[9:4]					
Target values digital clamping 1	25h	F_DIG1_CL[7:0]							

Table 26. Registers 20h to 3Fh used by Analog Input Control (AIC) expert mode and extended analog input/output functions *…continued*

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Target values digital clamping 1, 2	26h	F_DIG2_CL[5:0]						F_DIG1_CL[9:8]	
Target values digital clamping 2, 3	27h	F_DIG3_CL[3:0]				F_DIG2_CL[9:6]			
Target values digital clamping 3, 4	28h	F_DIG4_CL[1:0]		F_DIG3_CL[9:4]					
Target values digital clamping 4	29h	F_DIG4_CL[9:2]							
Target values digital gain	2Ah	GAIN_TARG[7:0]							
Target values digital gain, range parameter analog gain control	2Bh	RANGE_LIM[5:0]						GAIN_TARG[9:8]	
Range parameter analog gain control, analog gain limit, clamp test active	2Ch	T_FIX_CLAA	AGAIN_LIM[2:0]			RANGE_LIM[9:6]			
Capture gating window control, clamp test fast	2Dh	T_FIX_CLAF	SY_TOFFSET[6:0]						
Capture gating window control, clamp test up	2Eh	T_FIX_CLAU	SY_WIDTH[6:0]						
Capture gating window control	2Fh	0	BLACK_DIST[6:0]						
Capture gating window control, analog clamp active	30h	A_CL_ACT	BLACK_WIDTH[6:0]						
Clamp inhibit gate (for Macrovision) beginning, end of field	31h	F_END_MSK[3:0]				VBI_MSK[3:0]			
Bias current for ADCs	32h	ADCSM4_PREMUX[1:0]		ADCSM3_PREMUX[1:0]		ADCSM2_PREMUX[1:0]		ADCSM1_PREMUX[1:0]	
Line selector for maximum value capturing	33h	LINESEL[7:0]							
Line selector for maximum value capturing, input channel selector for maximum value capturing	34h	CHROMA_OBS_MUX	DBG_OBS[1:0]		0	AAGC_ACC	ADC_OBS[1:0]		LINESEL[8]
Reserved[1]	35h to 3Ah	0	0	0	0	0	0	0	0
V_{ref} settings, bias current select analog out 1 and 2	3Bh	PDIS	PRATIO[4:0]					AOSC[1:0]	
Analog output select 2	3Ch	0	0	AOSL2B[1:0]		AOSL2A[1:0]		AOSL2[1:0]	
Reference select	3Dh	REFS4[1:0]		REFS3[1:0]		REFS2[1:0]		REFS1[1:0]	
Input signal detection ADCs disable	3Eh	0	0	0	0	0	ADISD[2:0]		
Input signal detection ADCs selection	3Fh	0	ISDMUX3[1:0]		ISDMUX2[1:0]		ISDMUX1[2:0]		

[1] Do not change these values.

Table 27. Registers 40h to 4Fh used by Analog Input Control (AIC) expert mode status (read only)

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Unused lower range of previous field	40h	FLD_LOWER_GAP[7:0]							
Unused lower range of previous field, Unused upper range of previous field	41h	FLD_UPPER_GAP[5:0]						FLD_LOWER_GAP[9:8]	
Flags	42h	reserved		LUM_UNDERRANGE	LUM_OVERRANGE	FLD_UPPER_GAP[9:6]			
Line selector for maximum value capturing result	43h	LNSL_UPPER_GAP[7:0]							
Line selector for maximum value capturing result, sync level	44h	SYNC_LVL[5:0]						LNSL_UPPER_GAP[9:8]	
Sync level	45h	reserved				SYNC_LVL[9:6]			
Sync amplitude	46h	SYNC_AMP[7:0]							
Black level, sync amplitude	47h	BLACK_LVL[5:0]						SYNC_AMP[9:8]	
Black level, burst amplitude	48h	BURST_AMP[3:0]				BLACK_LVL[9:6]			
Burst amplitude, digital clamp value	49h	FINE_CLMP[1:0]		BURST_AMP[9:4]					
Digital clamp value	4Ah	FINE_CLMP[9:2]							
Digital gain value	4Bh	FINE_GAIN[7:0]							
Digital gain value, gain correction value	4Ch	WIPA_CORR[4:0]					FINE_GAIN[10:8]		
Gain correction value	4Dh	reserved		WIPA_CORR[10:5]					
Noise on horizontal sync, DC-values on input detection ADCs Input Source Detection ISD1 and ISD2	4Eh	HNOISE	reserved	DCS2[2:0]			DCS1[2:0]		
Level on FSW / L4 -input DC-values on input detection ADC ISD3	4Fh	DCS4	reserved				DCS3[2:0]		

Table 28. Registers 50h to 59h used by color improvement (gravity functions)

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Gravity 11	50h	GR_EN1	0	GR_UV_FORCE1[1:0]		0	GR_UV_RANGE1[2:0]		
Gravity 12	51h	GR_U_CENTER1[7:0]							
Gravity 13	52h	GR_V_CENTER1[7:0]							
Gravity 21	53h	GR_EN2	0	GR_UV_FORCE2[1:0]		0	GR_UV_RANGE2[2:0]		
Gravity 22	54h	GR_U_CENTER2[7:0]							
Gravity 23	55h	GR_V_CENTER2[7:0]							
Gravity 31	56h	GR_EN3	0	GR_UV_FORCE3[1:0]		0	GR_UV_RANGE3[2:0]		

Table 28. Registers 50h to 59h used by color improvement (gravity functions) *…continued*

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Gravity 32	57h	GR_U_CENTER3[7:0]							
Gravity 33	58h	GR_V_CENTER3[7:0]							
Gravity 4	59h	GR_EN4	GR_VSHIFT[1:0]		GR_UV_FORCE4[1:0]		GR_UV_RANGE4[2:0]		
Reserved[1]	5Ah to 5Fh	0	0	0	0	0	0	0	0

[1] Do not change these values.

Table 29. Registers 60h to 78h used by OSD

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Digital OSD									
OSD RGB look-up table 0	60h	OS_LT0[7:0]							
	61h	OS_LT0[15:8]							
OSD RGB look-up table 1	62h	OS_LT1[7:0]							
	63h	OS_LT1[15:8]							
OSD RGB look-up table 2	64h	OS_LT2[7:0]							
	65h	OS_LT2[15:8]							
OSD RGB look-up table 3	66h	OS_LT3[7:0]							
	67h	OS_LT3[15:8]							
OSD RGB look-up table 4	68h	OS_LT4[7:0]							
	69h	OS_LT4[15:8]							
OSD RGB look-up table 5	6Ah	OS_LT5[7:0]							
	6Bh	OS_LT5[15:8]							
OSD RGB look-up table 6	6Ch	OS_LT6[7:0]							
	6Dh	OS_LT6[15:8]							
OSD RGB look-up table 7	6Eh	OS_LT7[7:0]							
	6Fh	OS_LT7[15:8]							
OSD RGB look-up table 8	70h	OS_LT8[7:0]							
	71h	OS_LT8[15:8]							
OSD_control	72h	OS_MD[2:0]			OS_INV	BSCR	0	0	OS_OD_F
Analog OSD									
Fast switch status OSD	73h	0	0	FSWSO[5:0]					
FSW OSD control 1	74h	0	0	0	0	FSRNDO	FSSHFTO[2:0]		

Table 29. Registers 60h to 78h used by OSD *…continued*

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
FSW OSD control 2	75h	FSLENO[1:0]		0	FSOFFSO[4:0]				
FSW OSD control 3	76h	0	FSWIO	1	FSDELO[4:0]				
Overlay OSD control	77h	0	0	0	0	OSDEN	OVMODO[2:0]		
Comp. OSD dither, peaking, delay	78h	0	0	CDITHO[1:0]		CMFIO	CPDLO[2:0]		
Reserved[1]	79h to 7Fh	0	0	0	0	0	0	0	0

[1] Do not change these values.

Table 30. Registers 80h to 8Bh used by edge-guided interpolation

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Edge-guided vertical interpolation threshold 1	80h	0	EDTHR1[6:0]						
Edge-guided vertical interpolation threshold 2	81h	EDTHR2[7:0]							
Edge-guided vertical interpolation threshold 3	82h	EDTHR3[7:0]							
Edge-guided vertical interpolation threshold 2, 3, 4	83h	0	EDTHR4[2:0]			0	0	EDTHR3[8]	EDTHR2[8]
Edge-guided vertical interpolation threshold 5, 6	84h	0	EDTHR6[2:0]			0	EDTHR5[2:0]		
Reserved[1]	85h	0	0	0	0	0	0	0	0
Edge-guided vertical interpolation function	86h	0	0	0	EDFUN[4:0]				
Edge-guided vertical interpolation function 1	87h	0	0	0	0	0	0	EDFAEE[1:0]	
Reserved[1]	88h to 8Bh	0	0	0	0	0	0	0	0

[1] Do not change these values.

Table 31. Registers 8Ch to BFh used by scaler post processing look-up tables

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Start point green path	8Ch	P0GST[7:0]							
Start point blue path	8Dh	P1GST[7:0]							
Start point red path	8Eh	P2GST[7:0]							

Table 31. Registers 8Ch to BFh used by scaler post processing look-up tables *…continued*

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Reserved[1]	8Fh	0	0	0	0	0	0	0	0
Green path	90h	P0GA0[7:0]							
	91h	P0GA1[7:0]							
	92h	P0GA2[7:0]							
	to	to							
	9Dh	P0GAD[7:0]							
	9Eh	P0GAE[7:0]							
	9Fh	P0GAF[7:0]							
Blue path	A0h	P1GA0[7:0]							
	A1h	P1GA1[7:0]							
	A2h	P1GA2[7:0]							
	to	to							
	ADh	P1GAD[7:0]							
	AEh	P1GAE[7:0]							
	AFh	P1GAF[7:0]							
Red path	B0h	P2GA0[7:0]							
	B1h	P2GA1[7:0]							
	B2h	P2GA2[7:0]							
	to	to							
	BDh	P2GAD[7:0]							
	BEh	P2GAE[7:0]							
	BFh	P2GAF[7:0]							

[1] Do not change these values.

Table 32. Registers C0h to CFh used by histogram collection

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Histogram control 0	C0h	HISTEN/ REPV	HISTP[2:0]			HISCON	HISCP[2:0]		
Reserved[1]	C1h	0	0	0	0	0	0	0	0
Histogram control 2	C2h	0	HSFP[10:8]			0	HSTP[10:8]		
Histogram control 3	C3h	HSFP[7:0]							

Table 32. Registers C0h to CFh used by histogram collection *…continued*

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Histogram control 4	C4h	HSTP[7:0]							
Histogram control 5	C5h	HSFF	HSFL[10:8]			0	HSTL[10:8]		
Histogram control 6	C6h	HSFL[7:0]							
Histogram control 7	C7h	HSTL[7:0]							
Reserved[1]	C8h to CFh	0	0	0	0	0	0	0	0

[1] Do not change these values.

Table 33. Registers D0h to DFh used by histogram status

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
Result bin 0	D0h	HSB0[7:0]							
Result bin 1	D1h	HSB1[7:0]							
Result bin 2	D2h	HSB2[7:0]							
Result bin 3	D3h	HSB3[7:0]							
Result bin 4	D4h	HSB4[7:0]							
Result bin 5	D5h	HSB5[7:0]							
Result bin 6	D6h	HSB6[7:0]							
Result bin 7	D7h	HSB7[7:0]							
Result bin 8	D8h	HSB8[7:0]							
Result bin 9	D9h	HSB9[7:0]							
Result bin 10	DAh	HSBA[7:0]							
Result bin 11	DBh	HSBB[7:0]							
Result bin 12	DCh	HSBC[7:0]							
Result bin 13	DDh	HSBD[7:0]							
Result bin 14	DEh	HSBE[7:0]							
Result bin 15	DFh	HSBF[7:0]							

Table 34. Registers E0h to FFh used by second PLL/CG (PLL2/CG2) and raster generator

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
LFCOs per line	E0h	SPLPL[7:0]							
P-/I-parameter select, PLL mode, PLL H-Source, LFCOs per line	E1h	SPPI[3:0]				SPMOD[1:0]		SPLPL[9:8]	
Nominal PLL2 DTO increment	E2h	SPNINC[7:0]							
	E3h	SPNINC[15:8]							
S_PLL maximum phase error threshold, PLL2 number of lines threshold	E4h	SPTHRL[3:0]				SPTHRM[3:0]			
CG2-feedback-divider	E5h	SPBYPNS	CG2FBD[6:0]						
CG2-clock delete, CG2-output-divider	E6h	CG2DIVRES	CG2EN	SPHSEL	CG2_CKDL[2:0]			CG2OD[1:0]	
CG2-PLL-parameters	E7h	CG2_R[3:0]				CG2_I[3:0]			
CG2-PLL-parameters	E8h	0	0	0	CG2_P[4:0]				
PLL2 digital/analog status	E9h	0	0	0	0	0	CG2LOCK	CG2ACT	SPLOCK
Raster generation-reference select, raster generation reset	EAh	PGRES[1:0]		PGRSEL	PGVED	0	0	0	0
Pulse generation line length	EBh	PGLLEN[7:0]							
HPulse A position, pulse generation line length	ECh	PGHAPS[3:0]				PGLLEN[11:8]			
HPulse A position	EDh	PGHAPS[11:4]							
HPulse B position	EEh	PGHBPS[7:0]							
HPulse B/C position	EFh	PGHCPS[3:0]				PGHBPS[11:8]			
HPulse C position	F0h	PGHCPS[11:4]							
HGate begin	F1h	PGHGB[7:0]							
HGate begin/stop	F2h	PGHGS[3:0]				PGHGB[11:8]			
HGate stop	F3h	PGHGS[11:4]							
Horizontal raster load	F4h	PGHRL[7:0]							
Horizontal/vertical raster load	F5h	PGVRL[3:0]				PGHRL[11:8]			
Vertical raster load	F6h	PGVRL[11:4]							
Pulse generator field length	F7h	PGFLEN[7:0]							
VPulse A position, pulse generator field length	F8h	PGVAPS[3:0]				PGFLEN[11:8]			
VPulse A position	F9h	PGVAPS[11:4]							

Table 34. Registers E0h to FFh used by second PLL/CG (PLL2/CG2) and raster generator *…continued*

Extended register function	Subaddress	D7	D6	D5	D4	D3	D2	D1	D0
HActive begin	FAh	PGHACB[7:0]							
HActive begin/stop	FBh	PGHACS[3:0]				PGHACB[11:8]			
HActive stop	FCh	PGHACS[11:4]							
VGate begin	FDh	PGVGB[7:0]							
VGate begin/stop	FEh	PGVGS[3:0]				PGVGB[11:8]			
VGate stop	FFh	PGVGS[11:4]							

8. Limiting values

Table 35. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Analog supply voltage						
V_{DDA1}	analog supply voltage 1			–0.5	+4.2	V
V_{DDA1A}	analog supply voltage 1A			–0.5	+4.2	V
V_{DDA2}	analog supply voltage 2			–0.5	+4.2	V
V_{DDA2A}	analog supply voltage 2A			–0.5	+4.2	V
V_{DDA3}	analog supply voltage 3			–0.5	+4.2	V
V_{DDA3A}	analog supply voltage 3A			–0.5	+4.2	V
V_{DDA4}	analog supply voltage 4			–0.5	+4.2	V
V_{DDA4A}	analog supply voltage 4A			–0.5	+4.2	V
$V_{DDA(XTAL)}$	crystal analog supply voltage			–0.5	+2.5	V
V_{DDA_A18}	analog supply voltage (1.8 V)			–0.5	+2.5	V
V_{DDA_C18}	analog supply voltage (1.8 V)			–0.5	+2.5	V
Core supply voltage, 1.8 V						
V_{DDD2}	digital supply voltage 2			–0.5	+2.5	V
V_{DDD4}	digital supply voltage 4			–0.5	+2.5	V
V_{DDD7}	digital supply voltage 7			–0.5	+2.5	V
V_{DDD8}	digital supply voltage 8			–0.5	+2.5	V
V_{DDD10}	digital supply voltage 10			–0.5	+2.5	V
V_{DDD12}	digital supply voltage 12			–0.5	+2.5	V
Peripheral cell supply voltage						
V_{DDD1}	digital supply voltage 1			–0.5	+4.2	V
V_{DDD3}	digital supply voltage 3			–0.5	+4.2	V
V_{DDD5}	digital supply voltage 5			–0.5	+4.2	V
V_{DDD6}	digital supply voltage 6			–0.5	+4.2	V
V_{DDD9}	digital supply voltage 9			–0.5	+4.2	V
V_{DDD11}	digital supply voltage 11			–0.5	+4.2	V
V_{DDD13}	digital supply voltage 13			–0.5	+4.2	V
Generic						
V_I	input voltage	analog and digital inputs	[1]	–0.5	V_{DD} + 0.5	V
ΔV_{SS}	ground supply voltage difference	between V_{SSAn} and V_{SSDn}		-	100	mV
T_{stg}	storage temperature			–40	+125	°C
T_{amb}	ambient temperature			0	70	°C

Table 35. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{esd}	electrostatic discharge voltage	human body model	[2]	-	±2000	V
		machine model	[3]	-	±200	V
I_{lu}	latch-up current	keep all supply voltages below the maximum values listed in this table	[4]	-	±100	mA

[1] Maximum value is 4.2 V.

[2] Class 2 according to *JEDEC JESD22-A114*.

[3] Class B according to *JEDEC JESD22-A115*.

[4] According to *NXP General Quality Specification SNW-FQ-611* in compliance with *NXP Latch-up Specification SNW-FQ-303*.

9. Thermal characteristics

Table 36. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]		
	SAA7154E/V2/G			38	K/W
	SAA7154H/V2			35	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample copper area direct under the SAA7154E; SAA7154H with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

10. Characteristics

Operating conditions for maximum and minimum values in Table 37 to Table 42: peripheral V_{DDD} = 3.0 V to 3.6 V; core V_{DDD} = 1.65 V to 1.95 V; peripheral V_{DDA} = 3.1 V to 3.5 V; core V_{DDA} = 1.65 V to 1.95 V; T_{amb} = 25 °C; timings and levels refer to drawings and conditions illustrated in Figure 17 to Figure 19; unless otherwise specified.

Table 37. Supplies

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog supply voltage						
V_{DDA0}	analog supply voltage 0		3.1	3.3	3.5	V
V_{DDA1}	analog supply voltage 1		3.1	3.3	3.5	V
V_{DDA1A}	analog supply voltage 1A		3.1	3.3	3.5	V
V_{DDA2}	analog supply voltage 2		3.1	3.3	3.5	V
V_{DDA2A}	analog supply voltage 2A		3.1	3.3	3.5	V
V_{DDA3}	analog supply voltage 3		3.1	3.3	3.5	V
V_{DDA3A}	analog supply voltage 3A		3.1	3.3	3.5	V
V_{DDA4}	analog supply voltage 4		3.1	3.3	3.5	V
V_{DDA4A}	analog supply voltage 4A		3.1	3.3	3.5	V

Table 37. Supplies *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA(XTAL)}$	crystal analog supply voltage		1.65	1.8	1.95	V
V_{DDA_A18}	analog supply voltage (1.8 V)		1.65	1.8	1.95	V
V_{DDA_C18}	analog supply voltage (1.8 V)		1.65	1.8	1.95	V
Digital core supply voltage						
V_{DDD2}	digital supply voltage 2		1.65	1.8	1.95	V
V_{DDD4}	digital supply voltage 4		1.65	1.8	1.95	V
V_{DDD7}	digital supply voltage 7		1.65	1.8	1.95	V
V_{DDD8}	digital supply voltage 8		1.65	1.8	1.95	V
V_{DDD10}	digital supply voltage 10		1.65	1.8	1.95	V
V_{DDD12}	digital supply voltage 12		1.65	1.8	1.95	V
Peripheral digital cell supply voltage						
V_{DDD1}	digital supply voltage 1		3.0	3.3	3.6	V
V_{DDD3}	digital supply voltage 3		3.0	3.3	3.6	V
V_{DDD5}	digital supply voltage 5		3.0	3.3	3.6	V
V_{DDD6}	digital supply voltage 6		3.0	3.3	3.6	V
V_{DDD9}	digital supply voltage 9		3.0	3.3	3.6	V
V_{DDD11}	digital supply voltage 11		3.0	3.3	3.6	V
V_{DDD13}	digital supply voltage 13		3.0	3.3	3.6	V
Power dissipation						
P_{tot}	total power dissipation	analog plus digital part				
		Power-down mode	-	-	15	mW
		CVBS mode	-	490	550	mW
		Y/C mode	-	710	780	mW
		Component mode	-	880	960	mW
		HD component mode	-	1290	1440	mW
		digital part				
		CVBS and Y/C mode	-	200	240	mW
		Component mode	-	210	250	mW
		HD component mode	-	290	340	mW
		analog part				
		CVBS and Y/C mode	-	290	310	mW
		Y/C mode	-	510	540	mW
		Component mode	-	670	710	mW
		HD component mode	-	1000	1100	mW

Table 38. Analog part

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog part						
I_{CL}	clamping current	V_I = 1 V (DC)	-	±4	-	µA
$V_{i(p-p)}$	peak-to-peak input voltage	on pins AIxx; for nominal video levels 1 V (p-p); –4 dB termination 27 Ω/47 Ω and AC coupling with 22 nF required	-	0.64	-	V

Table 38. Analog part *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\|Z_i\|$	input impedance	clamping current off	200	-	-	kΩ
C_i	input capacitance		-	-	10	pF
$\alpha_{ct(ch)}$	channel crosstalk	f_i < 10 MHz	-	-	–50	dB
$V_{o(p-p)}$	peak-to-peak output voltage	on pin AOUT1 or AOUT2; for normal video levels 1 V (p-p), 75 Ω termination	-	1	-	V
B	bandwidth	on pin AOUT1 or AOUT2; 75 Ω/20 pF termination at –1 dB	-	10	-	MHz
10-bit ADC (including analog clamp and gain stages)						
B	bandwidth	at –1 dB	-	30	-	MHz
φ_{dif}	differential phase		-	2	-	deg
G_{dif}	differential gain		-	2	-	%
f_{clk}	clock frequency		-	-	58.6	MHz
$V_{i(range)}$	input voltage range		0.4	-	1.6	V
DLE_{DC}	DC differential linearity error		-	-	3	LSB
ILE_{DC}	DC integral linearity error		-	-	4	LSB
$M_{G(CTC)}$	channel-to-channel gain matching		-	3	6	%
3-bit ADC (FSW, AV-detect and OSD; see Section 11.3)						
f_{clk}	clock frequency		-	-	58.6	MHz
$V_{i(range)}$	input voltage range		0	-	1.304	V

Table 39. Digital inputs and outputs

Attention: *Digital inputs and I/O ports are not 5 V tolerant.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital inputs (all pins with type I in Table 4)						
V_{IL}	LOW-level input voltage	pin XTALI	–0.5	-	$+0.2 \times V_{DDA(XTAL)}$	V
		other inputs	–0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage	pin XTALI	$0.8 \times V_{DDA(XTAL)}$	-	1.95	V
		other inputs	2.0	-	3.6	V
I_{LI}	input leakage current		-	-	1	µA
$I_{L(I/O)}$	leakage current (I/O)		-	-	10	µA
C_i	input capacitance	I/O at high-impedance	-	-	8	pF
Digital outputs (all pins with type O in Table 4)[1]						
V_{OL}	LOW-level output voltage	pin SDA at 3 mA sink current	-	-	0.4	V
		for clocks	-	-	0.4	V
		other digital outputs	-	-	0.4	V
V_{OH}	HIGH-level output voltage	for clocks	$V_{DDD} - 0.4$	-	-	V
		other digital outputs	$V_{DDD} - 0.4$	-	-	V

[1] The levels must be measured with load circuits: R_L = 1.2 kΩ at 3 V (TTL load) and C_L = 50 pF.

Table 40. Clocks and oscillators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock output timing (pins LLC and LLC2_54)[1]						
$C_{o(L)}$	output load capacitance		15	-	50	pF
T_{cy}	cycle time	pin LLC	35	-	39	ns
		pin LLC2_54	17.5	-	78	ns
δ	duty cycle	for t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}; C_L = 40 pF	40	-	60	%
t_r	rise time	pins LLC and LLC2_54; 0.2 V to V_{DDD} − 0.2 V	-	-	5	ns
t_f	fall time	pins LLC and LLC2_54; V_{DDD} − 0.2 V to 0.2 V	-	-	5	ns
$t_{d(LLC-LLC2\_54)}$	delay time from LLC to LLC2_54	measured at 1.5 V; C_L = 25 pF	−4	-	+8	ns
Horizontal PLL						
$f_{nom(line)}$	nominal line frequency	50 Hz field/625 lines	-	15625	-	Hz
		60 Hz field/525 lines	-	15734	-	Hz
$\Delta f_{hl}/f_{hl(nom)}$	horizontal line frequency deviation		-	-	5.7	%
Subcarrier PLL						
$f_{nom(subc)}$	nominal subcarrier frequency	PAL BGHI, PAL44-60, NTSC44-60	-	4433619	-	Hz
		NTSC M/J	-	3579545	-	Hz
		PAL M	-	3575612	-	Hz
		PAL N	-	3582056	-	Hz
$\Delta f_{lock-in}$	lock-in frequency range		±400	-	-	Hz
Crystal oscillator for 32.11 MHz[2]						
General						
f_{nom}	nominal frequency	3rd harmonic	-	32.11	-	MHz
Δf_{nom}	nominal frequency deviation		-	-	±30	ppm
$\Delta f_{nom(T)}$	nominal frequency deviation with temperature		-	-	±30	ppm
Crystal specification (X1)						
T_{amb}	ambient temperature		0	-	70	°C
C_L	load capacitance		8	-	-	pF
$R_{s(rsn)}$	resonant series resistor		-	40	80	Ω
C_1	motional capacitance		1.2	1.5	1.8	fF
C_0	shunt capacitance		3.5	4.3	5.1	pF
Crystal oscillator for 24.576 MHz[2]						
General						
f_{nom}	nominal frequency	3rd harmonic	-	24.576	-	MHz
Δf_{nom}	nominal frequency deviation		-	-	±50	ppm
$\Delta f_{nom(T)}$	nominal frequency deviation with temperature		-	-	±20	ppm

Table 40. Clocks and oscillators *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal specification (X1)						
T_{amb}	ambient temperature		0	-	70	°C
C_L	load capacitance		8	-	-	pF
$R_{s(rsn)}$	resonant series resistor		-	40	80	Ω
C_1	motional capacitance		1.2	1.5	1.8	fF
C_0	shunt capacitance		2.8	3.5	4.2	pF

[1] The effects of rise and fall times are included in the calculation of $t_{h(Q)}$ and t_{PD}. Timings and levels refer to drawings and conditions illustrated in Figure 17.

[2] The crystal oscillator drive level is typical 0.28 mW.

Table 41. X-port

Attention: *Digital inputs and I/O ports are not 5 V tolerant.*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{o(L)}$	output load capacitance			15	-	30	pF
Clock input and output timing (pin XCLK); see Figure 18							
T_{cy}	cycle time	as input		31	-	45	ns
		as output		35	-	39	ns
δ	duty cycle	for t_{LLCH}/t_{LLC}; XCLK as input	[1]	40	50	60	%
		for t_{XCLKH}/T_{cy}; XCLK as output		35	-	65	%
t_r	rise time	0.6 V to 2.6 V		-	-	5	ns
t_f	fall time	2.6 V to 0.6 V		-	-	5	ns
Data and control signal input timing X-port, related to XCLK input							
$t_{su(D)}$	data input set-up time	valid for bits XPCK[1:0] = 01b; valid for inputs: XPD[7:0], HPD[7:0], XRV, XRH and XDQ		6	-	-	ns
$t_{h(D)}$	data input hold time			4	-	-	ns
Data and control signal input timing X-port, related to XCLK output							
$t_{h(Q)}$	data output hold time	valid for bits XPCK[1:0] = 00b; valid for outputs: XPD[7:0], XRH, XRV and XDQ; C_L = 30 pF		2	-	-	ns
t_{PD}	propagation delay	from positive edge of XCLK output; valid for bits XPCK[1:0] = 00b; valid for outputs: XPD[7:0], XRH, XRV and XDQ; C_L = 30 pF		-	-	25	ns
Data and control signal output timing X-port, related to XCLK input							
$t_{h(Q)}$	data output hold time	valid for bits XPCK[1:0] = 01b; valid for output XRDY; C_L = 30 pF		3	-	-	ns
t_{PD}	propagation delay	from positive edge of XCLK input; valid for bits XPCK[1:0] = 01b; valid for output XRDY; C_L = 30 pF		-	-	23	ns

Table 41. X-port *…continued*

Attention: *Digital inputs and I/O ports are not 5 V tolerant.*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Data and control signal output timing X-port, related to XCLK output[2]							
$t_{h(Q)}$	data output hold time	valid for bits XPCK[1:0] = 01b; valid for outputs: XPD[7:0], XRH, XRV, XDQ, RTS0, RTS1 and RTCO; C_L = 30 pF		2	-	-	ns
t_{PD}	propagation delay	from positive edge of XCLK output; valid for bits XPCK[1:0] = 01b; valid for outputs: XPD[7:0], XRH, XRV, XDQ, RTS0, RTS1 and RTCO; C_L = 30 pF		-	-	23	ns
		from ADC to XPD	[3]	4.90	-	5.46	µs

[1] From internal PLL (clock oscillator)

[2] The effects of rise and fall times are included in the calculation of $t_{h(Q)}$ and t_{PD}. Timings and levels refer to drawings and conditions illustrated in Figure 18.

[3] $t_{PD} = 140 \times T_{cy}$ for pin LLC; see Table 40.

Table 42. I-port, IX-port and H-port

Attention: *Digital inputs and I/O ports are not 5 V tolerant.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{o(L)}$	output load capacitance	at all outputs	15	-	30	pF
ICLK input and output timing; see Figure 19						
T_{cy}	cycle time	pin ICLK as input	31	-	100	ns
		pin ICLK as output	18	-	45	ns
δ	duty cycle	for t_{ICLKH}/T_{cy}	35	-	65	%
t_r	rise time	0.6 V to 2.6 V	-	-	5	ns
t_f	fall time	2.6 V to 0.6 V	-	-	5	ns
Data and control signal output timing I-port, pins IDQ, IGP1, IPG0, IGPH and IGPV, IX-port and H-port						
$t_{h(Q)}$	data output hold time	valid for bits IPCK[1:0] = 01b; C_L = 30 pF	2	-	-	ns
t_{PD}	propagation delay	from positive edge of ICLK output; valid for bits IPCK[1:0] = 01b; C_L = 30 pF	-	-	13	ns

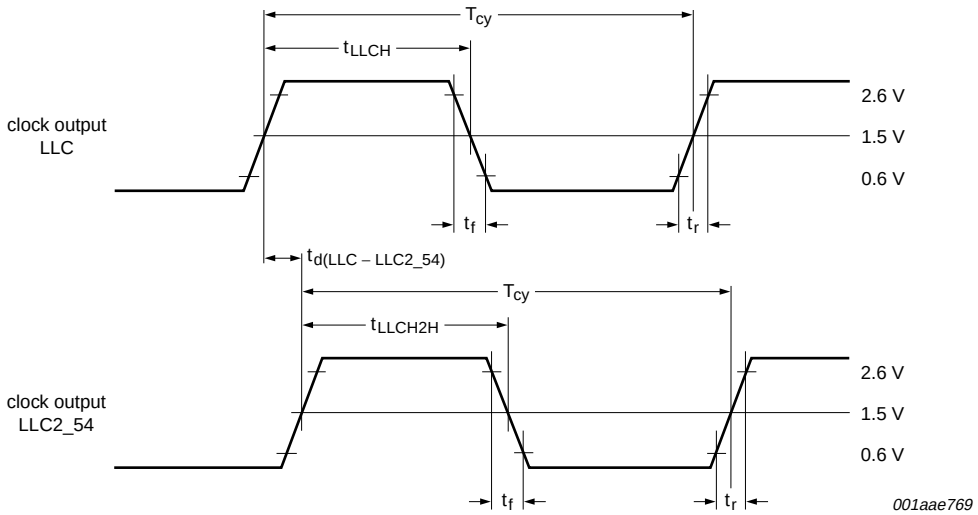
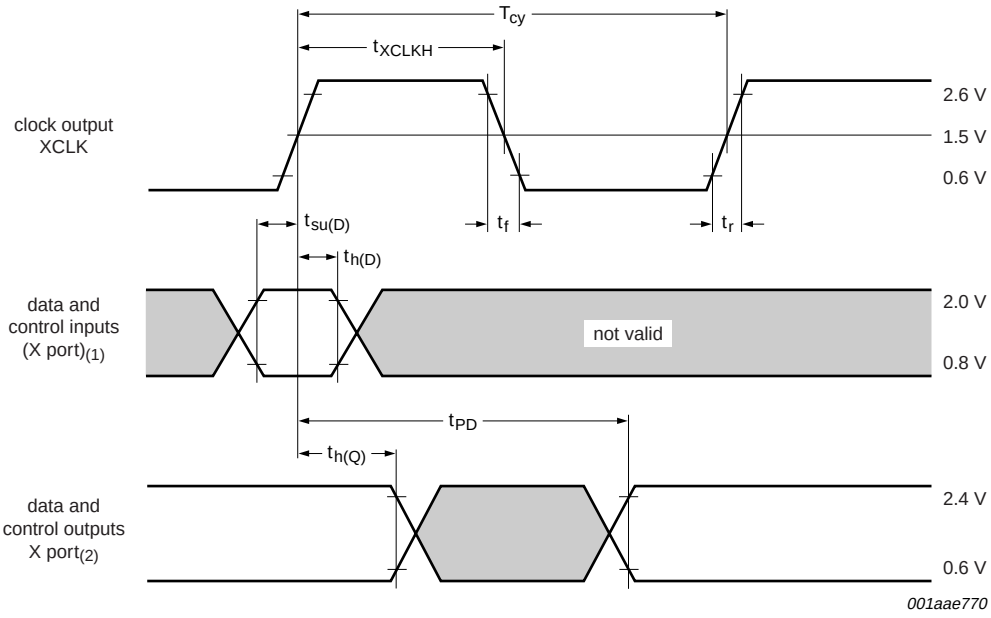


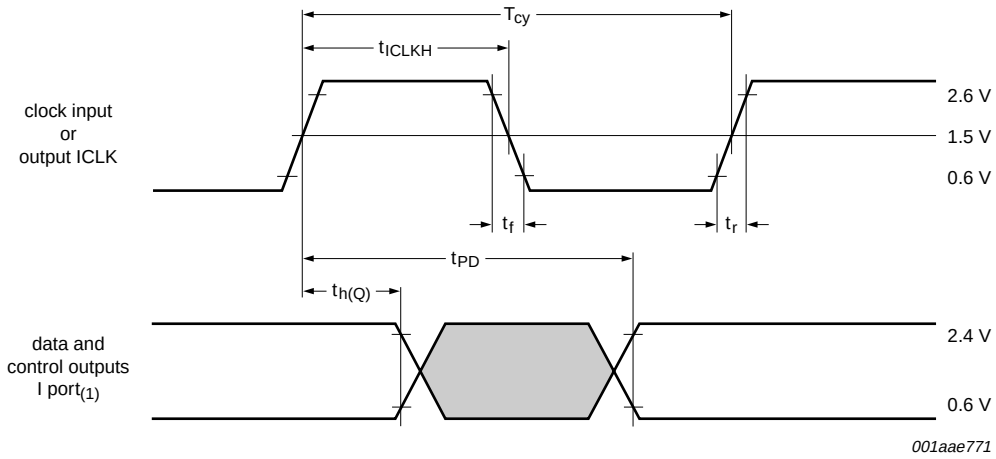
Fig 17. Line-Locked Clock (LLC) output timing



(1) See Table 41.

(2) See Table 41.

Fig 18. X-port input and output timing



(1) See Table 42.

Fig 19. I-port, IX-port and H-port output timing

11. Application information

11.1 General schematics

The schematics from Figure 20 and Figure 21 describe a simple start configuration where all analog inputs can be used either as CVBS or Y/C inputs. For best performance all analog inputs intended for RGB or YUV components only should be terminated directly by 75 Ω (instead of 27 Ω and 47 Ω voltage divider).

Remark: the recommended standard resistor divider combination (27 Ω and 47 Ω) has been changed from 18 Ω and 56 Ω formerly used with the SAA7118. The recommended input capacity has also been changed from 47 nF (SAA7118) to 22 nF.

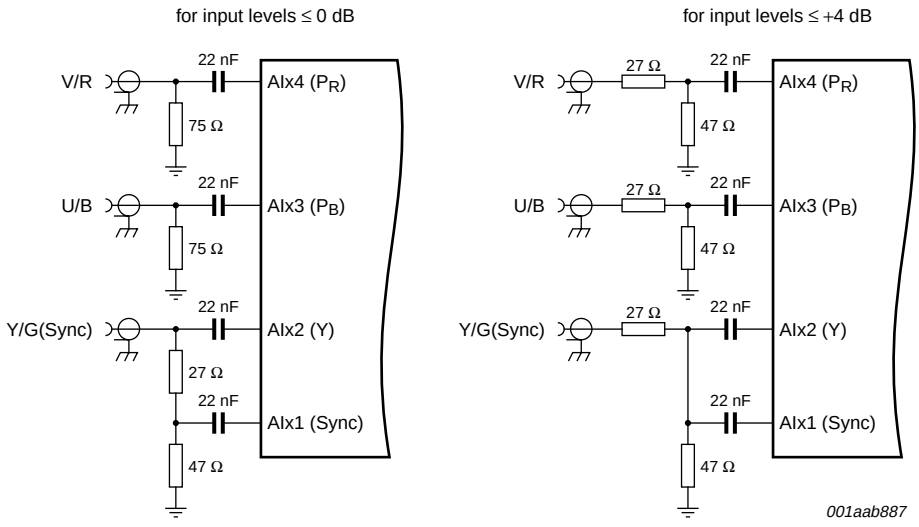


Fig 20. Connection of YUV and RGB signal with SYNC on green

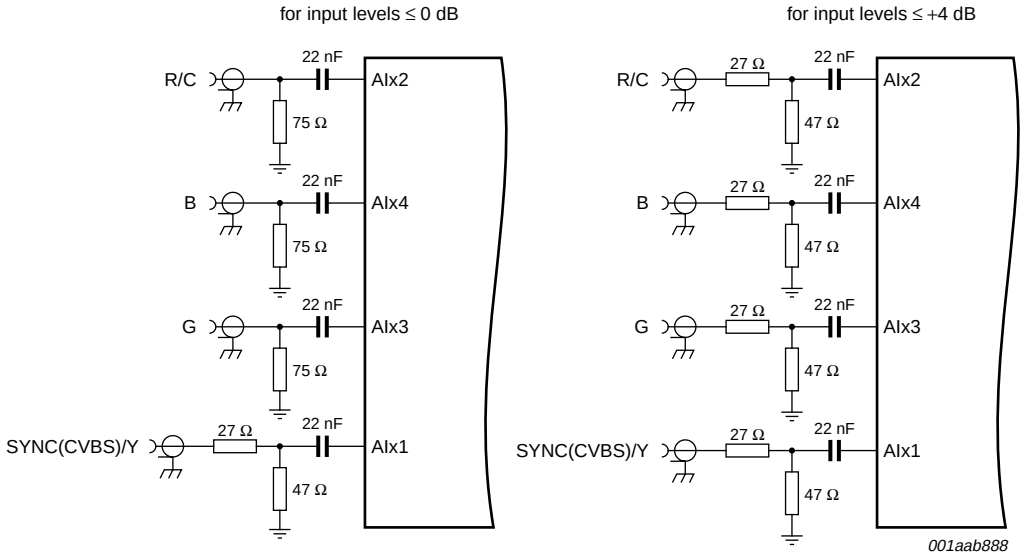
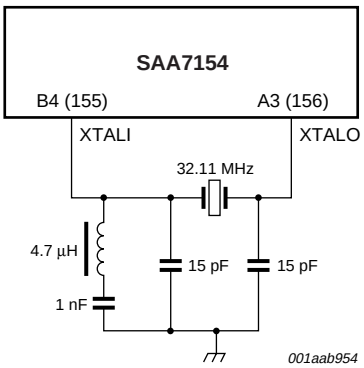
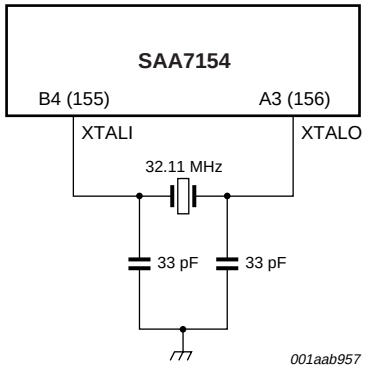


Fig 21. Connection for RGB with SYNC on separate input

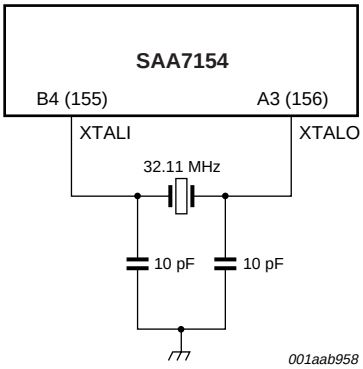
11.2 Oscillator applications



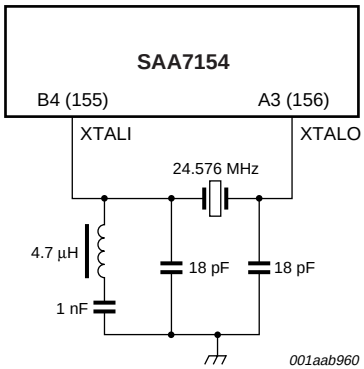
a. With 3rd harmonic quartz crystal. Crystal load C_L = 8 pF.



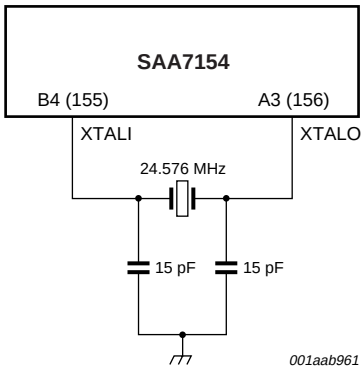
b. With fundamental quartz crystal. Crystal load C_L = 20 pF.



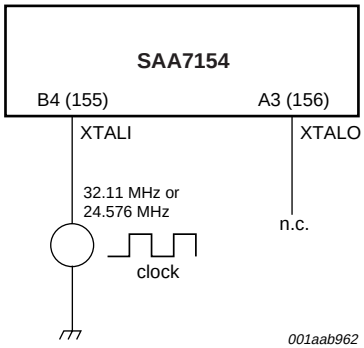
c. With fundamental quartz crystal. Crystal load C_L = 8 pF.



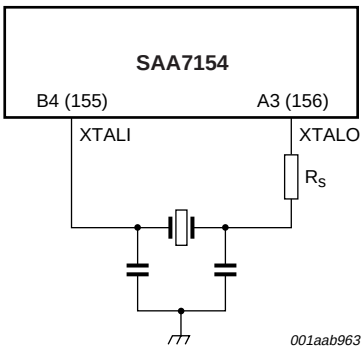
d. With 3rd harmonic quartz crystal. Crystal load C_L = 8 pF.



e. With fundamental quartz crystal. Crystal load C_L = 8 pF.



f. With direct clock.



g. With fundamental quartz crystal and restricted drive level. When P_{drive} of the internal oscillator is too high, a resistance R_s can be placed in series with the output of the oscillator at pin XTALO. Note that the decreased crystal amplitude results in a lower drive level, but on the other hand the jitter performance will decrease.

Fig 22. Oscillator applications

11.3 3-bit ADC application

The SAA7154E; SAA7154H has 3-bit ADCs, which can be selected on input groups AI3x and AI4x. They permit many applications (see Figure 23, Section 7.1.1.1, Section 7.4 and Section 7.14.1):

- DC-level detection for D-connector and SCART
- FSW-control
- external VGA vertical sync input
- analog OSD-overlay.

Table 43. Voltage ranges

Application	Voltage range of input signal	Voltage range at pin
AV-mode	0 V to 12 V	0 V to 1.304 V
D-terminal	0 V to 5 V	0 V to 1.531 V
FSW	0 V to 3 V	0 V to 3 V
VGA sync	0 V to 5 V	0 V to 1.4 V
analog OSD (teletext decoder)	1.304 V maximum	1.304 V maximum

Table 44. Relationship between logic levels and ADC slices for different applications

Application	ADC slices (%)[1]							
	0 to 12.5	12.5 to 25	25 to 37.5	37.5 to 50	50 to 62.5	62.5 to 75	75 to 87.5	87.5 to 100
AV mode	low: 0 % to 16.7 %		-	middle: 37.5 % to 58.3 %		-	high: 79.2 % to 100 %	
D-terminal	low: 0 % to 14.1 % of 1.304 V		middle: 32.9 % to 56.3 % of 1.304 V			-	high: 82.2 % to > 100 % of 1.304 V	
FSW	≤ 0.4 V (30.7 %)		slope				> 1 V (76.7 %)	

[1] The definition, the function and the required ADC slices depend on the application of pins AI3x to AI4x.

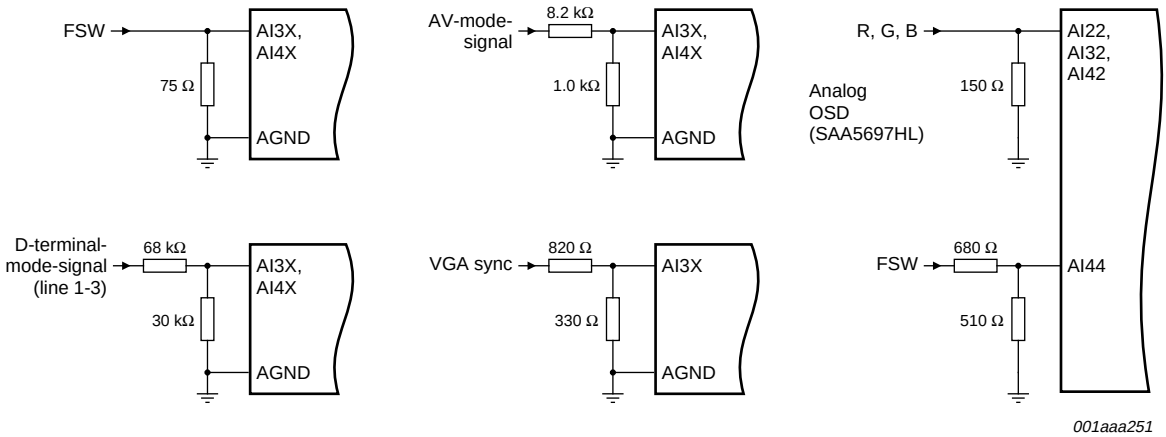


Fig 23. External connection of different signal inputs

11.4 Digital OSD application

Figure 24 shows an example of an OSD application with the external OSD controller chip MTV048.

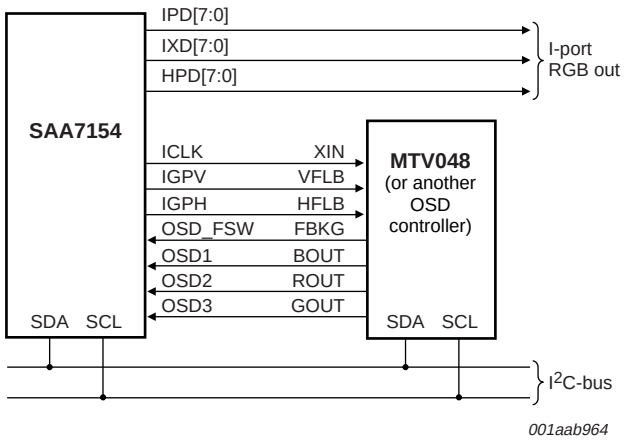


Fig 24. Application of SAA7154E; SAA7154H and an OSD controller chip (e.g. Myson MTV048)

12. Test information

12.1 Boundary scan test

The SAA7154E; SAA7154H has built-in logic and 5 dedicated pins to support boundary scan testing which allows board testing without special hardware. The SAA7154E; SAA7154H follows the *IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture* set by the Joint Test Action Group (JTAG).

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRST_N), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 45). Details about the JTAG BST-TEST can be found in specification *IEEE Std. 1149.1*. A file containing the detailed Boundary Scan Description Language (BSDL) description of the SAA7154E; SAA7154H is available on request.

Table 45. BST instructions supported by the SAA7154E; SAA7154H

Instruction	Description
BYPASS	This mandatory instruction provides a minimum length serial path (1-bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.

Table 45. BST instructions supported by the SAA7154E; SAA7154H *…continued*

Instruction	Description
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

12.1.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRST_N pin to LOW.

12.1.2 Device identification codes

A device identification register is specified in *IEEE Std. 1149.1b-1994*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (closest to TDI) and bit 0 is the least significant bit (closest to TDO); see Figure 25.

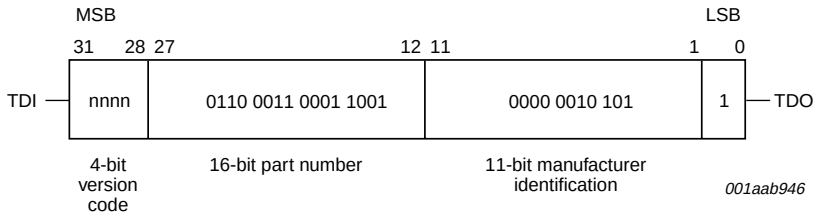
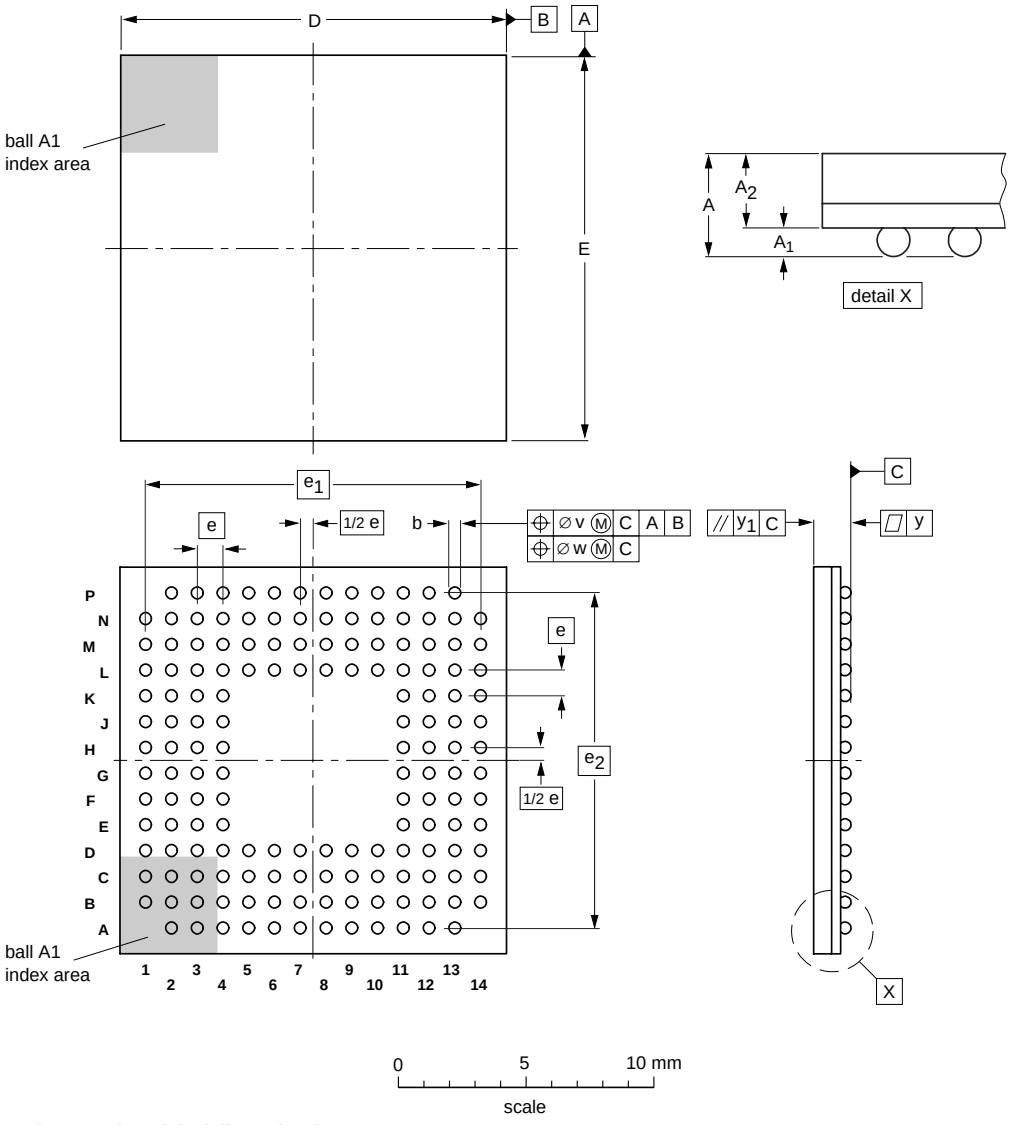


Fig 25. 32 bits of identification code

13. Package outline

LBGA156: plastic low profile ball grid array package; 156 balls; body 15 x 15 x 1.05 mm **SOT700-1**



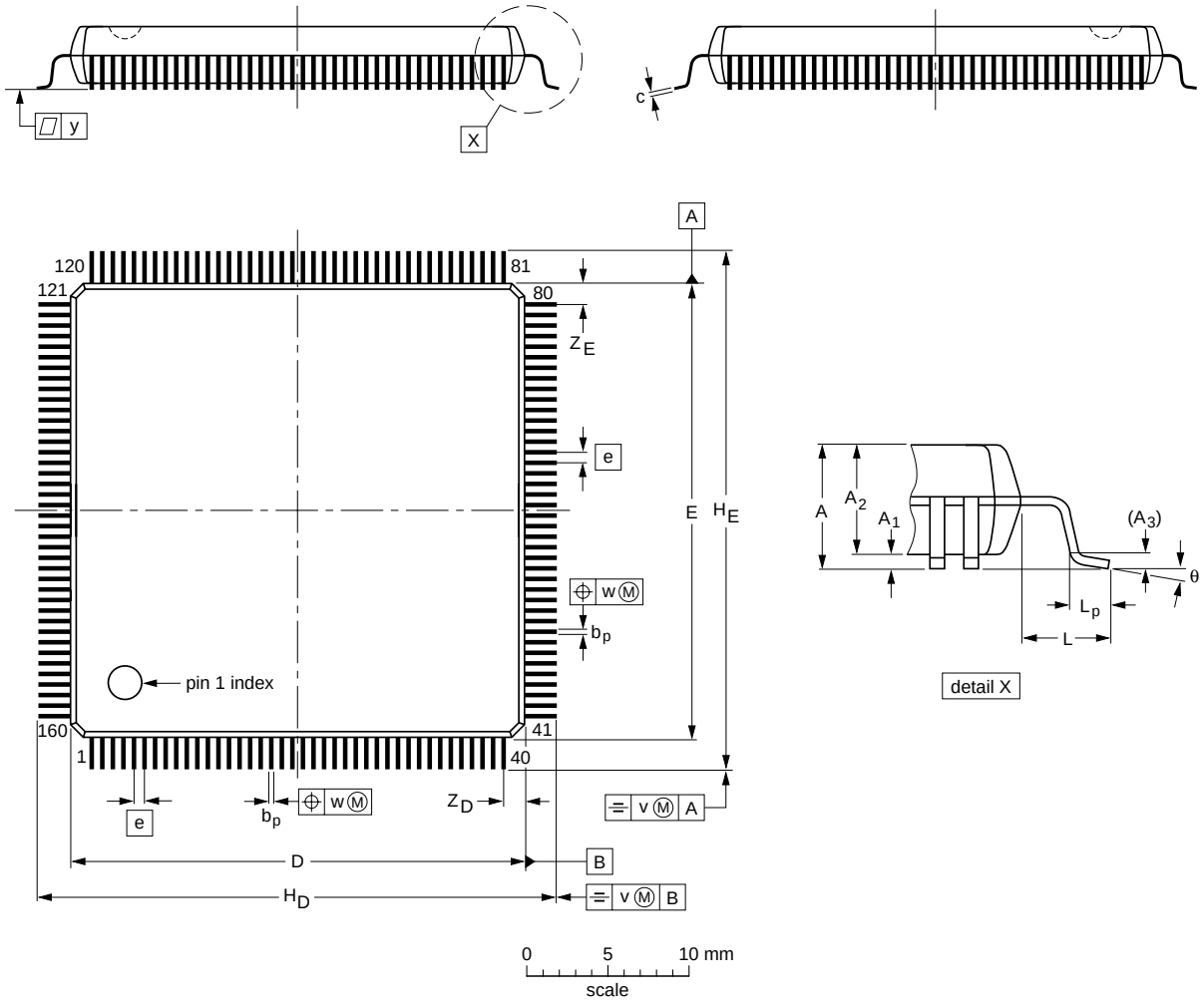
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.65	0.45 0.35	1.20 0.95	0.55 0.45	15.2 14.8	15.2 14.8	1	13	13	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT700-1	- - -	MO-192	- - -			~~01-05-11~~ 01-11-06

Fig 26. Package outline SOT700-1 (LBGA156)

QFP160: plastic quad flat package;
160 leads (lead length 1.6 mm); body 28 x 28 x 3.4 mm; high stand-off height **SOT322-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	4.07	0.50 0.25	3.6 3.2	0.25	0.38 0.22	0.23 0.13	28.1 27.9	28.1 27.9	0.65	31.45 30.95	31.45 30.95	1.6	1.03 0.73	0.3	0.13	0.1	1.5 1.1	1.5 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT322-2	135E12	MS-022				~~00-01-19~~ 03-02-25

Fig 27. Package outline SOT 322-2 (QFP160)

14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 28) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 46 and 47

Table 46. SnPb eutectic process (from J-STD-020C)

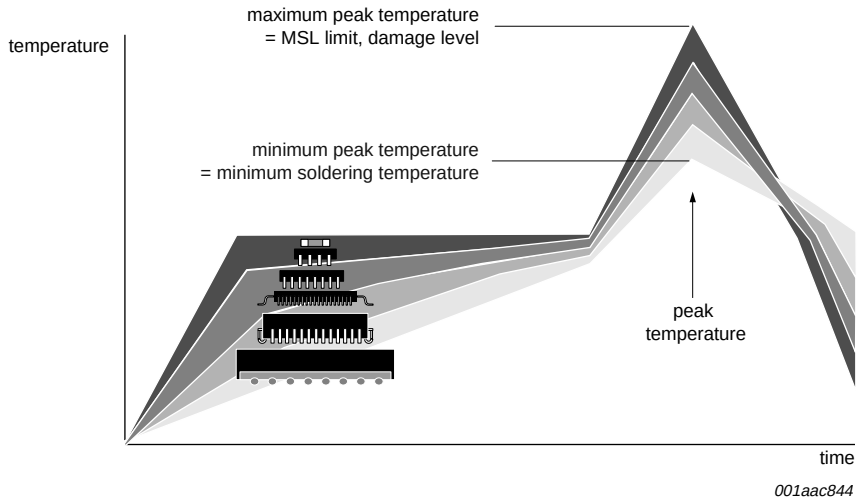
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 47. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 28.



MSL: Moisture Sensitivity Level

Fig 28. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 48. Abbreviations

Acronym	Description
ACM	ACcumulation Mode
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AIC	Analog Input Control
ANC	ANCillary data packet[1]
AV	Audio and Video
BCS	Brightness-Contrast-Saturation
BST	Boundary Scan Test
CC	Closed Caption
CCST	Chinese Character System Teletext
CE	Chip Enable
CG	Clock Generation
CGC	Clock Generation Circuit
CGMS	Copy Generation Management System
CIF	Common Intermediate Format
CMOS	Complementary MOS
CTI	Color Transient Improvement
CVBS	Color Video Blanking Signal
DCI	Dynamic Contrast Improvement

Table 48. Abbreviations *...continued*

Acronym	Description
DVD	Digital Versatile Disc
EAV	End of Active Video
EDGI	EDge-Guided Interpolation (in vertical direction)
ESD	ElectroStatic Discharge
FIFO	First-In First-Out
FIR	Finite Impulse Response
FSW	Fast SWitch
HDTV	High Definition TV
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
ISD	Input Source Detection
ITU	International Telecommunication Union
JEDEC	Joint Electronic Device Engineering Council
JTAG	Joint Test Architecture Group
LCD	Liquid Crystal Display
LLC	Line-Locked Clock
LSB	Least Significant Bit
LUT	Look-Up Table
MOS	Metal-Oxide-Semiconductor
MPEG	Motion Picture Estimation Group
MSB	Most Significant Bit
MUX	MUltipleXer
NABTS	North-American Broadcast Text System
NTSC	National Television Systems Committee
OSD	On-Screen Display
PAL	Phase Alternating Line
PC	Personal Computer
PLL	Phase-Locked Loop
PVR	Personal Video Recording
RGB	Red-Green-Blue
RMS	Root Mean Square
RTC	Real-Time Control
RTCO	Real-Time Control Output
SAV	Start of Active Video
SCART	Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs
SECAM	Systeme Electronique Couleur Avec Mémoire (French color TV standard)
SDTV	Standard Definition TV
SMPTE	Society of Motion Picture and Television Engineers
STB	Set-Top Box
SYNC	SYNChronization
TAP	Test Access Port

Table 48. Abbreviations *...continued*

Acronym	Description
TFT	Thin-Film Transistor
TTL	Transistor-Transistor Logic
TV	TeleVision
VBI	Vertical Blanking Interval
VCR	Video Cassette Recorder
VGA	Video Graphics Array
VITC	Vertical Interval Time Code
VPD	Variable Phase Delay
VPS	Video Program System
VTR	Video Tape Recorder
WSS	Wide Screen Signalling
WST	World System Teletext
XDS	eXtended Data Service
XTAL	CrysTAL[2]

[1] For example, VBI data can be inserted as ANC data into the video stream.

[2] X became a synonym for Crys.

16. Glossary

H-port — Digital host-port for extension of the image port or expansion port from 8-bit to 16-bit.

I-port — Digital image-port for scaled video data output.

IX-port — Extended I-port.

RT-port — Digital real-time signal port.

S-video — Separate video; an analog video signal, also known as Y/C.

V-chip — Violence chip: allows blocking of TV-programs based on their rating categories. It is intended for use by parents to manage their children's television viewing.

X-port — Digital video expansion port (X-port), for unscaled digital video input and output.

Y-C_B-C_R — Digital color coding format.

Y-P_B-P_R — Analog color coding format.

17. Revision history

Table 49. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAA7154E_SAA7154H_2	20071206	Product data sheet	-	SAA7154E_SAA7154H_1
Modifications:	• Update of active types (see Table 1 and Table 36) • Adding limiting values for latch-up currents (see Table 35) • Update of ESD related documents (see Table 35) • Presenting information more clearly (see Table 35) • Adding missing abbreviations • Correcting spelling errors • Replacing f_{cl_sco} by the certified symbol $f_{clk(o)(SC)}$ (see Section 7.6.1.2 and Section 7.6.1.3)			
SAA7154E_SAA7154H_1 (9397 750 13951)	20070411	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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