SAA7160

PCI Express based audio and video bridge

Rev. 01 — 25 February 2008 **Product data sheet**

1. General description

The SAA7160E and the SAA7160ET are PCI Express based audio and video capture bridges. Both devices provide ports for capturing video streams, transport streams, program streams and audio streams with audio functionality like I²S-bus inputs. The bridges provide audio and video capture function as required for PCI Express applications like Microsoft ‘multimedia center’.

The target is to cover a range of performance applications like personal video recording and PC TV cards.

The SAA7160E and the SAA7160ET are highly integrated circuits for TV insertion inside PC systems. Additional high-speed programming ports enable high integrated system solutions for multimedia applications.

2. Features

2.1 PCI Express interface SAA7160E and SAA7160ET

- Compliant to PCI Express Base Specification 1.0a
- Native PCI Express
  - 64-bit address support
  - MSI and INT_A message support
- The PCI Express circuit supports isochronous data traffic intended for uninterrupted transfer of streaming data like video streaming
  - x1 PCI Express endpoint device (2.5 Gbit/s)
  - Low jitter and bit error rate
- Type 0 configuration space header
  - Single BAR; configurable address range of 17 bits, 18 bits, 19 bits or 20 bits dependent on application requirements
- DMA write support
  - 12 DMA write channels for AV streaming
  - Managing up to 8 software buffers per DMA channel
  - Buffer size of 2 MB extendable to 4 MB (e.g. HDTV)
  - Round-robin arbitration between DMAs

    Support overflow recovery if PCI Express bandwidth is not granted in the required amount

founded by Philips

- DMA read support
  - Autonomous address translation on PCI Express bus
  - One DMA read channel for reading from page table(s) in system memory
- PCI Express capabilities
  - 128 B write packet size and 64 B read packet size
  - MSI support
  - INT_A emulation

2.2 Digital interfaces SAA7160E

- Digital video input ports of 60 pins usable for maximum clock rates up to 75 MHz
  - Six independent standard TV (ITU-R BT.656) 8-bit or 10-bit wide input streams (27 MHz)
    or
  - Two standard TV 20-bit wide input streams
    or
  - Four TS or PS 8-bit wide input streams (13.5 MHz to 54 MHz) and two independent standard TV (ITU-R BT.656) 8-bit or 10-bit wide input streams
    or
  - One HDTV 20-bit wide input stream (75 MHz)

2.3 Digital interfaces SAA7160ET

- Digital video input ports of 20 pins usable for maximum clock rates up to 75 MHz
  - Two independent standard TV (ITU-R BT.656) 8-bit or 10-bit wide input streams (27 MHz)
    or
  - Two TS or PS 8-bit wide input streams (13.5 MHz to 54 MHz)
    or
  - One TS or PS 8-bit wide input stream (13.5 MHz to 54 MHz) and one independent standard TV (ITU-R BT.656) 8-bit or 10-bit wide input stream
    or
  - One HDTV 20-bit wide input stream (75 MHz)

2.4 Digital peripheral audio interfaces SAA7160E and SAA7160ET

- Two independent I^2S-bus input channels supporting 32 kHz, 44.1 kHz or 48 kHz

2.5 Peripheral programming ports SAA7160E

- Two I^2C-bus interfaces
  - I^2C-bus master port to program other peripheral devices
  - Support register access with 100 kHz and 400 kHz bit rate
  - I^2C-bus slave port, usable to support a programming interface for application systems
- One SPI master interface for controlling external peripherals
- PHI; this is an 16-bit wide interface for fast access to microcontroller
  - Supports 8-bit data and 16-bit address interface

- 28 GPIO pins for general I/O purposes, e.g. usable for interrupt input and chip select functions

2.6 Peripheral programming ports SAA7160ET

- Two I^{2}C-bus interfaces
    - I^{2}C-bus master port to program other peripheral devices
    - Support register access with 100 kHz and 400 kHz bit rate
    - I^{2}C-bus slave port, usable to support a programming interface for application systems
- One SPI master interface for controlling external peripherals
- 13 GPIO pins for general I/O purposes, e.g. usable for interrupt input and chip select functions

2.7 General features SAA7160E and SAA7160ET

- Boundary scan test circuit according to *'IEEE Std. 1149.1'*

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAA7160E	LBGA196	plastic low profile ball grid array package; 196 balls; body 15 × 15 × 1 mm	SOT879-1
SAA7160ET	TFBGA88	plastic thin fine-pitch ball grid array package; 88 balls; body 7 × 7 × 0.8 mm	SOT951-1

4. Block diagram

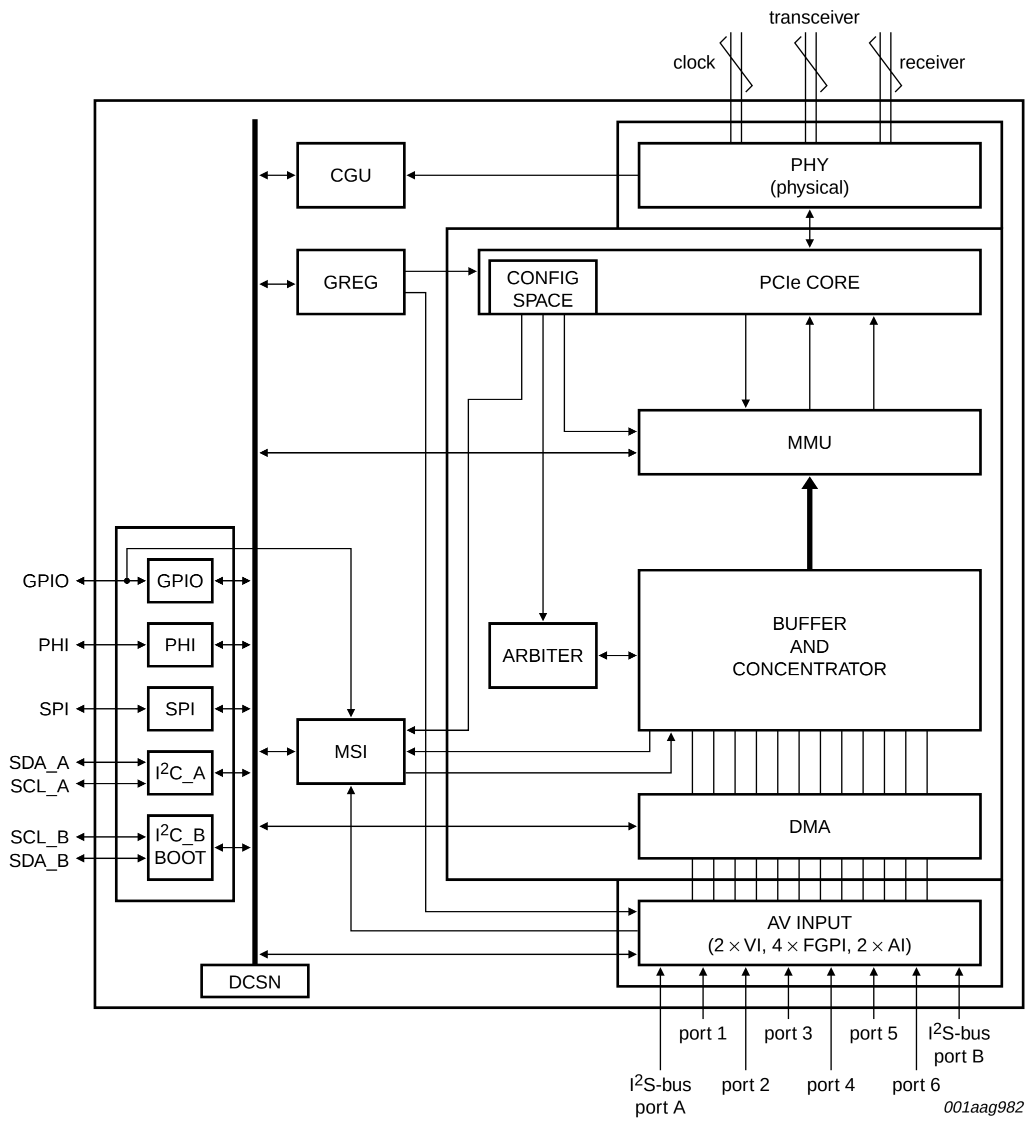

Fig 1. Block diagram of SAA7160

5. Pinning information

5.1 SAA7160E package LBGA196

5.1.1 Pinning

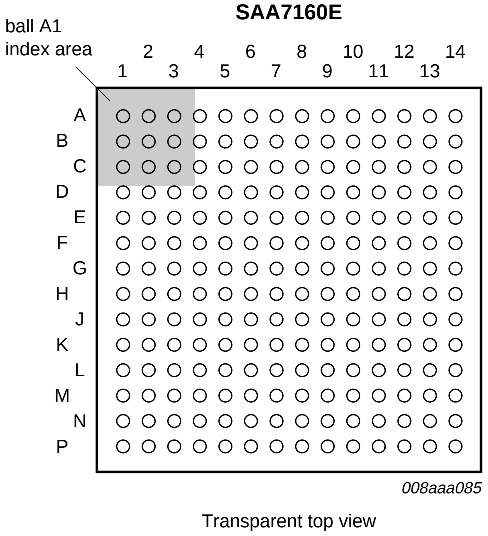

Fig 2. Pin configuration for LBGA196

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	P1_4	P1_5	P1_6	P1_7	P1_CLK	P5_3	P4_CLK	P4_4	P5_CLK	P5_HS	P4_1	P4_0	P6_VS _SOP	P6_HS
B	P1_1	P1_2	P1_3	P1_HS	P5_2	P4_HS	P4_7	P4_5	P5_7	P4_6	P4_VS _SOP	P4_2	P6_VAL	P6_CLK
C	P2_HS	P2_VS _SOP	P1_0	P1_VS _SOP	P5_5	P5_6	P5_0	P5_4	P5_1	P5_VS _SOP	P4_3	P6_0	P6_1	P6_2
D	P2_CLK	P2_7	P2_6	PHI_7	PHI_8	PHI_RDY_0	PHI_RDN	PHI_WRN	GPIO_17	GPIO_16	PHI_RDY_1	P6_3	P6_4	P6_5
E	P2_5	P2_4	P2_3	PHI_14	PHI_12	V_{DDDI1} (1V25)	V_{DDDE3} (3V3)	V_{DDDE3} (3V3)	PHI_15	PHI_13	PHI_6	P5_VAL	P6_6	P6_7
F	P2_2	P2_1	P2_0	PHI_4	V_{DDDI1} (1V25)	V_{SS}	V_{SS}	V_{SS}	V_{SS}	PHI_10	PHI_11	P4_VAL	P2_VAL	P1_VAL
G	I2S_SCK_B	I2S_SD1_B	I2S_WS_B	PHI_5	V_{DDDE1} (3V3)	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDDE2} (3V3)	PHI_9	I2S_SD1_A	I2S_WS_A	I2S_SD0_A
H	P3_VAL	P3_VS _SOP	I2S_SD0_B	PHI_3	V_{DDDE1} (3V3)	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDDI2} (1V25)	PHI_ALE	PHI_RDY_3	P1_2_VS	I2S_SCK_A
J	P3_HS	P3_CLK	P3_7	PHI_1	PHI_2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$V_{DDDI(1V25)}$/ TEST	PHI_RDY_2	P1_2_HS	P4_5_VS	P1_2_FRE
K	P3_6	P3_5	P3_4	PHI_0	$V_{DDD(PCI0)}$ (1V0)	$V_{DDD(PCI1)}$ (1V0)	$V_{DDD(PCI0)}$ (1V25)	V_{DDDE2} (3V3)	V_{DDDI2} (1V25)	GPIO_6	TEST1	P4_5_HS	GPIO_3	P4_5_FRE
L	P3_3	P3_2	P3_1	GPIO_0	$V_{DDA(PCI0)}$ (3V3)	$V_{DDA(PCI1)}$ (3V3)	$V_{DDD(PCI1)}$ (1V25)	GPIO_29	GPIO_26	GPIO_21	GPIO_10	GPIO_13	GPIO_5	GPIO_2
M	P3_0	SCL_B	TMS	TRSTN	GPIO_1	PCI_PVT	PCI_RESN	BOOT_1	SPI_SL_MA	GPIO_28	GPIO_18	GPIO_14	GPIO_9	GPIO_4
N	SCL_A	SDA_B	TDO	V_{SS}	V_{SS}	PCI_REF CLKP	PCI_REF CLKN	BOOT_0	SPI_MA_SL	GPIO_23	GPIO_20	GPIO_15	GPIO_11	GPIO_7
P	SDA_A	TCK	TDI	PCI_PER _P0	PCI_PER _N0	PCI_PET _P0	PCI_PET _N0	V_{SS}	SPI_CLK	GPIO_27	GPIO_22	GPIO_19	GPIO_12	GPIO_8

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Fig 3. Pin configuration (LBGA196 top view) for SAA7160E

5.1.2 Pin description

Table 2. Description of functional pins

Symbol	Pin	Type[1]	Description
SCL_A	N1	IO	I^2C-bus clock of first I^2C-bus interface
SDA_A	P1	IO	I^2C-bus data of first I^2C-bus interface
I2S_SD0_A	G14	IO	I^2S-bus port A: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
I2S_WS_A	G13	IO	I^2S-bus port A: digital audio input signal for • I2S_WS word select line of Inter IC Sound bus serial interconnect format
I2S_SCK_A	H14	I	I^2S-bus port A: digital audio input signal for • I2S_SCK bit clock of Inter IC Sound bus serial interconnect format
I2S_SD1_A	G12	I	I^2S-bus port A: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
P1_0	C3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV Y[9:0] bit 2 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 0 – program stream data of PS1[7:0] bit 0
P1_1	B1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV Y[9:0] bit 3 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 1 – program stream data of PS1[7:0] bit 1
P1_2	B2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV Y[9:0] bit 4 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 2 – program stream data of PS1[7:0] bit 2
P1_3	B3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV Y[9:0] bit 5 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 3 – program stream data of PS1[7:0] bit 3

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P1_4	A1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV Y[9:0] bit 6 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 4 – program stream data of PS1[7:0] bit 4
P1_5	A2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV Y[9:0] bit 7 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 5 – program stream data of PS1[7:0] bit 5
P1_6	A3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV Y[9:0] bit 8 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 6 – program stream data of PS1[7:0] bit 6
P1_7	A4	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV Y[9:0] bit 9 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS1[7:0] bit 7 – program stream data of PS1[7:0] bit 7
P1_CLK	A5	ID	1. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream clock of TS1 – program stream clock of PS1 2. digital input signal of VIP_1, FGPI_2 or FGPI_3 for – clock signal of parallel video data
P1_HS	B4	ID	digital input signal of VIP_1, FGPI_2 or FGPI_3 for • horizontal synchronization reference in 8-bit STV mode • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV Y[9:0] bit 0
P1_2_HS	J12	ID	horizontal synchronization reference for HD stream from video port 1 and port 2
P1_2_VS	H13	ID	vertical synchronization reference for HD stream from video port 1 and port 2
P1_2_FRE	J14	ID	field indication reference for HD stream from video port 1 and port 2

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P1_VS_SOP	C4	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV Y[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal ‘start of package’ of FGPI_2 or FGPI_3 for parallel – program stream data of PS1 – transport stream data of TS1
P1_VAL	F14	ID	digital input control signal ‘valid data’ of FGPI_2 or FGPI_3 for parallel • transport stream data of TS1 • program stream data of PS1 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
P2_0	F3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV UV[9:0] bit 2 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 0 – program stream data of PS2[7:0] bit 0
P2_1	F2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV UV[9:0] bit 3 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 1 – program stream data of PS2[7:0] bit 1
P2_2	F1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV UV[9:0] bit 4 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 2 – program stream data of PS2[7:0] bit 2
P2_3	E3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV UV[9:0] bit 5 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 3 – program stream data of PS2[7:0] bit 3

Table 2. Description of functional pins *…continued*

Symbol	Pin	Type[1]	Description
P2_4	E2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV UV[9:0] bit 6 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 4 – program stream data of PS2[7:0] bit 4
P2_5	E1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV UV[9:0] bit 7 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 5 – program stream data of PS2[7:0] bit 5
P2_6	D3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV UV[9:0] bit 8 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 6 – program stream data of PS2[7:0] bit 6
P2_7	D2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV UV[9:0] bit 9 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 7 – program stream data of PS2[7:0] bit 7
P2_CLK	D1	ID	1. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream clock of TS2 – program stream clock of PS2 2. digital input signal of VIP_1, FGPI_2 or FGPI_3 for clock signal of parallel video data
P2_HS	C1	ID	digital input signal of VIP_1, FGPI_2 or FGPI_3 for • horizontal synchronization of digital video port • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV UV[9:0] bit 0

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P2_VS_SOP	C2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV UV[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal ‘start of package’ of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2 – program stream data of PS2
P2_VAL	F13	ID	digital input control signal ‘valid data’ of FGPI_2 or FGPI_3 for parallel • transport stream data of TS2 • program stream data of PS2 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
P3_0	M1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV UV[9:0] bit 2 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 0 – program stream data of PS3[7:0] bit 0
P3_1	L3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV UV[9:0] bit 3 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 1 – program stream data of PS3[7:0] bit 1
P3_2	L2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV UV[9:0] bit 4 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 2 – program stream data of PS3[7:0] bit 2
P3_3	L1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV UV[9:0] bit 5 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 3 – program stream data of PS3[7:0] bit 3

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P3_4	K3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV UV[9:0] bit 6 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 4 – program stream data of PS3[7:0] bit 4
P3_5	K2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV UV[9:0] bit 7 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 5 – program stream data of PS3[7:0] bit 5
P3_6	K1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV UV[9:0] bit 8 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 6 – program stream data of PS3[7:0] bit 6
P3_7	J3	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV UV[9:0] bit 9 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3[7:0] bit 7 – program stream data of PS3[7:0] bit 7
P3_CLK	J2	ID	1. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream clock of TS3 – program stream clock of PS3 2. digital input signal of VIP_1, FGPI_2 or FGPI_3 for – clock signal of parallel video data
P3_HS	J1	ID	digital input signal of VIP_1, FGPI_2 or FGPI_3 for • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV UV[9:0] bit 0 • horizontal synchronization reference in 8-bit STV mode

Table 2. Description of functional pins *…continued*

Symbol	Pin	Type[1]	Description
P3_VS_SOP	H2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV UV[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal ‘start of package’ of FGPI_2 or FGPI_3 for parallel – transport stream data of TS3 – program stream data of PS3
P3_VAL	H1	ID	digital input control signal ‘valid data’ of FGPI_2 or FGPI_3 for parallel • transport stream data of TS3 • program stream data of PS3 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
P4_0	A12	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV Y[9:0] bit 2 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 0 – program stream data of PS4[7:0] bit 0
P4_1	A11	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV Y[9:0] bit 3 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 1 – program stream data of PS4[7:0] bit 1
P4_2	B12	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV Y[9:0] bit 4 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 2 – program stream data of PS4[7:0] bit 2
P4_3	C11	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV Y[9:0] bit 5 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 3 – program stream data of PS4[7:0] bit 3

Table 2. Description of functional pins *…continued*

Symbol	Pin	Type[1]	Description
P4_4	A8	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV Y[9:0] bit 6 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 4 – program stream data of PS4[7:0] bit 4
P4_5	B8	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV Y[9:0] bit 7 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 5 – program stream data of PS4[7:0] bit 5
P4_6	B10	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV Y[9:0] bit 8 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 6 – program stream data of PS4[7:0] bit 6
P4_7	B7	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV Y[9:0] bit 9 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4[7:0] bit 7 – program stream data of PS4[7:0] bit 7
P4_CLK	A7	ID	1. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream clock of TS4 – program stream clock of PS4 2. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – clock signal of parallel video data
P4_HS	B6	ID	digital input signal of VIP_0, FGPI_0 or FGPI_1 for • horizontal synchronization reference in 8-bit STV mode • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV Y[9:0] bit 0
P4_5_HS	K12	ID	horizontal synchronization reference for HD stream from video port 4 and port 5
P4_5_VS	J13	ID	vertical synchronization reference for HD stream from video port 4 and port 5
P4_5_FRE	K14	ID	field indication reference for HD stream from video port 4 and port 5

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P4_VS_SOP	B11	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV Y[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal ‘start of package’ of FGPI_0 or FGPI_1 for parallel – transport stream data of TS4 – program stream data of PS4
P4_VAL	F12	ID	digital input control signal ‘valid data’ of FGPI_0 or FGPI_1 for parallel • transport stream data of TS4 • program stream data of PS4 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
P5_0	C7	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV UV[9:0] bit 2 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 0 – program stream data of PS5[7:0] bit 0
P5_1	C9	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV UV[9:0] bit 3 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 1 – program stream data of PS5[7:0] bit 1
P5_2	B5	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV UV[9:0] bit 4 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 2 – program stream data of PS5[7:0] bit 2
P5_3	A6	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV UV[9:0] bit 5 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 3 – program stream data of PS5[7:0] bit 3

Table 2. Description of functional pins *…continued*

Symbol	Pin	Type[1]	Description
P5_4	C8	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV UV[9:0] bit 6 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 4 – program stream data of PS5[7:0] bit 4
P5_5	C5	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV UV[9:0] bit 7 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 5 – program stream data of PS5[7:0] bit 5
P5_6	C6	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV UV[9:0] bit 8 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 6 – program stream data of PS5[7:0] bit 6
P5_7	B9	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV UV[9:0] bit 9 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5[7:0] bit 7 – program stream data of PS5[7:0] bit 7
P5_CLK	A9	ID	1. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream clock for port TS5 – program stream clock for port PS5 2. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – clock signal of parallel video data
P5_HS	A10	ID	digital input signal of VIP_0, FGPI_0 or FGPI_1 for • horizontal synchronization reference in 8-bit STV mode • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV UV[9:0] bit 0

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P5_VS_SOP	C10	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV UV[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal ‘start of package’ of FGPI_0 or FGPI_1 for parallel – transport stream data of TS5 – program stream data of PS5
P5_VAL	E12	ID	digital input control signal ‘valid data’ of FGPI_0 or FGPI_1 for parallel • transport stream data of TS5 • program stream data of PS5 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
P6_0	C12	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV UV[9:0] bit 2 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 0 – program stream data of PS6[7:0] bit 0
P6_1	C13	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV UV[9:0] bit 3 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 1 – program stream data of PS6[7:0] bit 1
P6_2	C14	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV UV[9:0] bit 4 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 2 – program stream data of PS6[7:0] bit 2
P6_3	D12	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV UV[9:0] bit 5 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 3 – program stream data of PS6[7:0] bit 3

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P6_4	D13	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV UV[9:0] bit 6 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 4 – program stream data of PS6[7:0] bit 4
P6_5	D14	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV UV[9:0] bit 7 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 5 – program stream data of PS6[7:0] bit 5
P6_6	E13	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV UV[9:0] bit 8 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 6 – program stream data of PS6[7:0] bit 6
P6_7	E14	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV UV[9:0] bit 9 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 7 – program stream data of PS6[7:0] bit 7
P6_CLK	B14	ID	1. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream clock of TS6 – program stream clock of PS6 2. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – clock signal for parallel video data modes
P6_HS	A14	ID	digital input signal of VIP_0, FGPI_0 or FGPI_1 for • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV UV[9:0] bit 0 • horizontal synchronization reference in 8-bit STV mode

Table 2. Description of functional pins *…continued*

Symbol	Pin	Type[1]	Description
P6_VS_SOP	A13	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV UV[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal 'start of package' of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6 – program stream data of PS6
P6_VAL	B13	ID	digital input control signal 'valid data' of FGPI_0 or FGPI_1 for parallel • transport stream data of TS6 • program stream data of PS6 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
GPIO_0	L4	IOU	GPIO: programming control port signal for • general purpose input/output port 0 • external interrupt 0; interrupt edge sensitive with programmable edge polarity
GPIO_1	M5	IOU	GPIO: programming control port signal for • general purpose input/output port 1 • external interrupt 1; interrupt edge sensitive with programmable edge polarity
GPIO_2	L14	IOU	GPIO: programming control port signal for • general purpose input/output port 2 • external interrupt 2; interrupt edge sensitive with programmable edge polarity
GPIO_3	K13	IOU	GPIO: programming control port signal for • general purpose input/output port 3 • external interrupt 3; interrupt edge sensitive with programmable edge polarity
GPIO_4	M14	IOU	GPIO: programming control port signal for • general purpose input/output port 4 • external interrupt 4; interrupt edge sensitive with programmable edge polarity
GPIO_5	L13	IOU	GPIO: programming control port signal for • general purpose input/output port 5 • external interrupt 5; interrupt edge sensitive with programmable edge polarity
GPIO_6	K10	IOU	GPIO: programming control port signal for • general purpose input/output port 6 • external interrupt 6; interrupt edge sensitive with programmable edge polarity
GPIO_7	N14	IOU	GPIO: programming control port signal for • general purpose input/output port 7 • external interrupt 7; interrupt edge sensitive with programmable edge polarity
GPIO_8	P14	IOU	GPIO: programming control port signal for • general purpose input/output port 8 • external interrupt 8; interrupt edge sensitive with programmable edge polarity
GPIO_9	M13	IOU	GPIO: programming control port signal for • general purpose input/output port 9 • external interrupt 9; interrupt edge sensitive with programmable edge polarity

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
GPIO_10	L11	IOU	GPIO: programming control port signal for • general purpose input/output port 10 • external interrupt 10; interrupt edge sensitive with programmable edge polarity
GPIO_11	N13	IOU	GPIO: programming control port signal for • general purpose input/output port 11 • external interrupt 11; interrupt edge sensitive with programmable edge polarity
GPIO_12	P13	IOU	GPIO: programming control port signal for • general purpose input/output port 12 • external interrupt 12; interrupt edge sensitive with programmable edge polarity
GPIO_13	L12	IOU	GPIO: programming control port signal for • general purpose input/output port 13 • external interrupt 13; interrupt edge sensitive with programmable edge polarity
GPIO_14	M12	IOU	GPIO: programming control port signal for • general purpose input/output port 14 • external interrupt 14; interrupt edge sensitive with programmable edge polarity
GPIO_15	N12	IOU	GPIO: programming control port signal for • general purpose input/output port 15 • external interrupt 15; interrupt edge sensitive with programmable edge polarity
GPIO_16	D10	IOU	GPIO: programming control port signal for • general purpose input/output port 16 • PHI chip select to other external devices (active LOW)
GPIO_17	D9	IOU	GPIO: programming control port signal for • general purpose input/output port 17 • PHI chip select to other external devices (active LOW)
GPIO_18	M11	IOU	GPIO: programming control port signal for • general purpose input/output port 18 • PHI chip select to other external devices (active LOW)
GPIO_19	P12	IOU	GPIO: programming control port signal for • general purpose input/output port 19 • PHI chip select to other external devices (active LOW)
GPIO_20	N11	IOU	GPIO: programming control port signal for • general purpose input/output port 20 • PHI chip select to other external devices (active LOW)
GPIO_21	L10	IOU	GPIO: programming control port signal for • general purpose input/output port 21 • PHI chip select to other external devices (active LOW)
GPIO_22	P11	IOU	GPIO: programming control port signal for • general purpose input/output port 22 • PHI chip select to other external devices (active LOW)
GPIO_23	N10	IOU	GPIO: programming control port signal for • general purpose input/output port 23 • PHI chip select to other external devices (active LOW)

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
GPIO_26	L9	IOU	GPIO: programming control port signal for • general purpose input/output port 26
GPIO_27	P10	IOU	GPIO: programming control port signal for • general purpose input/output port 27
GPIO_28	M10	IOU	GPIO: programming control port signal for • general purpose input/output port 28
GPIO_29	L8	IOU	GPIO: programming control port signal for • general purpose input/output port 29
BOOT_0	N8	IOU	GPIO: programming control port signal for • general purpose input/output port 30 • boot mode GPIO_[31:30] bit 0
BOOT_1	M8	IOU	GPIO: programming control port signal for • general purpose input/output port 31 • boot mode GPIO_[31:30] bit 1
PHI_0	K4	IO	PHI signal for • data input/output port bit 0 • Intel microcontroller multiplexed address output or data input port bit 0
PHI_1	J4	IO	PHI signal for • data input/output port bit 1 • Intel microcontroller multiplexed address output or data input port bit 1
PHI_2	J5	IO	PHI signal for • data input/output port bit 2 • Intel microcontroller multiplexed address output or data input port bit 2
PHI_3	H4	IO	PHI signal for • data input/output port bit 3 • Intel microcontroller multiplexed address output or data input port bit 3
PHI_4	F4	IO	PHI signal for • data input/output port bit 4 • Intel microcontroller multiplexed address output or data input port bit 4
PHI_5	G4	IO	PHI signal for • data input/output port bit 5 • Intel microcontroller multiplexed address output or data input port bit 5
PHI_6	E11	IO	PHI signal for • data input/output port bit 6 • Intel microcontroller multiplexed address output or data input port bit 6
PHI_7	D4	IO	PHI signal for • data input/output port bit 7 • Intel microcontroller multiplexed address output or data input port bit 7
PHI_8	D5	IO	PHI signal for • data input/output port bit 8 • Intel microcontroller multiplexed address output or data input port bit 8

Table 2. Description of functional pins *…continued*

Symbol	Pin	Type[1]	Description
PHI_9	G11	IO	PHI signal for • data input/output port bit 9 • Intel microcontroller multiplexed address output or data input port bit 9
PHI_10	F10	IO	PHI signal for • data input/output port bit 10 • Intel microcontroller address output port bit 10
PHI_11	F11	IO	PHI signal for • data input/output port bit 11 • Intel microcontroller address output port bit 11
PHI_12	E5	IO	PHI signal for • data input/output port bit 12 • Intel microcontroller address output port bit 12
PHI_13	E10	IO	PHI signal for • data input/output port bit 13 • Intel microcontroller address output port bit 13
PHI_14	E4	IO	PHI signal for • data input/output port bit 14 • Intel microcontroller address output port bit 14
PHI_15	E9	IO	PHI signal for • data input/output port bit 15 • Intel microcontroller address output port bit 15
PHI_WRN	D8	IOU	PHI signal for • data write cycle indicator ‘WRN’ (active LOW)
PHI_RDN	D7	IOU	PHI signal for • data read cycle indicator ‘RDN’ (active LOW)
PHI_RDY_0	D6	IOU	PHI signal for • PHI, parallel host port ready/wait indicator ‘phi_rdy_0’
PHI_RDY_1	D11	IOU	PHI signal for • ready/wait indicator ‘phi_rdy_1’
PHI_RDY_2	J11	IOD	PHI signal for • external parallel host port ready/wait indicator ‘phi_rdy_2’
PHI_RDY_3	H12	IOD	PHI signal for • external parallel host port ready/wait indicator ‘phi_rdy_3’
PHI_ALE	H11	IOD	PHI signal for • output address latch enable; latches the LOW byte of the address
PCI_PER_P0	P4	AI	PCI Express differential receive data input 0 (positive)
PCI_PER_N0	P5	AI	PCI Express differential receive data input 0 (negative)
PCI_PET_P0	P6	AO	PCI Express differential transmit data output 0 (positive)
PCI_PET_N0	P7	AO	PCI Express differential transmit data output 0 (negative)
PCI_REFCLKP	N6	AI	PCI Express clock 100 MHz differential input (positive)
PCI_REFCLKN	N7	AI	PCI Express clock 100 MHz differential input (negative)

Table 2. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
PCI_PVT	M6	AI	this signal is used to create a compensation signal internally which will adjust the I/O pads' characteristics as PVT drifts; connect 33 Ω resistor to $V_{DDD(PCI0)(1V0)}$
PCI_RESN	M7	ID	system reset (active LOW)
TRSTN	M4	IU	JTAG test reset input: drive HIGH for JTAG mode, drive LOW for normal operation
TCK	P2	IU	JTAG test clock input
TMS	M3	IU	JTAG test mode select
TDO	N3	O	JTAG test serial data output
TDI	P3	IU	JTAG test serial data input
SPI_CLK	P9	IU	SPI clock
SPI_MA_SL	N9	IOU	SPI; transfer serial data from master to slave (slave data input or master data output)
SPI_SL_MA	M9	IOU	SPI; transfer serial data from slave to master (master data input or slave data output)
TEST1	K11	ID	enable test mode 1; must be connected to V_{SS}
SCL_B	M2	IO	I^2C-bus clock of second I^2C-bus interface (interface can be used for boot EEPROM)
SDA_B	N2	IO	I^2C-bus data of second I^2C-bus interface (interface can be used for boot EEPROM)
I2S_SD0_B	H3	IO	I^2S-bus port B: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
I2S_SD1_B	G2	IO	I^2S-bus port B: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
I2S_WS_B	G3	IO	I^2S-bus port B: digital audio input signal for • I2S_WS word select line of Inter IC Sound bus serial interconnect format
I2S_SCK_B	G1	I	I^2S-bus port B: digital audio input signal for • I2S_SCK bit clock of Inter IC Sound bus serial interconnect format

[1] The pin types are defined in Table 3.

Table 3. Pin type description

Type	Description
AI	analog input
AO	analog output
I	digital input
ID	input with pull-down
IO	digital input and output
IOD	input and output with pull-down
IOU	input and output with internal pull-up
IU	input with internal pull-up
O	digital output

Table 4. Supply pins

Symbol	Pin	Description
3.3 V IO supply voltage		
$V_{DDDE1(3V3)}$	G5, H5	digital extend supply voltage 1 (3.3 V)
$V_{DDDE2(3V3)}$	G10, K8	digital extend supply voltage 2 (3.3 V)
$V_{DDDE3(3V3)}$	E7, E8	digital extend supply voltage 3 (3.3 V)
3.3 V analog supply voltage		
$V_{DDA(PCI0)(3V3)}$	L5	PCI Express 0 analog supply voltage (3.3 V)
$V_{DDA(PCI1)(3V3)}$	L6	PCI Express 1 analog supply voltage (3.3 V)
1.0 V IO supply voltage		
$V_{DDD(PCI0)(1V0)}$	K5	PCI Express 0 digital supply voltage (1.0 V)
$V_{DDD(PCI1)(1V0)}$	K6	PCI Express 1 digital supply voltage (1.0 V)
1.25 V core supply voltage		
$V_{DDDI1(1V25)}$	E6, F5	digital internal supply voltage 1 (1.25 V)
$V_{DDDI2(1V25)}$	H10, K9	digital internal supply voltage 2 (1.25 V)
$V_{DDDI(1V25)}$/TEST	J10	digital internal supply voltage (1.25 V) and power start-up test input; must be connected to 1.25 V
$V_{DDD(PCI0)(1V25)}$	K7	PCI Express 0 digital supply voltage (1.25 V)
$V_{DDD(PCI1)(1V25)}$	L7	PCI Express 1 digital supply voltage (1.25 V)
Ground supply voltage		
V_{SS}	G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, F6, F7, F8, F9, N4, N5, P8	ground supply voltage

5.2 SAA7160ET package TFBGA88

5.2.1 Pinning

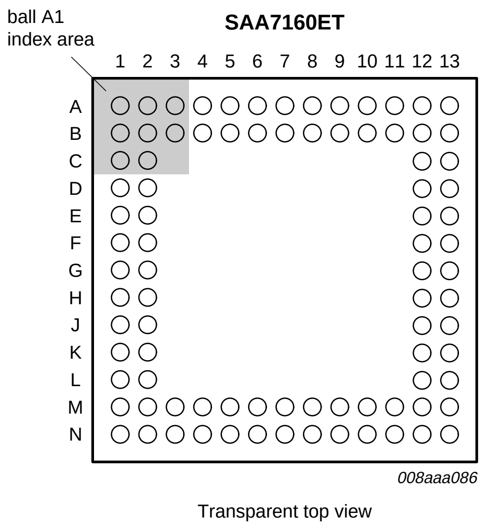


Fig 4. Pin configuration for TFBGA88

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2_VS _SOP	P2_HS	P2_CLK	P6_VAL	P6_VS _SOP	P6_CLK	P6_6	P6_3	P6_1	P6_0	I2S_SCK_A	I2S_SD0_A	I2S_SD1_A
B	P2_7	V_{DDDE1} (3V3)	V_{SS}	V_{SS}	V_{DDDE3} (3V3)	P6_HS	P6_7	V_{SS}	P6_5	P6_4	P6_2	V_{SS}	I2S_WS_A
C	P2_6	V_{DDDI} (1V25)										V_{DDDI} (1V25)	GPIO_17
D	P2_5	V_{DDDI} (1V25)										V_{DDDE2} (3V3)	GPIO_16
E	P2_4	P2_3										V_{SS}	P2_VAL
F	P2_2	V_{SS}										TEST1	GPIO_2
G	P2_1	I2S_SD1_B										GPIO_3	GPIO_4
H	I2S_WS_B	P2_0										GPIO_5	GPIO_6
J	I2S_SCK_B	V_{DDDE1} (3V3)										V_{SS}	GPIO_14
K	I2S_SD0_B	SCL_B										V_{DDDI} (1V25)	$V_{DDDI(1V25)}$/ TEST
L	SDA_A	SCL_A										GPIO_15	GPIO_26
M	SDA_B	V_{SS}	V_{SS}	$V_{DDD(PCI)}$ (1V0)	PCI_PVT	PCI_RESN	V_{SS}	TRSTN	TCK	TDO	BOOT_1	TMS	GPIO_20
N	PCI_PER _P0	PCI_PER _N0	$V_{DDA(PCI)}$ (3V3)	PCI_PET _P0	PCI_PET _N0	$V_{DDD(PCI)}$ (1V25)	PCI_REF CLKP	PCI_REF CLKN	TDI	SPI_CLK	SPI_MA_SL	SPI_SL_MA	BOOT_0

008aaa088

Fig 5. Pin configuration (TFBGA88 top view) for SAA7160ET

5.2.2 Pin description

Table 5. Description of functional pins

Symbol	Pin	Type[1]	Description
SCL_A	L2	IO	I^2C-bus clock of first I^2C-bus interface
SDA_A	L1	IO	I^2C-bus data of first I^2C-bus interface
I2S_SD0_A	A12	IO	I^2S-bus port A: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
I2S_WS_A	B13	IO	I^2S-bus port A: digital audio input signal for • I2S_WS word select line of Inter IC Sound bus serial interconnect format
I2S_SCK_A	A11	I	I^2S-bus port A: digital audio input signal for • I2S_SCK bit clock of Inter IC Sound bus serial interconnect format
I2S_SD1_A	A13	IO	I^2S-bus port A: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
P2_0	H2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV UV[9:0] bit 2 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 0 – program stream data of PS2[7:0] bit 0
P2_1	G1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV UV[9:0] bit 3 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 1 – program stream data of PS2[7:0] bit 1
P2_2	F1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV UV[9:0] bit 4 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 2 – program stream data of PS2[7:0] bit 2
P2_3	E2	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV UV[9:0] bit 5 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 3 – program stream data of PS2[7:0] bit 3

Table 5. Description of functional pins *…continued*

Symbol	Pin	Type[1]	Description
P2_4	E1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV UV[9:0] bit 6 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 4 – program stream data of PS2[7:0] bit 4
P2_5	D1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV UV[9:0] bit 7 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 5 – program stream data of PS2[7:0] bit 5
P2_6	C1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV UV[9:0] bit 8 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 6 – program stream data of PS2[7:0] bit 6
P2_7	B1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV UV[9:0] bit 9 2. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2[7:0] bit 7 – program stream data of PS2[7:0] bit 7
P2_CLK	A3	ID	1. digital input signal of FGPI_2 or FGPI_3 for parallel – transport stream clock of TS2 – program stream clock of PS2 2. digital input signal of VIP_1, FGPI_2 or FGPI_3 for clock signal of parallel video data
P2_HS	A2	ID	digital input signal of VIP_1, FGPI_2 or FGPI_3 for • horizontal synchronization of digital video port • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV UV[9:0] bit 0

Table 5. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P2_VS_SOP	A1	ID	1. digital input signal of VIP_1, FGPI_2 or FGPI_3 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV UV[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal ‘start of package’ of FGPI_2 or FGPI_3 for parallel – transport stream data of TS2 – program stream data of PS2
P2_VAL	E13	ID	digital input control signal ‘valid data’ of FGPI_2 or FGPI_3 for parallel • transport stream data of TS2 • program stream data of PS2 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
P6_0	A10	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 0 – STV YUV[9:0] bit 2 – HDTV Y[9:0] bit 2 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 0 – program stream data of PS6[7:0] bit 0
P6_1	A9	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 1 – STV YUV[9:0] bit 3 – HDTV Y[9:0] bit 3 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 1 – program stream data of PS6[7:0] bit 1
P6_2	B11	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 2 – STV YUV[9:0] bit 4 – HDTV Y[9:0] bit 4 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 2 – program stream data of PS6[7:0] bit 2
P6_3	A8	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 3 – STV YUV[9:0] bit 5 – HDTV Y[9:0] bit 5 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 3 – program stream data of PS6[7:0] bit 3

Table 5. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P6_4	B10	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 4 – STV YUV[9:0] bit 6 – HDTV Y[9:0] bit 6 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 4 – program stream data of PS6[7:0] bit 4
P6_5	B9	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 5 – STV YUV[9:0] bit 7 – HDTV Y[9:0] bit 7 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 5 – program stream data of PS6[7:0] bit 5
P6_6	A7	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 6 – STV YUV[9:0] bit 8 – HDTV Y[9:0] bit 8 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 6 – program stream data of PS6[7:0] bit 6
P6_7	B7	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for parallel video data modes – STV YUV[7:0] bit 7 – STV YUV[9:0] bit 9 – HDTV Y[9:0] bit 9 2. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6[7:0] bit 7 – program stream data of PS6[7:0] bit 7
P6_CLK	A6	ID	1. digital input signal of FGPI_0 or FGPI_1 for parallel – transport stream clock of TS6 – program stream clock of PS6 2. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – clock signal for parallel video data modes
P6_HS	B6	ID	digital input signal of VIP_0, FGPI_0 or FGPI_1 for • parallel video data mode STV YUV[9:0] bit 0 • parallel video data mode HDTV Y[9:0] bit 0 • horizontal synchronization reference in 8-bit STV mode

Table 5. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
P6_VS_SOP	A5	ID	1. digital input signal of VIP_0, FGPI_0 or FGPI_1 for – parallel video data mode STV YUV[9:0] bit 1 – parallel video data mode HDTV Y[9:0] bit 1 – vertical synchronization reference in 8-bit STV mode 2. digital input signal ‘start of package’ of FGPI_0 or FGPI_1 for parallel – transport stream data of TS6 – program stream data of PS6
P6_VAL	A4	ID	digital input control signal ‘valid data’ of FGPI_0 or FGPI_1 for parallel • transport stream data of TS6 • program stream data of PS6 If this pin is unused it is necessary to connect the pin to 3.3 V supply voltage.
GPIO_2	F13	IOU	GPIO: programming control port signal for • general purpose input/output port 2 • external interrupt 2; interrupt edge sensitive with programmable edge polarity
GPIO_3	G12	IOU	GPIO: programming control port signal for • general purpose input/output port 3 • external interrupt 3; interrupt edge sensitive with programmable edge polarity
GPIO_4	G13	IOU	GPIO: programming control port signal for • general purpose input/output port 4 • external interrupt 4; interrupt edge sensitive with programmable edge polarity
GPIO_5	H12	IOU	GPIO: programming control port signal for • general purpose input/output port 5 • external interrupt 5; interrupt edge sensitive with programmable edge polarity
GPIO_6	H13	IOU	GPIO: programming control port signal for • general purpose input/output port 6 • external interrupt 6; interrupt edge sensitive with programmable edge polarity
GPIO_14	J13	IOU	GPIO: programming control port signal for • general purpose input/output port 14 • external interrupt 14; interrupt edge sensitive with programmable edge polarity
GPIO_15	L12	IOU	GPIO: programming control port signal for • general purpose input/output port 15 • external interrupt 15; interrupt edge sensitive with programmable edge polarity
GPIO_16	D13	IOU	GPIO: programming control port signal for • general purpose input/output port 16 • PHI chip select to other external devices (active LOW)
GPIO_17	C13	IOU	GPIO: programming control port signal for • general purpose input/output port 17 • PHI chip select to other external devices (active LOW)
GPIO_20	M13	IOU	GPIO: programming control port signal for • general purpose input/output port 20 • PHI chip select to other external devices (active LOW)
GPIO_26	L13	IOU	GPIO: programming control port signal for • general purpose input/output port 26

Table 5. Description of functional pins *...continued*

Symbol	Pin	Type[1]	Description
BOOT_0	N13	IOU	GPIO: programming control port signal for • general purpose input/output port 30 • boot mode GPIO_[31:30] bit 0
BOOT_1	M11	IOU	GPIO: programming control port signal for • general purpose input/output port 31 • boot mode GPIO_[31:30] bit 1
PCI_PER_P0	N1	AI	PCI Express differential receive data input 0 (positive)
PCI_PER_N0	N2	AI	PCI Express differential receive data input 0 (negative)
PCI_PET_P0	N4	AO	PCI Express differential transmit data output 0 (positive)
PCI_PET_N0	N5	AO	PCI Express differential transmit data output 0 (negative)
PCI_REFCLKP	N7	AI	PCI Express clock 100 MHz differential input (positive)
PCI_REFCLKN	N8	AI	PCI Express clock 100 MHz differential input (negative)
PCI_PVT	M5	AI	this signal is used to create a compensation signal internally which will adjust the IO pads' characteristics as PVT drifts; connect 33 Ω resistor to $V_{DDD(PCI)(1V25)}$
PCI_RESN	M6	ID	system reset (active LOW)
TRSTN	M8	IU	JTAG test reset input: drive HIGH for normal operation
TCK	M9	IU	JTAG test clock input
TMS	M12	IU	JTAG test mode select
TDO	M10	O	JTAG test serial data output
TDI	N9	IU	JTAG test serial data input
SPI_CLK	N10	IU	SPI clock
SPI_MA_SL	N11	IOU	SPI; transfer serial data from master to slave (slave data input or master data output)
SPI_SL_MA	N12	IOU	SPI; transfer serial data from slave to master (master data input or slave data output)
TEST1	F12	ID	enable test mode 1; must be connected to V_{SS}
SCL_B	K2	IO	I^2C-bus clock of second I^2C-bus interface (interface can be used for boot EEPROM)
SDA_B	M1	IO	I^2C-bus data of second I^2C-bus interface (interface can be used for boot EEPROM)
I2S_SD0_B	K1	IO	I^2S-bus port B: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
I2S_SD1_B	G2	IO	I^2S-bus port B: digital audio input signal for • I2S_SD serial data line of Inter IC Sound bus serial interconnect format
I2S_WS_B	H1	IO	I^2S-bus port B: digital audio input signal for • I2S_WS word select line of Inter IC Sound bus serial interconnect format
I2S_SCK_B	J1	I	I^2S-bus port B: digital audio input signal for • I2S_SCK bit clock of Inter IC Sound bus serial interconnect format

[1] The pin types are defined in Table 3.

Table 6. Supply pins

Symbol	Pin	Description
3.3 V IO supply voltage		
$V_{DDE1(3V3)}$	B2, J2	digital extend supply voltage 1 (3.3 V)
$V_{DDE2(3V3)}$	D12	digital extend supply voltage 2 (3.3 V)
$V_{DDE3(3V3)}$	B5	digital extend supply voltage 3 (3.3 V)
3.3 V analog supply voltage		
$V_{DDA(PCI)(3V3)}$	N3	PCI Express analog supply voltage (3.3 V)
1.0 V IO supply voltage		
$V_{DDD(PCI)(1V0)}$	M4	PCI Express digital supply voltage (1.0 V)
1.25 V core supply voltage		
$V_{DDI(1V25)}$	C2, C12, D2, K12	digital internal supply voltage (1.25 V)
$V_{DDI(1V25)}$/TEST	K13	digital internal supply voltage (1.25 V) and power start-up test input; must be connected to 1.25 V
$V_{DDD(PCI)(1V25)}$	N6	PCI Express digital supply voltage (1.25 V)
Ground supply voltage		
V_{SS}	B3, B4, B8, B12, E12, F2, J12, M2, M3, M7	ground supply voltage

6. Functional description

6.1 DVI

The video input processing is responsible for capturing and processing the different video input streams. After capturing and processing the data streams, the VIP transfers the data via multiple DMA channels to the PCI Express bus. The processor supports data tagging to indicate to the system when a certain amount of data (e.g. a video frame) has been transferred to the PCI Express core. Figure 6 shows the functional block diagram of the VIP. The video input module contains the following submodules:

- 2 × VIP, used for SD or HD video capture (YUV 4 : 2 : 2)
- 4 × FGPI, used for SD video capture (YUV 4 : 2 : 2) or TS/PS

Features:

- Independent digital video inputs in YUV (8-bit or 10-bit)

The DVI interface supports the following signal formats as inputs.

- STV: ITU-R BT.656, ITU-R BT.601, VIP (VESA)
- Progressive: ITU-R BT.1358, SMPTE 293M-1996 (480p)
- HDTV: SMPTE 274-1998 (1080i, 4, 5), SMPTE 296M-1997 (720p)

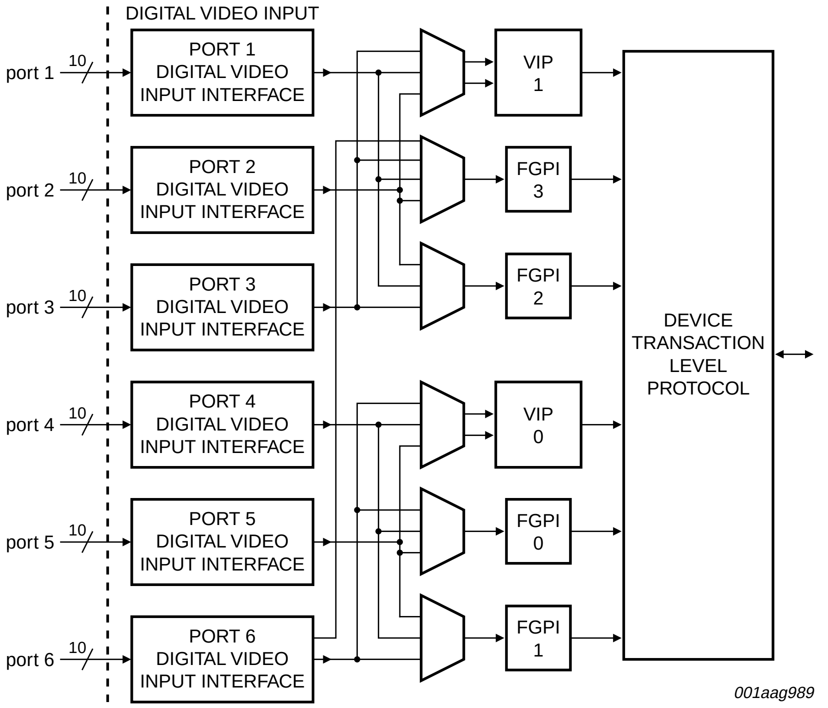


Fig 6. DVI system

The input modules can be used in different combinations. The SAA7160E supports up to a maximum of six simultaneous streams (e.g. six SD video streams, or four TS/PS streams, or a combination of both). HD support is limited to one stream.

The SAA7160ET supports up to two simultaneous streams (e.g. two SD video streams, two TS/PS streams, or a combination of both) and one HD stream.

In order to support all the possible use cases, six 10-bit wide input ports (port 1, port 2, port 3, port 4, port 5, port 6) are required. The SAA7160E supports all six ports. The SAA7160ET supports two ports only (port 2 and port 6).

Table 7 describes the combination of the video input modes.

The routing of the video input ports to the video input processors is implemented by a multiplexer. The multiplexer is implemented such that each video input port drives VIP or FGPI. The HD support is wired to two internal ports for VIP 0 and VIP 1 respectively.

The video input multiplexer takes care of routing the video input ports to the VIP and the FGPI. The video input multiplexer includes one multiplexer for routing the VIP to the video input processor and another one for routing the input ports to the FGPI.

Each 10-bit wide video input port can be used for capturing a single SD or TS/PS stream, or two ports can be combined to capture an HD stream. Dependent on the stream type, the port bits may serve a different purpose. Input streams can be either 8-bit or 10-bit wide, and in case of 8-bit wide input streams the two LSBs of the video input port may be used for the horizontal and vertical synchronization signals (href and vref).

Table 7. Example of digital video input pin groups

Function	Digital video data input pin groups																																			
Digital pin groups	digital input port 1[1]					digital input port 2					port 1 and port 2[1]			digital input port 3[1]					digital input port 4[1]					digital input port 5[1]					port 4 and port 5[1]			digital input port 6				
Digital input 4 × TS and 2 × STV YUV[7:0]	TS[7:0]	SOP	CLK	VAL		STV YUV[7:0]	VS	CLK		HS				TS[7:0]	SOP	CLK	VAL		TS[7:0]	SOP	CLK	VAL		STV YUV[7:0]	VS	CLK		HS				TS[7:0]	SOP	CLK	VAL	
Digital input 4 × TS and 2 × STV YUV[7:0]	STV YUV[7:0]	VS	CLK		HS	TS[7:0]	SOP	CLK	VAL					TS[7:0]	SOP	CLK	VAL		STV YUV[7:0]	VS	CLK		HS	TS[7:0]	SOP	CLK	VAL					TS[7:0]	SOP	CLK	VAL	
Digital input 4 × TS and 2 × STV YUV[7:0]	TS[7:0]	SOP	CLK	VAL		TS[7:0]	SOP	CLK	VAL					STV YUV[7:0]	VS	CLK		HS	TS[7:0]	SOP	CLK	VAL		TS[7:0]	SOP	CLK	VAL					STV YUV[7:0]	VS	CLK		HS
Digital input 4 × TS and 2 × STV YUV[9:0]	TS[7:0]	SOP	CLK	VAL		STV YUV[9:2]	YUV1	CLK		YUV0				TS[7:0]	SOP	CLK	VAL		TS[7:0]	SOP	CLK	VAL		STV YUV[9:2]	YUV1	CLK		YUV0				TS[7:0]	SOP	CLK	VAL	
Digital input 4 × TS and 2 × STV YUV[9:0]	STV YUV[9:2]	YUV1	CLK		YUV0	TS[7:0]	SOP	CLK	VAL					TS[7:0]	SOP	CLK	VAL		STV YUV[9:2]	YUV1	CLK		YUV0	TS[7:0]	SOP	CLK	VAL					TS[7:0]	SOP	CLK	VAL	
Digital input 4 × TS and 2 × STV YUV[9:0]	TS[7:0]	SOP	CLK	VAL		TS[7:0]	SOP	CLK	VAL					STV YUV[9:2]	YUV1	CLK		YUV0	TS[7:0]	SOP	CLK	VAL		TS[7:0]	SOP	CLK	VAL					STV YUV[9:2]	YUV1	CLK		YUV0
Digital input 2 × TS and 1 × HDTV YUV[9:0][2]	HDTV Y[9:2]	Y1	CLK		Y0	HDTV UV[9:2]	UV1	CLK		UV0	HS	VS	FRE	-					HDTV Y[9:2]	Y1	CLK		Y0	HDTV UV[9:2]	UV1	CLK		UV0	HS	VS	FRE	-				
Digital input 2 × TS and 1 × HDTV YUV[9:0][3]	-					HDTV UV[9:2]	UV1	CLK		UV0				-					-					-								HDTV Y[9:2]	Y1	CLK		Y0

[1] Input port not available in SAA7160ET.

[2] SAA7160E combination port 1 and port 2 or port 4 and port 5.

[3] SAA7160ET only.

6.1.1 DMA byte alignment

The DMA byte alignment module implements the byte address alignment for each of the DMA channels coming from the AV input modules. The module addresses alignment with byte granularity in an entire 4 kB page.

The main features are:

- Byte address alignment for DTL-MMSD streams
  - Address alignment within 4 kB page (0 B to 4095 B)
- Support for multiple buffering
  - Maximum 8 memory buffers (8 address offset registers per DMA channel)
- Support for 12 DMA channels
  - 2 × 3 VIP (data width is 64 bit)
  - 4 × 1 FGPI
  - 2 × 1 AI

Based on the current buffer number the module selects the correct address offset register. It implements 8 address offset registers per DMA channel to support multiple buffering.

The memory buffer handling supports up to 8 buffers per DMA channel. The (byte) address alignment for the different buffers is the same, and hence the module implements 8 address offset registers per DMA channel such that each buffer can have a different address alignment.

6.2 Message signal interrupt

The MSI logic is responsible for generating the MSI messages. MSI is a native feature in PCI Express that enables a device to request a service by writing an interrupt event. The write transaction address specifies the MSI message destination and the write transaction data specifies the message including a message ID.

The main features of the MSI logic are:

- MSI capability
  - 32 different messages
  - Programmable ID in MSI message data field
  - Programmable MSI message address field
- Programmable MSI delay timer
- Support for the following interrupt sources:
  - DMA channel acknowledge interrupts (12 ×)
  - DMA channel overflow interrupts (12 ×)
  - AV interrupts (8 ×)
  - I^2C-bus interrupts (2 ×)
  - External interrupts from GPIO (16 ×)
  - All interrupts edge sensitive with programmable edge polarity
- Support for interrupt masking (i.e. enable/disable)

- Support for INT_A emulation

During device configuration, system software reads the capability list of the logic core to find out whether it supports MSI, and if yes how many different MSI messages it is requesting. Using the multiple message feature allows a PCI Express device to give different MSI messages a unique message ID.

The maximum number of requested MSI messages is 32 and must be aligned to a power of two (1, 2, 4, 8, 16 or 32). The PCI Express core will be configured for 32 requested messages (i.e. before device configuration). After reading the capability list, system software initializes the following parameters:

- MME field

  Defines the number of granted messages, which is either all 32 or a subset of the number of requested messages.
- MSI message destination address

  Defines the (physical) message destination address for MSI messages.
- MSI message data

  Defines the message data for MSI messages.

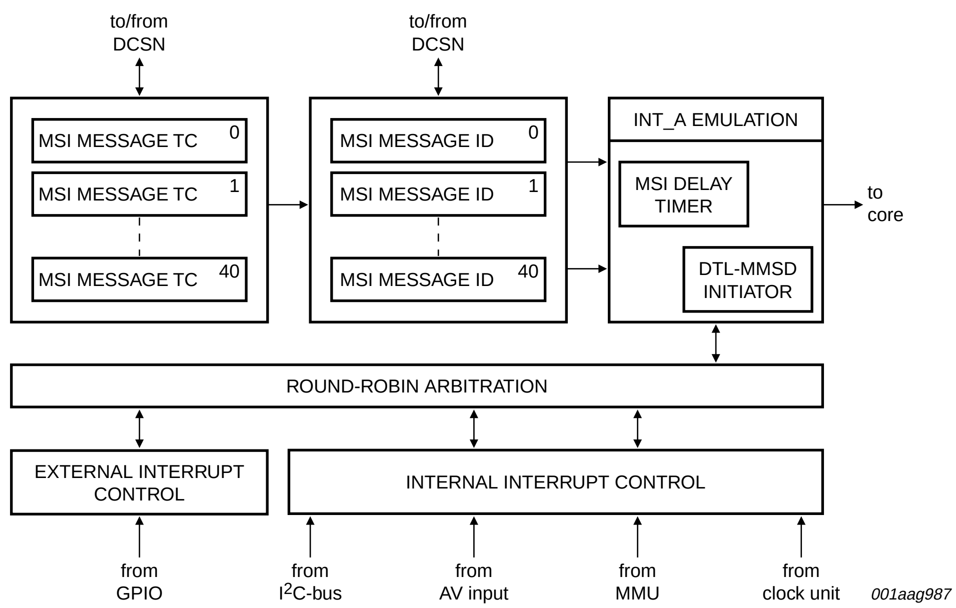


Fig 7. Block diagram MSI

MSI messages can be generated for one of the following events:

- DMA channel interrupts

  Two types of DMA channel interrupts are available:
  - Acknowledge interrupt

    Indicates a tagged write data element (last data element of a buffer) in the corresponding DMA channel.

- Overflow interrupt

  Indicates that a buffer overflow has occurred in the corresponding DMA channel. It should be noted that overflow interrupts are only generated for the AV DMA channels (i.e. DMA channel 1 to 12).

- Unmapped TC interrupt

  The unmapped TC interrupt indicates the MMU dropped data packet with unmapped TC.

- AV interrupts

  An AV interrupt indicates an interrupt event in the associated AV input (i.e. VIP, FGPI or AI). An AV interrupt remains asserted HIGH until the interrupt status has been cleared.

- External interrupts from GPIO

  External interrupts are assumed to be edge sensitive with programmable edge polarity (i.e. rising and falling edge). Furthermore, external interrupts are assumed to be asynchronous to the MSI clock domain and are synchronized internally before they are actually being used. This imposes the constraint that an external interrupt must be kept asserted for at least three MSI clock cycles to ensure proper synchronization.

In the event of simultaneous interrupts only one interrupt request can be served at the same time.

6.3 Memory management unit

The MMUs' main task is to translate the virtual, logical addresses of the DMA data packet into the physical addresses that are used by the operating system. The virtual address space is 32 bit, while the physical address space is 64 bit.

The main features of the MMU are:

- Logical to physical address mapping
  - 32-bit logical address
  - 64-bit physical address: for legacy systems with 32-bit addressing, can be selected for MMU physical address requirements
  - Support for 12 DMA channels
- Support for multiple buffering
  - Managing address transfer for 8 buffer DMA handling
  - Maximum 8 memory buffers => 8 page table addresses per DMA channel => 12×8 PTA
- Support for buffer sizes larger than 2 MB
- Support pre-fetching from page table to reduce latency
  - 8 page table entries for 64-bit addressing

The virtual to physical address mapping is defined by the operating system using so-called page tables. A page table is a 4 kB space in system memory. Each entry in a page table contains the physical base address for 4 kB page of contiguous memory.

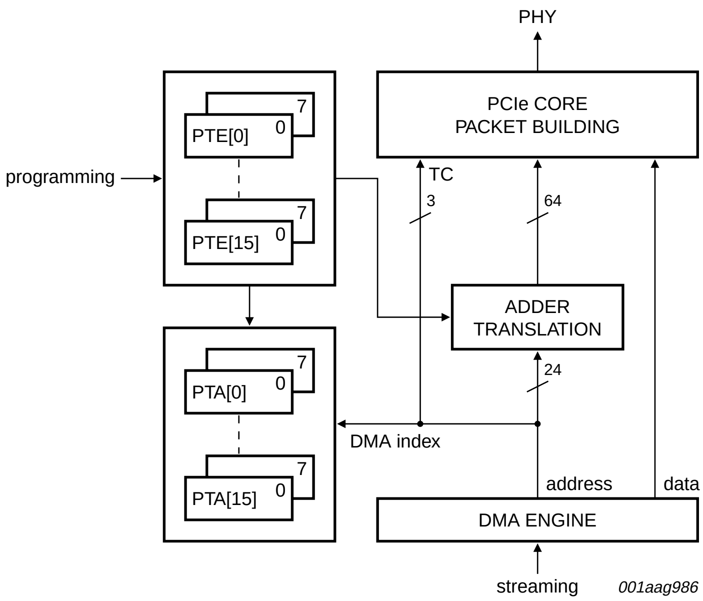


Fig 8. Block diagram MMU

Once the address mapping has been completed the data packet is forwarded to the PCI Express core. The routing of the data packet is dependent on the traffic class of the data packet.

6.3.1 Logical to physical address mapping

The logical to physical address mapping is defined by page tables. A page table is 4 kB large and 4 kB aligned space in system memory. Each entry in a page table contains the physical base address for 4 kB of contiguous memory (i.e. one page). With 64-bit addressing each page table contains 4096 / 8 = 512 entries. Hence, one 4 kB page table defines the virtual to physical addressing mapping for a memory buffer with a maximum size of 2 MB.

The incoming data packet originates from one out of 12 DMA channels. For each DMA channel at least one PTA is needed. Although the MMU allows to enable only one buffer per DMA channel. In order to prevent potential audio and/or video artifacts when host SW and AV input module are accessing the same buffer space in system memory, a minimum of two buffers (i.e. double buffering) is required. In order to select the correct PTA the MMU needs to know from which stream channel the data packet originates.

Based on the DMA channel number and buffer number, the MMU knows which page table to use.

6.3.2 Multiple buffer support

The SW is able to support up to 8 buffers per DMA channel. Hence, the MMU is able to support up to 8 PTAs per DMA channel.

Based on the DMA channel number the MMU knows which set of PTAs’ to use. The correct PTA within a set of eight of PTAs is selected using the current memory buffer number.

When switching from current memory buffer to the next memory buffer, the entire set of pre-fetched page table entries needs to be updated. If we were to update the set of pre-fetched page table entries based on the memory buffer number that is encoded in the virtual DMA address. The MMU takes some time to fetch the new page table entries from system memory.

6.3.3 Large buffer support

The MMU supports up to 16 virtual DMA channel numbers while only 12 physical DMA channels are implemented. Hence, even in a scenario with all 12 DMA channels used, and 3 DMA channel numbers are available for supporting buffers that are larger than 2 MB.

6.4 Programming and controlling parts

The SAA7160E can be separated into 6 programming controlling parts. The SAA7160ET supports 5 programming controlling parts.

- PCI Express interface
- PHI (not in SAA7160ET)
- SPI
- GPIO interface
- I^2C-bus interfaces
- IRQ

6.4.1 PCI Express interface

The PCI Express subsystem is separated in the PHY (electrical layer) and the PCI Express core circuit.

The function of the PHY is to connect a chip with another chip. A data link can be established when two PHYs are connected to each other through a cable or a metal trace on a PCB. The PHY includes a receiver and transmitter interface.

The main function of the PHY is to convert digital data into electrical signals and vice versa.

The SAA7160 features a native PCI Express single lane (× 1) link compliant to PCI Express Base Specification 1.0a.

The PCI Express link consists of a differential input and a differential output pair. The data rate of these signals is 2.5 Gbit/s (× 1 configuration).

6.4.1.1 Receiving data

Incoming data enters the chip at the pins PCI_PER_N0 and PCI_PER_P0. The receiver converts these signals from small amplitude differential signals into rail-to-rail digital signals.

6.4.1.2 Transmitting data

The PHY transmits 8-bit data. This data is encoded using an 8-bit to 10-bit encoding algorithm. The 2-bits overhead of the 8-bit to 10-bit encoding ensures the serial data will be balanced and has a minimum frequency of data changes (needed for recovery).

The parallel-to-serial converter serializes the 10-bits data into serial data streams. These data streams are latched into the transmitter, where they are converted into small amplitude differential signals. The transmitter has built-in de-emphasis for a larger eye opening in the received data.

6.4.1.3 Clocking

The pins PCI_REFCLKN and PCI_REFCLKP are 100 MHz external reference clock inputs that the PHY uses to generate the 250 MHz data clock and the internal bit rate clock. This clock may have spread spectrum modulation that matches a system reference clock.

6.4.2 PHI

The PHI supports the next generation of multimedia platforms with modern microcontrollers or other peripheral devices, like e.g. MPG encoder.

The PHI interface provides the following features to control the external peripheral devices:

- Bidirectional 16-bit wide address/data bus
- Support read/write function
- Support wait states, handshake handling with RDY signals

The interface supports two kinds of operating modes. The PHI operating mode defines how address and data will be mapped onto the 16-bit PHI address/data bus.

- SRAM mode (address and data multiplexed)

  In the SRAM mode address and read/write data are transferred across the 16-bit PHI address/data bus. The transfer are 32-bit data with 16-bit address.
  - 32-bit data read from 16-bit address (1 × address cycle + 2 × data cycle)
  - 32-bit data write to 16-bit address (1 × address cycle + 2 × data cycle)
- FIFO mode (data only)

  For FIFO based devices the SAA7160E supports the FIFO mode in which only data is transferred across the 16-bit PHI address/data bus. In the FIFO mode each transfer consists of two data cycles.
  - 32-bit data read (2 × data cycle)
  - 32-bit data write (2 × data cycle)

6.4.3 SPI

The SPI operates in a master mode. The interface is compliant with the Motorola SPI specification. This interface can be used in an application where a master, slave or combined master and slave SPI is required.

The SPI master mode interface can access external SPI slave interfaces. Each external slave interface has its own slave device select input signal via the GPIO pin. This signal must be driven LOW to indicate to the slave interface that it is currently selected. The corresponding GPIO signal must be asserted LOW before data transaction begins and stays LOW for duration of the transfer. The main features of the master SPI are:

- Synchronous serial full duplex communication
  - 32 bit is the maximum data bit rate of ⅛ of the input clock
- Compliant with Motorola SPI specification
- Maximum data bit rate is ⅛ of the input clock rate

The SPI is a serial full duplex interface. It is designed to be able to handle multiple masters and slaves being connected to a given instantiation of the interface. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave and the slave always sends a byte of data to the master.

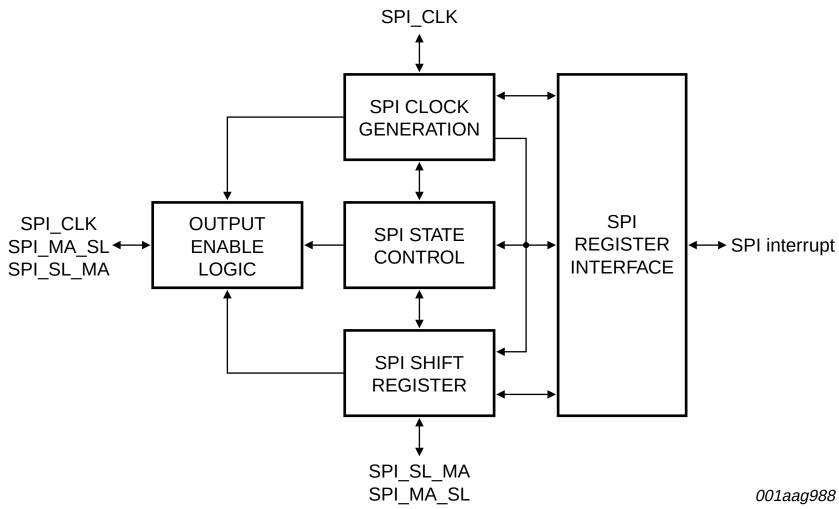


Fig 9. Block diagram SPI

6.4.4 GPIO interface

The GPIO interface of the SAA7160E provides 32 GPIOs and of the SAA7160ET provides 13 GPIOs. A set of registers is available to control the function of the GPIOs.

The following table describes the application purposes of the GPIO pins.

- GPIO_[15:1]: interrupts from other external devices
- GPIO_[23:16]: chip select to other external devices
- GPIO_[29:26]: general purpose
- BOOT_0 and BOOT_1: boot mode. The boot mode pins can be used as application GPIO pins after 500 µs (after power-up). The boot mode has been latched.

6.4.5 I²C-bus interface

Both types SAA7160E and SAA7160ET support two I²C-bus master interfaces. All interfaces are developed according the ‘fast mode’ I²C-bus specification extension (data rate up to 400 kbit/s). The pins for the different I²C-bus interfaces are:

- Pins SCL_A and SDA_A: pins for first master/slave and second master/slave I^2C-bus interfaces
- Pins SCL_B and SDA_B: pins for third and fourth master/slave I^2C-bus interfaces, provide for external boot EEPROM

The external boot EEPROM will be connected to the pins SDA_B and SCL_B. This interface allows only to support multiple masters on the I^2C-bus after the boot sequence is completed.

The main features of the I^2C-bus interfaces are:

- I^2C-bus multiple master programmable via internal configuration bus
- I^2C-bus slave to access programmable control bytes
- Programmable I^2C-bus sequencer to ease and accelerate I^2C-bus sequence generated by the I^2C-bus master
- Free programmable slave address
- Bidirectional data transfer between masters and slaves
- Multiple master I^2C-bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the I^2C-bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial I^2C-bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer

The two I^2C-bus multiple master interface circuits provide serial interfaces which meets the I^2C-bus specification and support all transfer modes from and to the I^2C-bus.

The I^2C-busses support the following functionality:

- The normal mode (100 kHz) and the fast mode (400 kHz)
- Interrupt generation on received or sent byte
- It has four modes of operation: master transmitter, master receiver, slave transmitter and slave receiver

The I^2C-bus is a multiple master bus. More than one master I^2C-bus device can be connected to the bus and it is possible to have data transfers at the same time. A collision detect scheme is used to arbitrate between the multiple masters and select a single master of the bus at any given time. If two or more masters try to put information onto the bus, the first to produce a logic 1 when the other produces a logic 0 will detect the collision and back-off transferring information on the bus.

The clock signals during arbitration are a synchronized through combination of the clocks generated by the I^2C-bus master circuits via the SCL lines. Two wires, SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I^2C-bus. Each device can operate as either a transmitter or receiver and as a master or a slave, depending on the function of the device. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer.

Any device addressed by a master is considered a slave. Generation of clock signals on the I²C-bus is always the responsibility of the master device; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave device holding down the clock line or by another master when arbitration occurs.

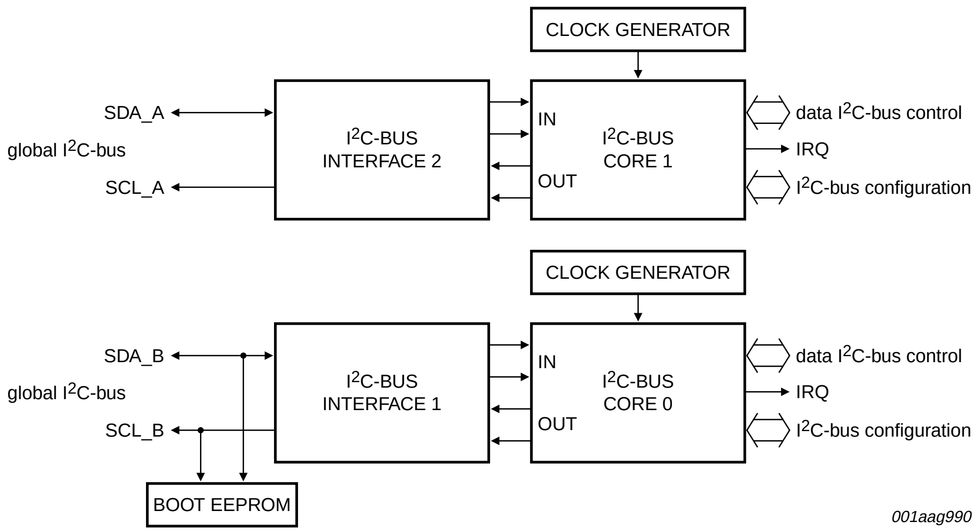


Fig 10. I²C-bus structure overview

6.5 I²S-bus input interface

The SAA7160 has two independent audio slave interface circuits for serial input of digital audio data streams. The audio interface circuits are based on the I²S-bus standard but can be configured to several data and timing formats (with respect to framing, bit clock and synchronization).

List of key features:

- Supports I²S-bus, LSB and MSB justified formats
- Sample size up to 32 bit
- Standard stereo I²S-bus (MSB first, 1-bit delay from word select, left and right data in a frame)
- LSB first with 1-bit to 32-bits data per channel
- Raw sample mode where the serial data for each active serial channel is sampled at each sampling clock edge along with the word-select signal

Each of the slave I²S-bus interfaces consists two data lines, a word select line and a serial clock line. The word select line distinguishes between the left and the right channel information of the data lines. It is possible to sample up to 32 bits per channel, and there are 4 channels on each module available.

The following block diagram shows the structure of the different I²S-bus interfaces.

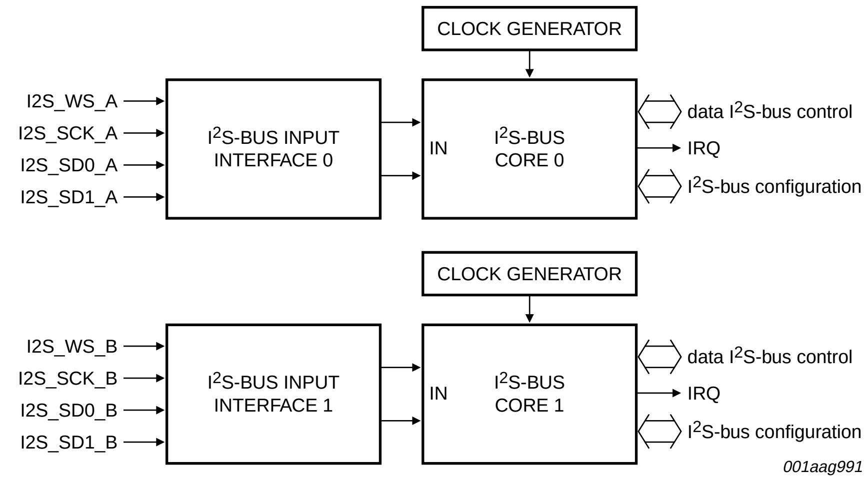


Fig 11. I²S-bus structure overview

Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock, word-select signal and data.

The serial data inputs are sampled under the serial clock and the word-select signal will be converted into parallel words of 32 bits width.

7. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and all corresponding supply pins connected together.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(PCI0)(3V3)}$	PCI Express 0 analog supply voltage (3.3 V)		–0.5	+4.5	V
$V_{DDA(PCI1)(3V3)}$	PCI Express 1 analog supply voltage (3.3 V)		–0.5	+4.5	V
$V_{DDA(PCI)(3V3)}$	PCI Express analog supply voltage (3.3 V)		–0.5	+4.5	V
$V_{DDE1(3V3)}$	digital extend supply voltage 1 (3.3 V)		–0.5	+4.5	V
$V_{DDE2(3V3)}$	digital extend supply voltage 2 (3.3 V)		–0.5	+4.5	V
$V_{DDE3(3V3)}$	digital extend supply voltage 3 (3.3 V)		–0.5	+4.5	V
$V_{DDI1(1V25)}$	digital internal supply voltage 1 (1.25 V)		–0.5	+1.7	V
$V_{DDI2(1V25)}$	digital internal supply voltage 2 (1.25 V)		–0.5	+1.7	V
$V_{DDI(1V25)}$	digital internal supply voltage (1.25 V)	includes pin $V_{DDI(1V25)}$/TEST	–0.5	+1.7	V
$V_{DD(PCI0)(1V25)}$	PCI Express 0 digital supply voltage (1.25 V)		–0.5	+1.7	V
$V_{DD(PCI1)(1V25)}$	PCI Express 1 digital supply voltage (1.25 V)		–0.5	+1.7	V
$V_{DD(PCI)(1V25)}$	PCI Express digital supply voltage (1.25 V)		–0.5	+1.7	V
$V_{DD(PCI0)(1V0)}$	PCI Express 0 digital supply voltage (1.0 V)		0.85	1.15	V
$V_{DD(PCI1)(1V0)}$	PCI Express 1 digital supply voltage (1.0 V)		0.85	1.15	V
$V_{DD(PCI)(1V0)}$	PCI Express digital supply voltage (1.0 V)		0.85	1.15	V
V_i	input voltage		–0.5	V_{DD} + 0.5	V
T_{stg}	storage temperature		–40	+125	°C

Table 8. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and all corresponding supply pins connected together.

Symbol	Parameter	Conditions		Min	Max	Unit
T_{amb}	ambient temperature			0	70	°C
V_{esd}	electrostatic discharge voltage	human body model	[1]	-	±2000	V
		charged-device model	[2]	-	±500	V

[1] Class 2 according to JESD22-A114.

[2] Class III according to JESD22-C101.

8. Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air			
		SAA7160E	[1]	36	K/W
		SAA7160ET	[1]	63	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

9. Characteristics

Table 10. Characteristics
$V_{DDE1(3V3)} = V_{DDE2(3V3)} = V_{DDE3(3V3)}$ = 3.0 V to 3.6 V; $V_{DDI1(1V25)} = V_{DDI2(1V25)} = V_{DDI(1V25)} = V_{DDD(PCI0)(1V25)} = V_{DDD(PCI1)(1V25)} = V_{DDD(PCI)(1V25)}$ = 1.2 V to 1.3 V; $V_{DDA(PCI0)(3V3)} = V_{DDA(PCI1)(3V3)} = V_{DDA(PCI)(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(PCI0)(1V0)} = V_{DDD(PCI1)(1V0)} = V_{DDD(PCI)(1V0)}$ = 0.9 V to 1.1 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDE1(3V3)}$	digital extend supply voltage 1 (3.3 V)		3.0	3.3	3.6	V
$V_{DDE2(3V3)}$	digital extend supply voltage 2 (3.3 V)		3.0	3.3	3.6	V
$V_{DDE3(3V3)}$	digital extend supply voltage 3 (3.3 V)		3.0	3.3	3.6	V
$V_{DDI1(1V25)}$	digital internal supply voltage 1 (1.25 V)		1.2	1.25	1.3	V
$V_{DDI2(1V25)}$	digital internal supply voltage 2 (1.25 V)		1.2	1.25	1.3	V
$V_{DDI(1V25)}$	digital internal supply voltage (1.25 V)	includes pin $V_{DDI(1V25)}$/TEST	1.2	1.25	1.3	V
$V_{DDD(PCI0)(1V25)}$	PCI Express 0 digital supply voltage (1.25 V)		1.2	1.25	1.3	V
$V_{DDD(PCI1)(1V25)}$	PCI Express 1 digital supply voltage (1.25 V)		1.2	1.25	1.3	V
$V_{DDD(PCI)(1V25)}$	PCI Express digital supply voltage (1.25 V)		1.2	1.25	1.3	V

Table 10. Characteristics *...continued*

$V_{DDE1(3V3)} = V_{DDE2(3V3)} = V_{DDE3(3V3)}$ = 3.0 V to 3.6 V; $V_{DDI1(1V25)} = V_{DDI2(1V25)} = V_{DDI(1V25)} = V_{DDD(PCI0)(1V25)} = V_{DDD(PCI1)(1V25)} = V_{DDD(PCI)(1V25)}$ = 1.2 V to 1.3 V; $V_{DDA(PCI0)(3V3)} = V_{DDA(PCI1)(3V3)} = V_{DDA(PCI)(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(PCI0)(1V0)} = V_{DDD(PCI1)(1V0)} = V_{DDD(PCI)(1V0)}$ = 0.9 V to 1.1 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDD(PCI0)(1V0)}$	PCI Express 0 digital supply voltage (1.0 V)			0.95	1.0	1.05	V
$V_{DDD(PCI1)(1V0)}$	PCI Express 1 digital supply voltage (1.0 V)			0.95	1.0	1.05	V
$V_{DDD(PCI)(1V0)}$	PCI Express digital supply voltage (1.0 V)			0.95	1.0	1.05	V
$V_{DDA(PCI0)(3V3)}$	PCI Express 0 analog supply voltage (3.3 V)			3.1	3.3	3.5	V
$V_{DDA(PCI1)(3V3)}$	PCI Express 1 analog supply voltage (3.3 V)			3.1	3.3	3.5	V
$V_{DDA(PCI)(3V3)}$	PCI Express analog supply voltage (3.3 V)			3.1	3.3	3.5	V
Power dissipation							
P_{tot}	total power dissipation	power management states					
		D0 for typical application		-	330	-	mW
		D0 after reset (not initialized)		-	240	-	mW
Digital inputs (pins P1_[9:0], P1_CLK, P1_VAL, P1_HS, P1_VS_SOP, P2_[9:0], P2_CLK, P2_VS_SOP, P2_HS, P2_VAL, P3_[9:0], P3_CLK, P3_HS, P3_VS_SOP, P3_VAL, P4_[9:0], P4_CLK, P4_VS_SOP, P4_HS, P4_VAL, P5_[9:0], P5_CLK, P5_VAL, P5_VS_SOP, P5_HS, P6_[9:0], P6_CLK, P6_HS, P6_VS_SOP, P6_VAL, SAA7160E: GPIO_[31:26] and GPIO_[23:0] and SAA7160ET: GPIO_31, GPIO_30, GPIO_26, GPIO_20, GPIO_[17:14] and GPIO_[6:2])							
V_{IL}	LOW-level input voltage			–0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage	minimum extend supply voltage $V_{DDE1(3V3)}$, $V_{DDE2(3V3)}$ and $V_{DDE3(3V3)}$		2.4	-	3.6	V
I_{LI}	input leakage current			-	-	10	µA
C_i	input capacitance	I/O at high-impedance		-	-	4	pF
Digital outputs (SAA7160E: pins GPIO_[31:26] and GPIO_[23:0]; SAA7160ET: pins GPIO_31, GPIO_30, GPIO_26, GPIO_20, GPIO_[17:14] and GPIO_[6:2])[1]							
V_{OL}	LOW-level output voltage	for clocks		-	-	0.4	V
		I_{OL} = 3.6 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	for clocks	[2]	V_{DDD} – 0.4	-	-	V
		I_{OH} = –4.5 mA	[2]	V_{DDD} – 0.4	-	-	V
I²C-bus interface; compatible to 3.3 V and 5 V signalling (pins SDA_A, SCL_A, SDA_B and SCL_B)							
f_{bit}	bit rate			0	-	400	kbit/s
V_{IL}	LOW-level input voltage		[3]	–0.5	-	+0.3$V_{CC(I2C-bus)}$	V
V_{IH}	HIGH-level input voltage			0.7$V_{CC(I2C-bus)}$	-	$V_{CC(I2C-bus)}$ + 0.5	V
V_{OL}	LOW-level output voltage	$I_{sink(o)}$ = 3 mA		-	-	0.4	V
PCI Express interface (pins PCI_PER_P0, PCI_PER_N0, PCI_PET_P0, PCI_PET_N0, PCI_REFCLKP and PCI_REFCLKN)							
$f_{clk(ref)}$	reference clock frequency	reference clock spread spectrum: –0.5 % to +0 %		99.97	100	100.03	MHz
f_{mod}	modulation frequency			30	-	33	kHz

Table 10. Characteristics *...continued*

$V_{DDE1(3V3)} = V_{DDE2(3V3)} = V_{DDE3(3V3)}$ = 3.0 V to 3.6 V; $V_{DDI1(1V25)} = V_{DDI2(1V25)} = V_{DDI(1V25)} = V_{DDD(PCI0)(1V25)} = V_{DDD(PCI1)(1V25)} = V_{DDD(PCI)(1V25)}$ = 1.2 V to 1.3 V; $V_{DDA(PCI0)(3V3)} = V_{DDA(PCI1)(3V3)} = V_{DDA(PCI)(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(PCI0)(1V0)} = V_{DDD(PCI1)(1V0)} = V_{DDD(PCI)(1V0)}$ = 0.9 V to 1.1 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{term}	termination resistance	pins PCI_REFCLKP and PCI_REFCLKN	[4]	-	50	-	Ω
V_i	input voltage	pins PCI_REFCLKP and PCI_REFCLKN					
		differential		50	-	-	mV
		single-ended		100	-	-	mV
$V_{I(cm)}$	common-mode input voltage	differential; pins PCI_REFCLKP and PCI_REFCLKN	[5]	0	-	0.6	V
$f_{bit(RX)}$	receiver bit rate			-	2.5	-	Gbit/s
$f_{bit(TX)}$	transmitter bit rate			-	2.5	-	Gbit/s
$t_{TX\_JITTER\_MAX}$	maximum transmitter jitter time			-	-	0.3	UI
$t_{jit(RX)}$	receiver jitter time			-	0.6	-	UI
$t_{r(tx)}$	transmit rise time			-	100	-	ps
$t_{f(tx)}$	transmit fall time			-	100	-	ps
$t_{lock(PLL)(tx)}$	transmit PLL lock time			-	-	50	µs
PHI bus inputs and outputs (pins PHI_WRN, PHI_RDN, PHI_RDY_[3:0] and PHI_ALE, PHI_[15:0]							
$t_{v(Q)}$	data output valid time	PHI_RDN to PHI output data, PHI_RDY_[3:0]		-	-	15	ns
		PHI chip select NOT to PHI output data, PHI_RDY_[3:0]		-	-	10	ns
$t_{PHI\_RDN(min)}$	minimum PHI_RDN time	PHI_RDN to PHI output data, PHI_RDY_[3:0]		3	-	-	ns
$t_{su(i)}$	input set-up time	PHI_WRN to PHI output data		5	-	-	ns
$t_{PHI\_WRN(min)}$	minimum PHI_WRN time	output data changed; PHI output data to PHI_WRN		0	-	-	ns
Digital inputs							
Clock input timing (pins P1_CLK, P2_CLK, P3_CLK, P4_CLK, P5_CLK and P6_CLK)							
T_{cy}	cycle time	HD1 = 75 MHz; HD0 = 54 MHz; STV = 13.5 MHz or 27 MHz		13	-	75	ns
δ	duty factor	for t_{LLCH} / t_{LLC}		40	50	60	%
t_r	rise time			-	-	4	ns
t_f	fall time			-	-	4	ns
Data and control input signals on P1, P2, P3, P4, P5 and P6 ports with respect to P1_CLK, P2_CLK, P3_CLK, P4_CLK, P5_CLK and P6_CLK							
$t_{su(D)}$	data input set-up time			3	-	-	ns
$t_{h(D)}$	data input hold time			0	-	-	ns

Table 10. Characteristics *…continued*

$V_{DDDE1(3V3)} = V_{DDDE2(3V3)} = V_{DDDE3(3V3)}$ = 3.0 V to 3.6 V; $V_{DDDI1(1V25)} = V_{DDDI2(1V25)} = V_{DDDI(1V25)} = V_{DDD(PCI0)(1V25)} = V_{DDD(PCI1)(1V25)} = V_{DDD(PCI)(1V25)}$ = 1.2 V to 1.3 V; $V_{DDA(PCI0)(3V3)} = V_{DDA(PCI1)(3V3)} = V_{DDA(PCI)(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(PCI0)(1V0)} = V_{DDD(PCI1)(1V0)} = V_{DDD(PCI)(1V0)}$ = 0.9 V to 1.1 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TS capture inputs with parallel transport streaming of the ports P1, P2, P3, P4, P5 and P6							
Clock input signal (pins P1_CLK, P2_CLK, P3_CLK, P4_CLK, P5_CLK and P6_CLK)							
T_{cy}	cycle time			-	333	-	ns
δ	duty factor			40	-	60	%
t_r	rise time	20 % V_{DDD} to 80 % V_{DDD}	[2]	-	-	4	ns
t_f	fall time	80 % V_{DDD} to 20 % V_{DDD}	[2]	-	-	4	ns
Data and control input signals on TS ports with respect to P1_CLK, P2_CLK, P3_CLK, P4_CLK, P5_CLK and P6_CLK							
$t_{su(D)}$	data input set-up time			3	-	-	ns
$t_{h(D)}$	data input hold time			0	-	-	ns

[1] The levels must be measured with load circuits; 1.2 kΩ at 3 V (TTL load); C_L = 50 pF.

[2] $V_{DDD} = V_{DDDE1(3V3)}$ or $V_{DDDE2(3V3)}$ or $V_{DDDE3(3V3)}$.

[3] $V_{CC(I2C-bus)}$ is the extended pull-up voltage of the I^2C-bus (3.3 V or 5 V bus).

[4] This reduces the mother board reference clock amplitude.

[5] The SAA7160 can handle a crossover voltage of pins PCI_REFCLKP and PCI_REFCLKN in the same range.

10. Application information

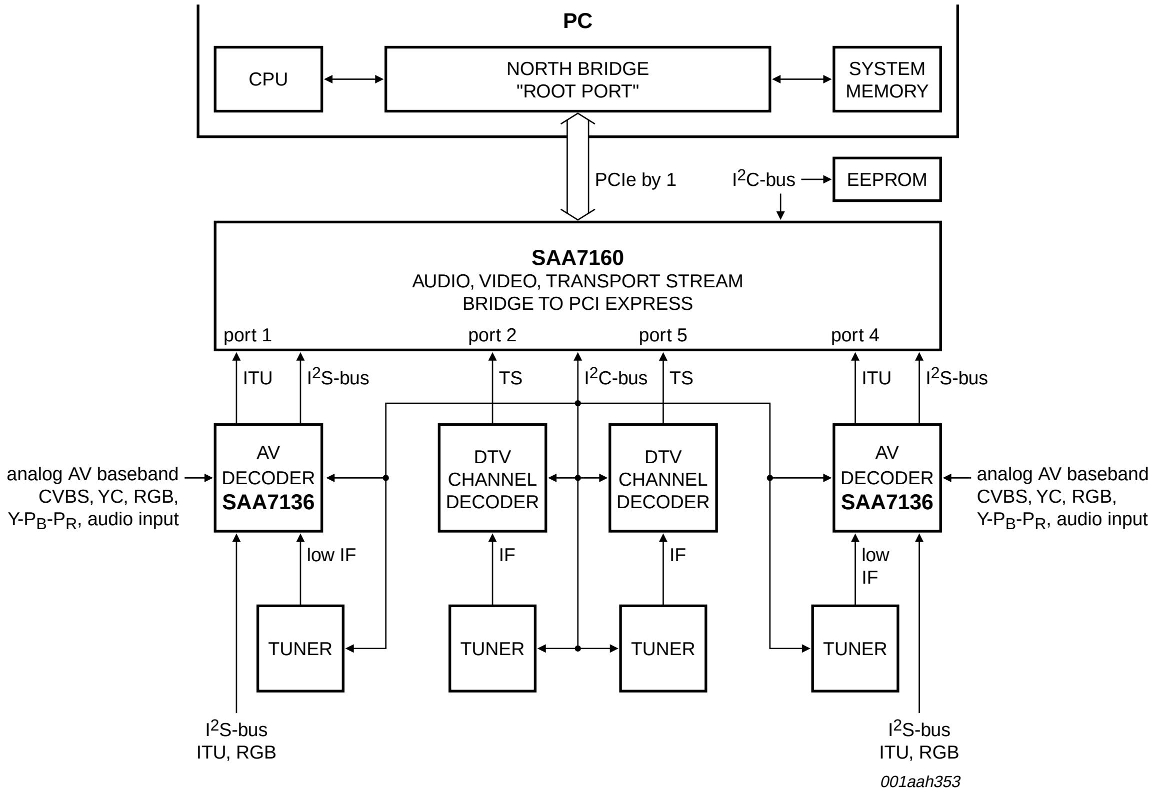


Fig 12. Application example for SAA7160

11. Test information

11.1 Boundary scan test

The SAA7160E and the SAA7160ET have built-in logic and 5 dedicated pins to support boundary scan testing, which allows board testing without special hardware (nails). The SAA7160E and the SAA7160ET follow the *“IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture”* set by the Joint Test Action Group (JTAG) chaired by NXP.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRSTN), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 11. Details about the JTAG BST-TEST can be found in the specification “*IEEE Std. 1149.1*”. Two files containing the detailed Boundary Scan Description Language (BSDL) of the SAA7160E and the SAA7160ET are available on request.

Table 11. BST instructions supported by the SAA7160E and the SAA7160ET

Instruction	Description
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

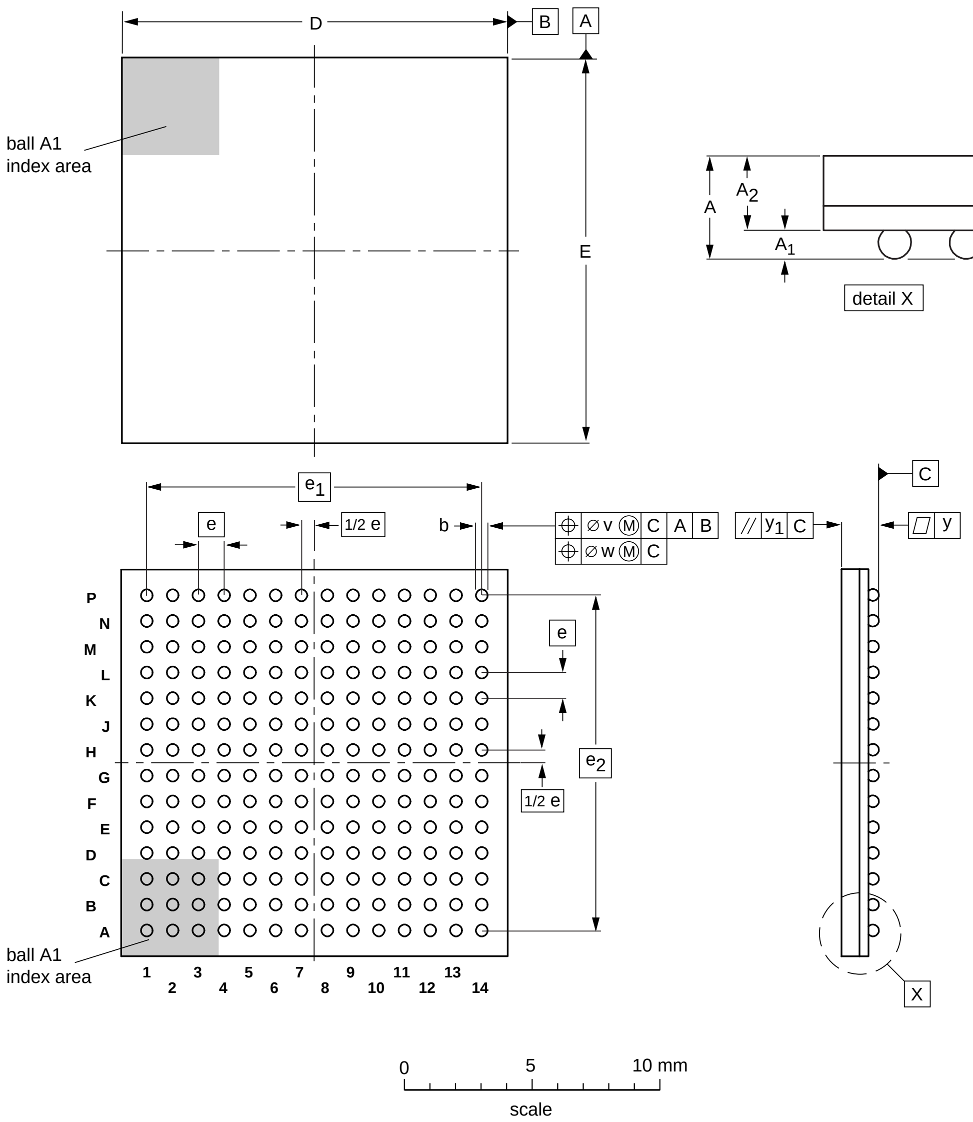
11.1.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRSTN pin LOW.

12. Package outline

LBGA196: plastic low profile ball grid array package; 196 balls; body 15 x 15 x 1 mm **SOT879-1**



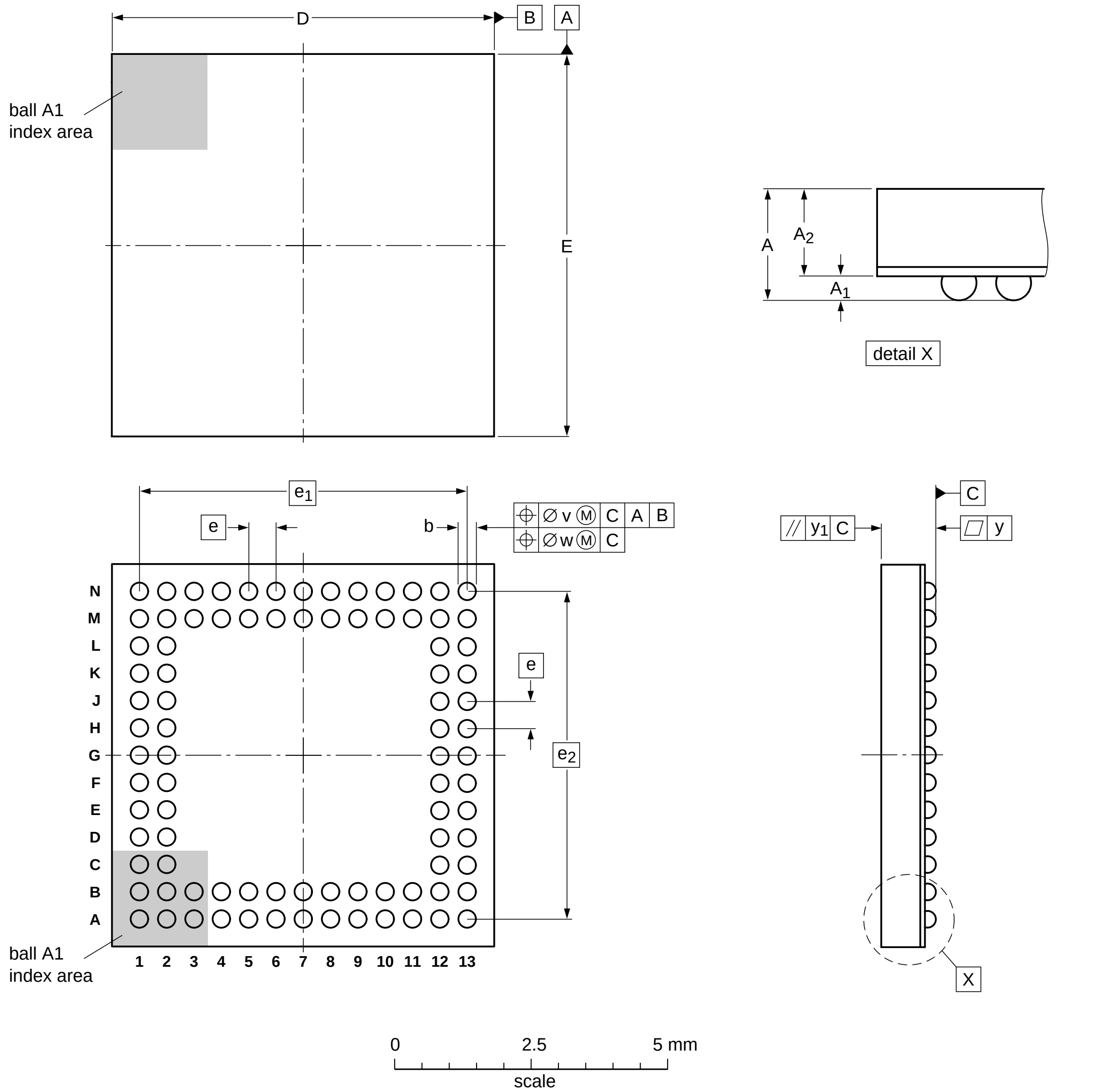
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.55	0.45 0.35	1.1 0.9	0.55 0.45	15.2 14.8	15.2 14.8	1	13	13	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT879-1	- - -	MO-192	- - -			~~05-03-08~~ 05-04-19

Fig 13. Package outline SOT879-1 (LBGA196)

TFBGA88: plastic thin fine-pitch ball grid array package; 88 balls; body 7 x 7 x 0.8 mm **SOT951-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.1	0.25 0.15	0.85 0.75	0.35 0.25	7.1 6.9	7.1 6.9	0.5	6	6	0.15	0.05	0.08	0.1

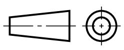
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT951-1	- - -	MO-195	- - -			~~06-05-26~~ 06-08-25

Fig 14. Package outline SOT951-1 (TFBGA88)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 15) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020C)

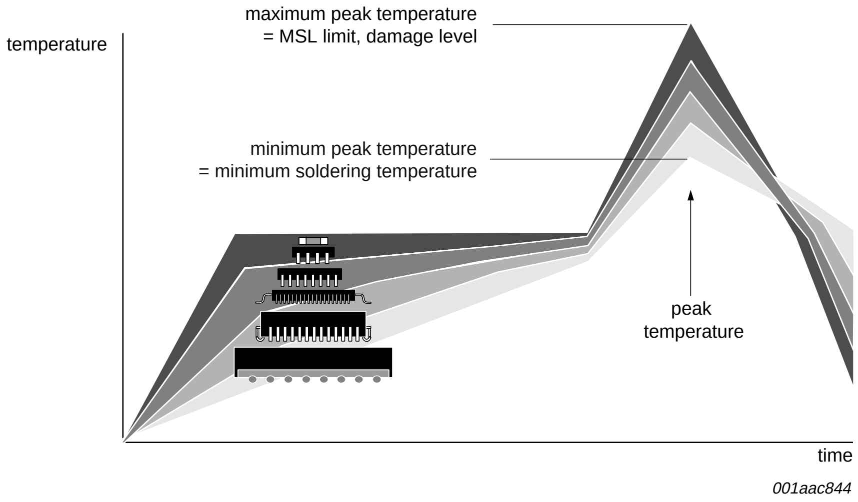
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 15.



MSL: Moisture Sensitivity Level

Fig 15. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 14. Abbreviations

Acronym	Description
AI	Analog Input
AV	Audio Video
BAR	Base Address Register
BSDL	Boundary Scan Description Language
BST	Boundary Scan Test
CGU	Clock Generation Unit
CPU	Central Processing Unit
DCSN	Device Control Status Network
DMA	Direct Memory Access
DTL	Device Transaction Level protocol
DTV	Digital TV
DVI	Digital Video Input
EEPROM	Electrically Erasable Programmable Read-Only Memory
FGPI	Fast General Purpose Input
FIFO	First In First Out
GPIO	General Purpose Input/Output
GREG	Global REGister
HD	High Definition
HDTV	High Definition TV

Table 14. Abbreviations *…continued*

Acronym	Description
ID	IDentification
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
JTAG	Joint Test Action Group
LSB	Least Significant Bit
MME	Multiple Message Enable
MMSD	Memory-Mapped Streaming Data
MMU	Memory Management Unit
MSB	Most Significant Bit
MSI	Message Signal Interrupt
PC	Personal Computer
PCB	Printed-Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PHI	Parallel Host port Interface
PHY	PHYsical interface
PLL	Phase-Locked Loop
PS	Program Stream
PTA	Page Table Address
PTE	Page Table Entry
PVT	Process Voltage Temperature
SD	Standard Definition
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STV	Standard TV
SW	SoftWare
TC	Traffic Class
TS	Transport Stream
TTL	Transistor-Transistor-Logic
VC	Virtual Channel
VI	Video Input
VIP	Video Input Port

15. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SAA7160_1	20080225	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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