



# TDA9981A

HDMI transmitter up to 150 MHz pixel rate with  $3 \times 8$ -bit video inputs and  $4 \times I^2S$ -bus with S/PDIF

Rev. 01 — 19 May 2008

Product data sheet

## HDMI

### 1. General description

The TDA9981A is an HDMI transmitter (which also supports DVI) that enables a  $3 \times 8$ -bit RGB or  $Y C_B C_R$  video stream (with a pixel rate up to 150 MHz for the TDA9981AHL/15 version), up to 4  $I^2S$ -bus audio streams (with an audio sampling rate up to 192 kHz) and the additional information required by all the HDMI 1.2a standards.

In order to be compatible with most applications, the TDA9981A integrates a full programmable input formatter and color space conversion block. The video input formats accepted are  $Y C_B C_R$  4 : 4 : 4 (up to  $3 \times 8$ -bit),  $Y C_B C_R$  4 : 2 : 2 semi-planar (up to  $2 \times 12$ -bit),  $Y C_B C_R$  4 : 2 : 2 compliant with ITU656 and ITU656-like (up to  $1 \times 12$ -bit).

For ITU656-like formats, double edges are supported so that data can be sampled on rising and falling edges.

The TDA9981A also includes a HDCP 1.1-compliant cipher block. The HDCP key set is stored internally in a One Time Programmable (OTP) non-volatile memory for maximum security.

The device can be controlled via an  $I^2C$ -bus interface.

### 2. Features

- $3 \times 8$ -bit video data input bus, CMOS and LV-TTL compatible
- Horizontal synchronization, vertical synchronization and Data Enable (DE) inputs or VREF, HREF and FREF could be used for input data synchronization
- Pixel rate clock input can be made active on one or both edges (selectable by  $I^2C$ -bus)
- The TDA9981A has 4  $I^2S$ -bus audio input channels and 1 S/PDIF channel; audio sampling rate up to 192 kHz
- 250 MHz to 1.50 GHz HDMI transmitter operation
- Programmable input formatter and upsampler/interpolator allows input of any of the 4 : 4 : 4, 4 : 2 : 2 semi-planar, 4 : 2 : 2 ITU656 and ITU656-like formats
- Programmable color space converter:
  - ◆ RGB to  $Y C_B C_R$
  - ◆  $Y C_B C_R$  to RGB
- Deals with multiple levels of HDCP receivers and repeaters
- Internal SHA-1 calculation
- Controllable via  $I^2C$ -bus
- Low power dissipation

- 1.8 V and 3.3 V power supplies
- Power-down mode
- Hard reset

### 3. Applications

- DVD players and recorders
- Set-Top Box (STB)
- AV receivers and amplifiers (repeater)
- Camcorders
- Digital still cameras
- Media players
- PVRs
- Media centers PCs, graphics add-in boards, notebook PCs
- Switches

### 4. Quick reference data

**Table 1. Quick reference data**

$V_{DDA(FRO\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDA(PLL\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDH(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  
 $V_{DDD(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDC(1V8)} = 1.65\text{ V to }1.95\text{ V}$ ;  $V_{PP} = 0\text{ V}$ ;  $T_{amb} = 0\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ .  
 Typical values are measured at  $V_{DDA(FRO\_3V3)} = V_{DDA(PLL\_3V3)} = V_{DDH(3V3)} = V_{DDD(3V3)} = 3.3\text{ V}$ ;  
 $V_{DDC(1V8)} = 1.8\text{ V}$ ;  $V_{PP} = 0\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TDA9981AHL/8 and TDA9981AHL/15</b>						
$V_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply voltage		3.0	3.3	3.6	V
$V_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply voltage		3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.65	1.8	1.95	V
$T_{amb}$	ambient temperature		0	-	85	$^{\circ}\text{C}$
<b>TDA9981AHL/8; up to 81 MHz</b>						
$f_{clk(max)}$	maximum clock frequency	[1]	81	-	-	MHz
$P_{cons}$	power consumption	[1]	-	235	288	mW
$P_{tot}$	total power dissipation	[1]	-	369	438	mW
$P_{pd}$	power dissipation in Power-down mode		-	14	19	mW

**Table 1. Quick reference data ...continued**

$V_{DDA(FRO\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDA(PLL\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDH(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  
 $V_{DDD(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDC(1V8)} = 1.65\text{ V to }1.95\text{ V}$ ;  $V_{PP} = 0\text{ V}$ ;  $T_{amb} = 0\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ .  
*Typical values are measured at  $V_{DDA(FRO\_3V3)} = V_{DDA(PLL\_3V3)} = V_{DDH(3V3)} = V_{DDD(3V3)} = 3.3\text{ V}$ ;  
 $V_{DDC(1V8)} = 1.8\text{ V}$ ;  $V_{PP} = 0\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TDA9981AHL/15; up to 150 MHz</b>						
$f_{clk(max)}$	maximum clock frequency		[2] 150	-	-	MHz
$P_{cons}$	power consumption		[2] -	381.5	468	mW
$P_{tot}$	total power dissipation		[2] -	515.5	618	mW
$P_{pd}$	power dissipation in Power-down mode		-	14	19	mW

[1] Worst case: video input format: 720p at 60 Hz (RGB 4 : 4 : 4 embedded sync), video output format: 720p at 60 Hz (YCbCr 4 : 4 : 4).

[2] Video input format: 1080p (RGB 4 : 4 : 4 embedded sync, rising edge), video output format: 1080p (RGB 4 : 4 : 4).

## 5. Ordering information

**Table 2. Ordering information**

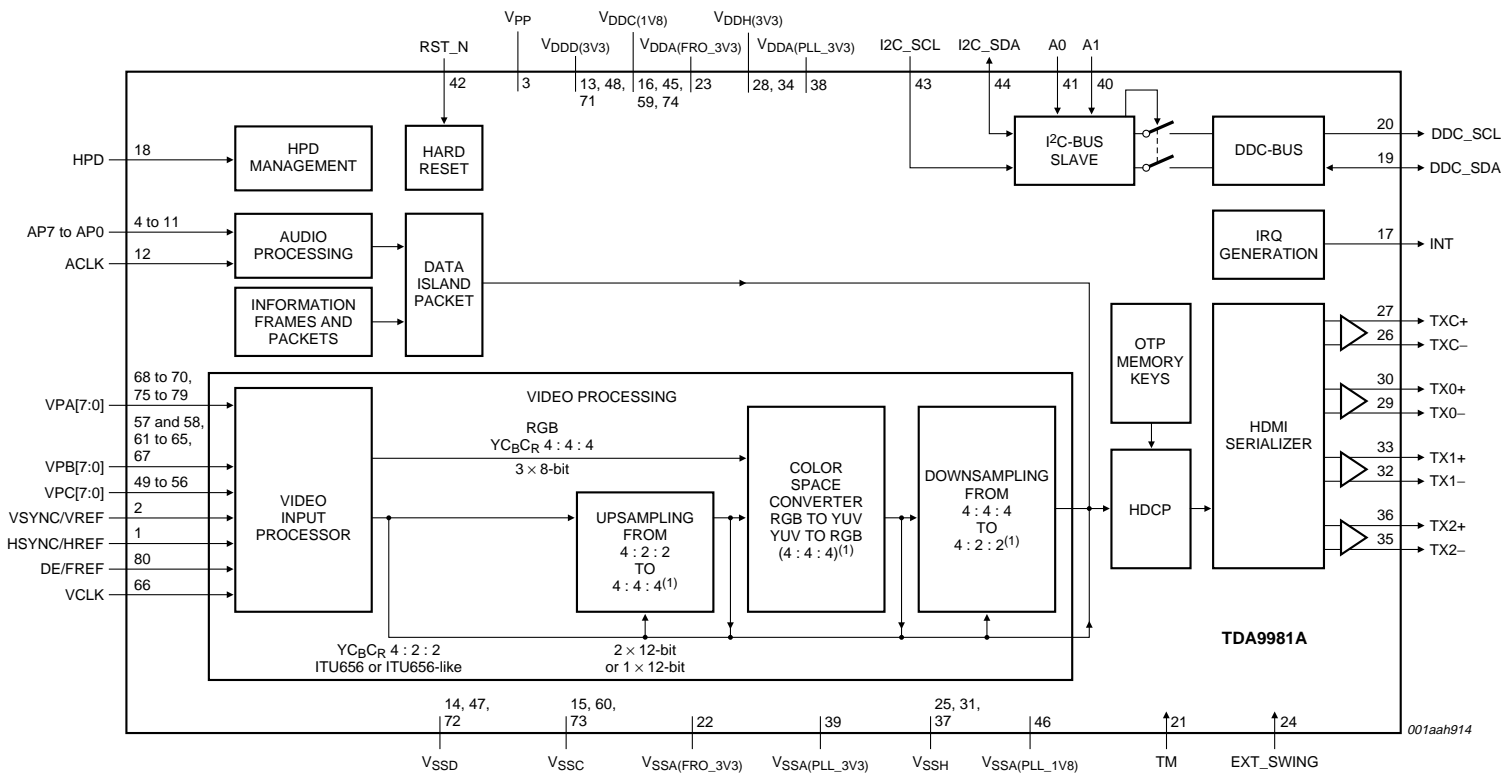
Type number	Package		
	Name	Description	Version
TDA9981AHL	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

### 5.1 Ordering options

**Table 3. Survey of type numbers**

Extended type number	Sampling frequency (Msample/s)	Application
TDA9981AHL/8/C1xx	81	customer specific version
TDA9981AHL/15/C1xx	150	customer specific version

## 6. Block diagram



(1) Block can be bypassed.

Fig 1. Block diagram

## 7. Pinning information

### 7.1 Pinning

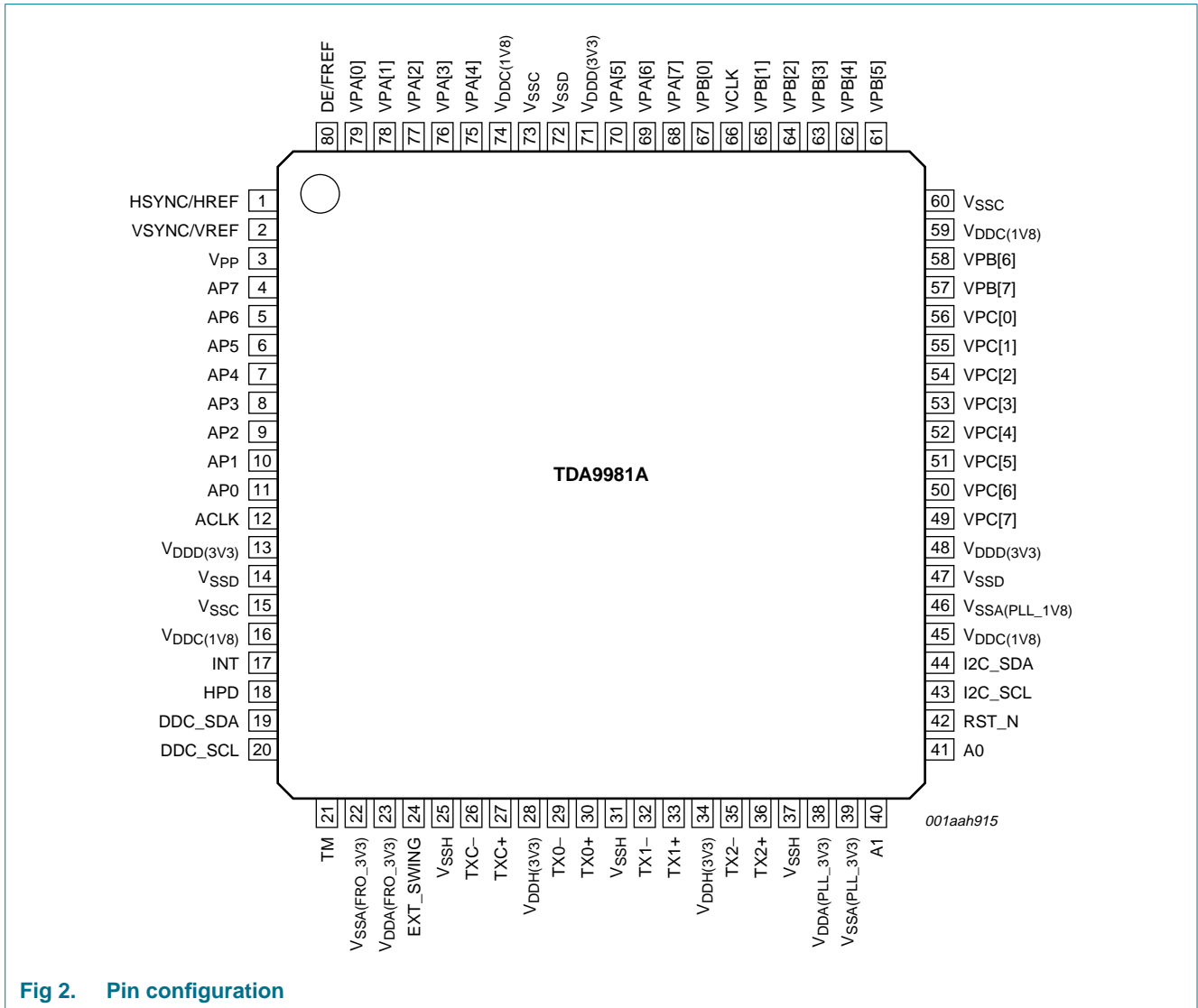


Fig 2. Pin configuration

### 7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type <sup>[1]</sup>	Description
HSYNC/HREF	1	I	horizontal synchronization or reference input
VSYNC/VREF	2	I	vertical synchronization or reference input
V <sub>PP</sub>	3	P	programming voltage for OTP memory (must be connected to the ground of the digital core in normal operation)
AP7	4	I	audio port 7 input; auxiliary (AUX)
AP6	5	I	audio port 6 input; S/PDIF stream
AP5	6	I	audio port 5 input; optional master clock MCLK for S/PDIF

Table 4. Pin description ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
AP4	7	I	audio port 4 input; I <sup>2</sup> S-bus port 3
AP3	8	I	audio port 3 input; I <sup>2</sup> S-bus port 2
AP2	9	I	audio port 2 input; I <sup>2</sup> S-bus port 1
AP1	10	I	audio port 1 input; I <sup>2</sup> S-bus port 0
AP0	11	I	audio port 0 input; word select WS for I <sup>2</sup> S-bus
ACLK	12	I	audio clock input; clock SCK for I <sup>2</sup> S-bus
V <sub>DD(3V3)</sub>	13	P	supply voltage for input ports (3.3 V)
V <sub>SSD</sub>	14	G	ground for input ports
V <sub>SSC</sub>	15	G	ground for digital core
V <sub>DDC(1V8)</sub>	16	P	supply voltage for digital core (1.8 V)
INT	17	O	interrupt output (open drain); warns the external microprocessor that a special event has occurred; must be connected to a pull-up resistor; 5 V tolerant
HPD	18	I	hot plug detect input; 5 V tolerant
DDC_SDA	19	I/O	DDC-bus data input/output (open drain); must be connected to a pull-up resistor; 5 V tolerant
DDC_SCL	20	O	DDC-bus clock output (open drain); must be connected to a pull-up resistor; 5 V tolerant
TM	21	I	internal test mode input (must be connected to the ground of the digital core in normal operation)
V <sub>SSA(FRO_3V3)</sub>	22	G	analog ground for free running oscillator
V <sub>D(FA(FRO_3V3)</sub>	23	P	analog supply voltage for free running oscillator (3.3 V)
EXT_SWING	24	I	external swing adjust input; a fixed resistor must be connected between this pin and pin V <sub>DDH(3V3)</sub> to set the HDMI output swing (see <a href="#">Section 8.15.1</a> )
V <sub>SSH</sub>	25	G	ground for HDMI transmitter
TXC-	26	O	negative clock channel for HDMI output
TXC+	27	O	positive clock channel for HDMI output
V <sub>DDH(3V3)</sub>	28	P	supply voltage for HDMI transmitter (3.3 V)
TX0-	29	O	negative data channel 0 for HDMI output
TX0+	30	O	positive data channel 0 for HDMI output
V <sub>SSH</sub>	31	G	ground for HDMI transmitter
TX1-	32	O	negative data channel 1 for HDMI output
TX1+	33	O	positive data channel 1 for HDMI output
V <sub>DDH(3V3)</sub>	34	P	supply voltage for HDMI transmitter (3.3 V)
TX2-	35	O	negative data channel 2 for HDMI output
TX2+	36	O	positive data channel 2 for HDMI output
V <sub>SSH</sub>	37	G	ground for HDMI transmitter
V <sub>D(PL(PLL_3V3)</sub>	38	P	analog supply voltage for PLL (3.3 V)
V <sub>SSA(PLL_3V3)</sub>	39	G	analog ground reference for PLL
A1	40	I	I <sup>2</sup> C-bus slave address input 1; bit 1
A0	41	I	I <sup>2</sup> C-bus slave address input 0; bit 0
RST_N	42	I	hard reset input; active LOW

Table 4. Pin description ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
I2C_SCL	43	I	I <sup>2</sup> C-bus clock input of device (open drain); must be connected to a pull-up resistor; 5 V tolerant
I2C_SDA	44	I/O	I <sup>2</sup> C-bus data input/output of device (open drain); must be connected to a pull-up resistor; 5 V tolerant
V <sub>DDC(1V8)</sub>	45	P	supply voltage for digital core (1.8 V)
V <sub>SSA(PLL_1V8)</sub>	46	G	analog ground reference for PLL
V <sub>SSD</sub>	47	G	ground for input ports
V <sub>DDD(3V3)</sub>	48	P	supply voltage for input ports (3.3 V)
VPC[7]	49	I	video port C input bit 7
VPC[6]	50	I	video port C input bit 6
VPC[5]	51	I	video port C input bit 5
VPC[4]	52	I	video port C input bit 4
VPC[3]	53	I	video port C input bit 3
VPC[2]	54	I	video port C input bit 2
VPC[1]	55	I	video port C input bit 1
VPC[0]	56	I	video port C input bit 0
VPB[7]	57	I	video port B input bit 7
VPB[6]	58	I	video port B input bit 6
V <sub>DDC(1V8)</sub>	59	P	supply voltage for digital core (1.8 V)
V <sub>SSC</sub>	60	G	ground for digital core
VPB[5]	61	I	video port B input bit 5
VPB[4]	62	I	video port B input bit 4
VPB[3]	63	I	video port B input bit 3
VPB[2]	64	I	video port B input bit 2
VPB[1]	65	I	video port B input bit 1
VCLK	66	I	video pixel clock input
VPB[0]	67	I	video port B input bit 0
VPA[7]	68	I	video port A input bit 7
VPA[6]	69	I	video port A input bit 6
VPA[5]	70	I	video port A input bit 5
V <sub>DDD(3V3)</sub>	71	P	supply voltage for input ports (3.3 V)
V <sub>SSD</sub>	72	G	ground for input ports
V <sub>SSC</sub>	73	G	ground for digital core
V <sub>DDC(1V8)</sub>	74	P	supply voltage for digital core (1.8 V)
VPA[4]	75	I	video port A input bit 4
VPA[3]	76	I	video port A input bit 3
VPA[2]	77	I	video port A input bit 2
VPA[1]	78	I	video port A input bit 1
VPA[0]	79	I	video port A input bit 0
DE/FREF	80	I	video data enable input or field reference input

[1] P = power supply; G = ground; I = input; O = output.

## 8. Functional description

The TDA9981A is designed to convert digital data (video and audio) into an HDMI or a DVI stream. This HDMI stream can handle RGB, YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4 and YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2. The TDA9981A can accept at its inputs any of the following video modes:

- RGB
- YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4
- YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar
- YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656 and ITU656-like

It can also handle audio. The TDA9981A can accept at its inputs any of the following audio buses:

- I<sup>2</sup>S-bus (4 lines): up to 8 audio channels
- S/PDIF (1 channel): L-PCM (IEC 60958) or compressed audio (IEC 61937)

### 8.1 System clock

The clock management is based on a set of two PLLs that generate the different clocks required inside the chip:

- PLL double edge can generate a clock at twice the VCLK input frequency to capture the data at the video input formatter.
- PLL serializer is a system clock generator, which enables the stream produced by the encoder to be transmitted on the HDMI data channel at ten times the sampling rate or more; see [Section 8.15.2](#).

### 8.2 Video input processor

The TDA9981A has three video input ports VPA[7:0], VPB[7:0] and VPC[7:0]. The TDA9981A can reallocate and swap each of the 3 input channel ports by inverting the bus and swapping each port.

The TDA9981A can be set to latch data at either the rising or falling edge or both.

The video input formats accept (see [Table 5](#)):

- RGB
- YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4 (up to 3 × 8-bit)
- YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar (up to 2 × 12-bit)
- YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 compliant with ITU656 and ITU656-like (up to 1 × 12-bit)



Table 5. Inputs of video input formatter

Color space	Format	Channels	Sync	Rising edge	Falling edge	Double edge <sup>[1]</sup>	Transmission input format	Max. pixel clock on pin VCLK (MHz)	Max. input format	Reference	
RGB	4 : 4 : 4	3 × 8-bit	external	X				150		<a href="#">Table 6</a>	
			external			X		150			
			embedded	X				150			
			embedded			X		150			
YCbCr	4 : 4 : 4	3 × 8-bit	external	X				150		<a href="#">Table 7</a>	
			external			X		150			
			embedded	X				150			
			embedded			X		150			
YCbCr	4 : 2 : 2	up to 1 × 12-bit ITU656-like	external	X			ITU656-like	54.054	480p/576p	<a href="#">Table 8</a>	
			external			X		ITU656-like	54.054		480p/576p
			external				X	ITU656-like	27.027		480p/576p
			embedded	X				ITU656-like	54.054		480p/576p
			embedded			X		ITU656-like	54.054		480p/576p
			embedded				X	ITU656-like	27.027		480p/576p
		up to 2 × 12-bit semi-planar	external	X					148.5	1080p	<a href="#">Table 12</a>
			external				X		148.5	1080p	
			embedded	X				SMPTE293M	148.5	1080p	
			embedded				X	SMPTE293M	148.5	1080p	

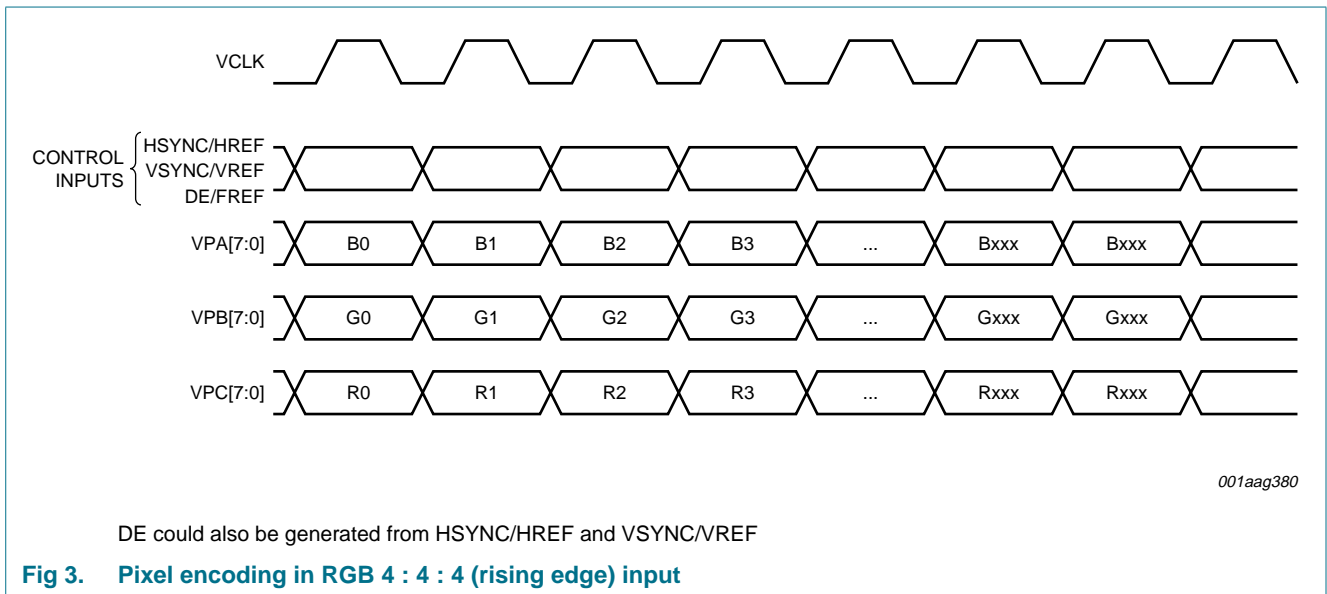
[1] Double edge means both rising and falling edges.

**Table 6. RGB 4 : 4 : 4 mappings**

RGB 4 : 4 : 4 (3 × 8-bit) external synchronization single edge.

Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 45h; VIP\_CNTRL\_2 = 01h.

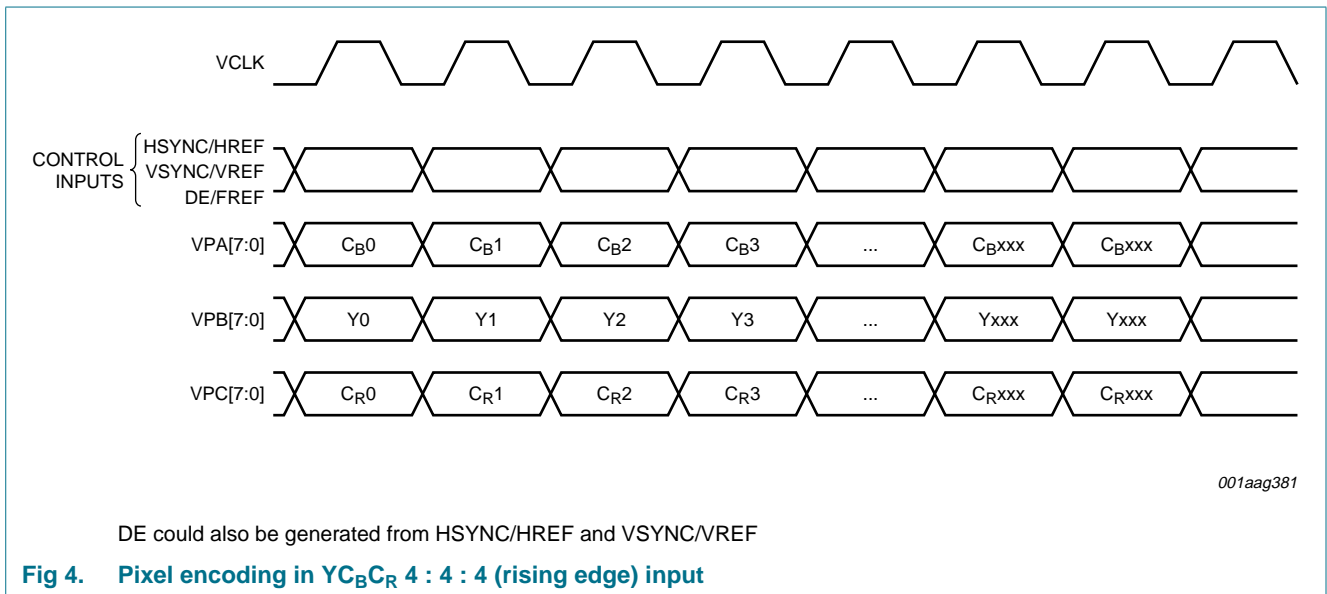
Video port A		Video port B		Video port C		Control	
Pin	RGB 4 : 4 : 4	Pin	RGB 4 : 4 : 4	Pin	RGB 4 : 4 : 4	Pin	RGB 4 : 4 : 4
VPA[0]	B[0]	VPB[0]	G[0]	VPC[0]	R[0]	HSYNC/HREF	used
VPA[1]	B[1]	VPB[1]	G[1]	VPC[1]	R[1]	VSYNC/VREF	used
VPA[2]	B[2]	VPB[2]	G[2]	VPC[2]	R[2]	DE/FREF	used
VPA[3]	B[3]	VPB[3]	G[3]	VPC[3]	R[3]		
VPA[4]	B[4]	VPB[4]	G[4]	VPC[4]	R[4]		
VPA[5]	B[5]	VPB[5]	G[5]	VPC[5]	R[5]		
VPA[6]	B[6]	VPB[6]	G[6]	VPC[6]	R[6]		
VPA[7]	B[7]	VPB[7]	G[7]	VPC[7]	R[7]		



**Table 7. YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4 mappings**

YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4 (3 × 8-bit) external synchronization single edge.  
 Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 45h; VIP\_CNTRL\_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 4 : 4	Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 4 : 4	Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 4 : 4	Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 4 : 4
VPA[0]	C <sub>B</sub> [0]	VPB[0]	Y[0]	VPC[0]	C <sub>R</sub> [0]	HSYNC/HREF	used
VPA[1]	C <sub>B</sub> [1]	VPB[1]	Y[1]	VPC[1]	C <sub>R</sub> [1]	VSYNC/VREF	used
VPA[2]	C <sub>B</sub> [2]	VPB[2]	Y[2]	VPC[2]	C <sub>R</sub> [2]	DE/FREF	used
VPA[3]	C <sub>B</sub> [3]	VPB[3]	Y[3]	VPC[3]	C <sub>R</sub> [3]		
VPA[4]	C <sub>B</sub> [4]	VPB[4]	Y[4]	VPC[4]	C <sub>R</sub> [4]		
VPA[5]	C <sub>B</sub> [5]	VPB[5]	Y[5]	VPC[5]	C <sub>R</sub> [5]		
VPA[6]	C <sub>B</sub> [6]	VPB[6]	Y[6]	VPC[6]	C <sub>R</sub> [6]		
VPA[7]	C <sub>B</sub> [7]	VPB[7]	Y[7]	VPC[7]	C <sub>R</sub> [7]		

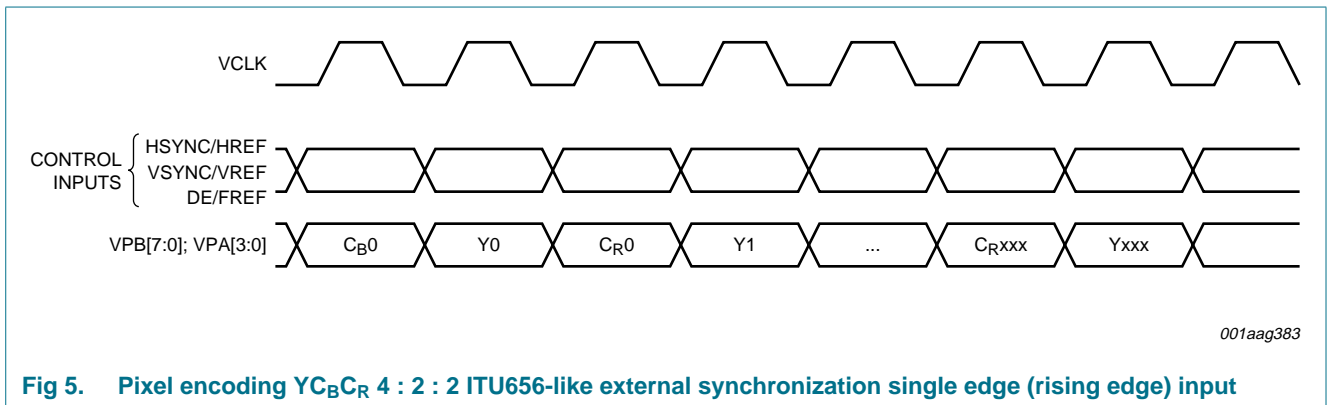


**Fig 4. Pixel encoding in YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4 (rising edge) input**

**Table 8. YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like external synchronization single edge mappings**

YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like external synchronization single edge.  
 Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 00h.

Video port A					Video port B					Control	
Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2
VPA[0]	C <sub>B</sub> [0]	Y <sub>0</sub> [0]	C <sub>R</sub> [0]	Y <sub>1</sub> [0]	VPB[0]	C <sub>B</sub> [4]	Y <sub>0</sub> [4]	C <sub>R</sub> [4]	Y <sub>1</sub> [4]	HSYNC/HREF	used
VPA[1]	C <sub>B</sub> [1]	Y <sub>0</sub> [1]	C <sub>R</sub> [1]	Y <sub>1</sub> [1]	VPB[1]	C <sub>B</sub> [5]	Y <sub>0</sub> [5]	C <sub>R</sub> [5]	Y <sub>1</sub> [5]	VSYNC/VREF	used
VPA[2]	C <sub>B</sub> [2]	Y <sub>0</sub> [2]	C <sub>R</sub> [2]	Y <sub>1</sub> [2]	VPB[2]	C <sub>B</sub> [6]	Y <sub>0</sub> [6]	C <sub>R</sub> [6]	Y <sub>1</sub> [6]	DE/FREF	used
VPA[3]	C <sub>B</sub> [3]	Y <sub>0</sub> [3]	C <sub>R</sub> [3]	Y <sub>1</sub> [3]	VPB[3]	C <sub>B</sub> [7]	Y <sub>0</sub> [7]	C <sub>R</sub> [7]	Y <sub>1</sub> [7]		
VPA[4]	-	-	-	-	VPB[4]	C <sub>B</sub> [8]	Y <sub>0</sub> [8]	C <sub>R</sub> [8]	Y <sub>1</sub> [8]		
VPA[5]	-	-	-	-	VPB[5]	C <sub>B</sub> [9]	Y <sub>0</sub> [9]	C <sub>R</sub> [9]	Y <sub>1</sub> [9]		
VPA[6]	-	-	-	-	VPB[6]	C <sub>B</sub> [10]	Y <sub>0</sub> [10]	C <sub>R</sub> [10]	Y <sub>1</sub> [10]		
VPA[7]	-	-	-	-	VPB[7]	C <sub>B</sub> [11]	Y <sub>0</sub> [11]	C <sub>R</sub> [11]	Y <sub>1</sub> [11]		

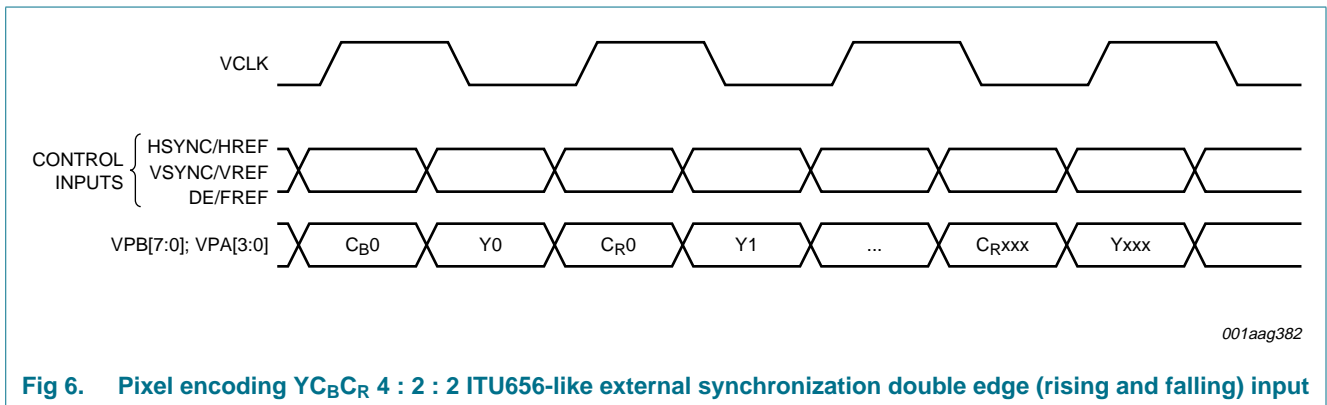


**Table 9. YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like external synchronization double edge mappings**

YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like external synchronization double edge.

Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 00h.

Video port A					Video port B					Control	
Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2
VPA[0]	C <sub>B</sub> [0]	Y <sub>0</sub> [0]	C <sub>R</sub> [0]	Y <sub>1</sub> [0]	VPB[0]	C <sub>B</sub> [4]	Y <sub>0</sub> [4]	C <sub>R</sub> [4]	Y <sub>1</sub> [4]	HSYNC/HREF	used
VPA[1]	C <sub>B</sub> [1]	Y <sub>0</sub> [1]	C <sub>R</sub> [1]	Y <sub>1</sub> [1]	VPB[1]	C <sub>B</sub> [5]	Y <sub>0</sub> [5]	C <sub>R</sub> [5]	Y <sub>1</sub> [5]	VSYNC/VREF	used
VPA[2]	C <sub>B</sub> [2]	Y <sub>0</sub> [2]	C <sub>R</sub> [2]	Y <sub>1</sub> [2]	VPB[2]	C <sub>B</sub> [6]	Y <sub>0</sub> [6]	C <sub>R</sub> [6]	Y <sub>1</sub> [6]	DE/FREF	used
VPA[3]	C <sub>B</sub> [3]	Y <sub>0</sub> [3]	C <sub>R</sub> [3]	Y <sub>1</sub> [3]	VPB[3]	C <sub>B</sub> [7]	Y <sub>0</sub> [7]	C <sub>R</sub> [7]	Y <sub>1</sub> [7]		
VPA[4]	-	-	-	-	VPB[4]	C <sub>B</sub> [8]	Y <sub>0</sub> [8]	C <sub>R</sub> [8]	Y <sub>1</sub> [8]		
VPA[5]	-	-	-	-	VPB[5]	C <sub>B</sub> [9]	Y <sub>0</sub> [9]	C <sub>R</sub> [9]	Y <sub>1</sub> [9]		
VPA[6]	-	-	-	-	VPB[6]	C <sub>B</sub> [10]	Y <sub>0</sub> [10]	C <sub>R</sub> [10]	Y <sub>1</sub> [10]		
VPA[7]	-	-	-	-	VPB[7]	C <sub>B</sub> [11]	Y <sub>0</sub> [11]	C <sub>R</sub> [11]	Y <sub>1</sub> [11]		



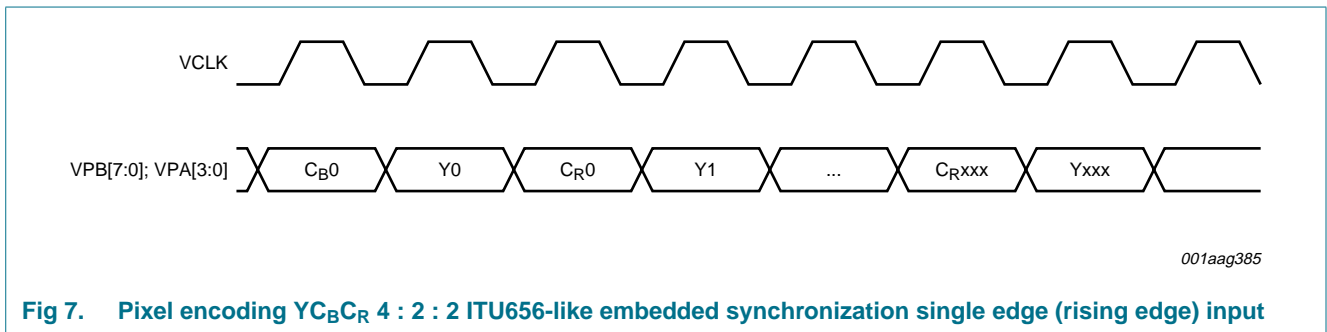
**Fig 6. Pixel encoding YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like external synchronization double edge (rising and falling) input**

**Table 10. YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like embedded synchronization single edge mappings**

YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like embedded synchronization single edge.

Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 00h.

Video port A					Video port B					Control	
Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2
VPA[0]	C <sub>B</sub> [0]	Y <sub>0</sub> [0]	C <sub>R</sub> [0]	Y <sub>1</sub> [0]	VPB[0]	C <sub>B</sub> [4]	Y <sub>0</sub> [4]	C <sub>R</sub> [4]	Y <sub>1</sub> [4]	HSYNC/HREF	not used
VPA[1]	C <sub>B</sub> [1]	Y <sub>0</sub> [1]	C <sub>R</sub> [1]	Y <sub>1</sub> [1]	VPB[1]	C <sub>B</sub> [5]	Y <sub>0</sub> [5]	C <sub>R</sub> [5]	Y <sub>1</sub> [5]	VSYNC/VREF	not used
VPA[2]	C <sub>B</sub> [2]	Y <sub>0</sub> [2]	C <sub>R</sub> [2]	Y <sub>1</sub> [2]	VPB[2]	C <sub>B</sub> [6]	Y <sub>0</sub> [6]	C <sub>R</sub> [6]	Y <sub>1</sub> [6]	DE/FREF	not used
VPA[3]	C <sub>B</sub> [3]	Y <sub>0</sub> [3]	C <sub>R</sub> [3]	Y <sub>1</sub> [3]	VPB[3]	C <sub>B</sub> [7]	Y <sub>0</sub> [7]	C <sub>R</sub> [7]	Y <sub>1</sub> [7]		
VPA[4]	-	-	-	-	VPB[4]	C <sub>B</sub> [8]	Y <sub>0</sub> [8]	C <sub>R</sub> [8]	Y <sub>1</sub> [8]		
VPA[5]	-	-	-	-	VPB[5]	C <sub>B</sub> [9]	Y <sub>0</sub> [9]	C <sub>R</sub> [9]	Y <sub>1</sub> [9]		
VPA[6]	-	-	-	-	VPB[6]	C <sub>B</sub> [10]	Y <sub>0</sub> [10]	C <sub>R</sub> [10]	Y <sub>1</sub> [10]		
VPA[7]	-	-	-	-	VPB[7]	C <sub>B</sub> [11]	Y <sub>0</sub> [11]	C <sub>R</sub> [11]	Y <sub>1</sub> [11]		

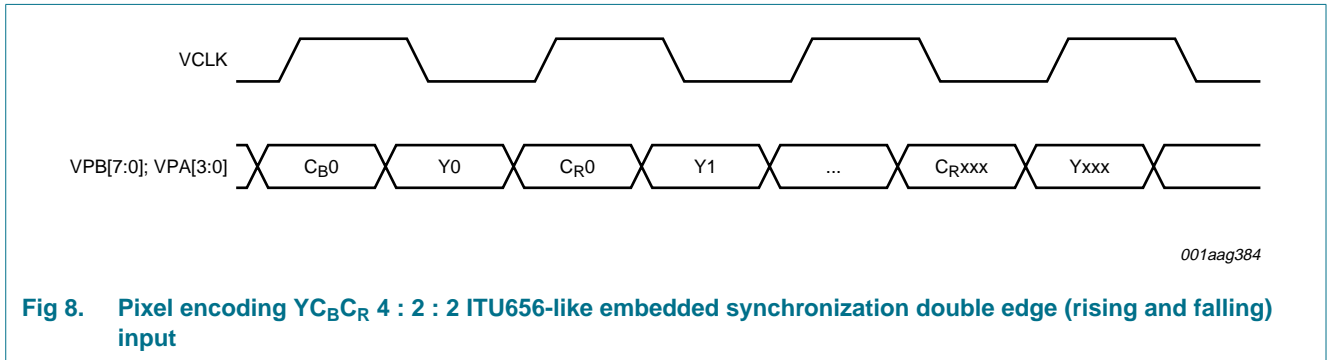


**Table 11. YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like embedded synchronization double edge mappings**

YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like embedded synchronization double edge.

Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 00h.

Video port A					Video port B					Control	
Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 (ITU656-like)				Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2
VPA[0]	C <sub>B</sub> [0]	Y <sub>0</sub> [0]	C <sub>R</sub> [0]	Y <sub>1</sub> [0]	VPB[0]	C <sub>B</sub> [4]	Y <sub>0</sub> [4]	C <sub>R</sub> [4]	Y <sub>1</sub> [4]	HSYNC/HREF	not used
VPA[1]	C <sub>B</sub> [1]	Y <sub>0</sub> [1]	C <sub>R</sub> [1]	Y <sub>1</sub> [1]	VPB[1]	C <sub>B</sub> [5]	Y <sub>0</sub> [5]	C <sub>R</sub> [5]	Y <sub>1</sub> [5]	VSYNC/VREF	not used
VPA[2]	C <sub>B</sub> [2]	Y <sub>0</sub> [2]	C <sub>R</sub> [2]	Y <sub>1</sub> [2]	VPB[2]	C <sub>B</sub> [6]	Y <sub>0</sub> [6]	C <sub>R</sub> [6]	Y <sub>1</sub> [6]	DE/FREF	not used
VPA[3]	C <sub>B</sub> [3]	Y <sub>0</sub> [3]	C <sub>R</sub> [3]	Y <sub>1</sub> [3]	VPB[3]	C <sub>B</sub> [7]	Y <sub>0</sub> [7]	C <sub>R</sub> [7]	Y <sub>1</sub> [7]		
VPA[4]	-	-	-	-	VPB[4]	C <sub>B</sub> [8]	Y <sub>0</sub> [8]	C <sub>R</sub> [8]	Y <sub>1</sub> [8]		
VPA[5]	-	-	-	-	VPB[5]	C <sub>B</sub> [9]	Y <sub>0</sub> [9]	C <sub>R</sub> [9]	Y <sub>1</sub> [9]		
VPA[6]	-	-	-	-	VPB[6]	C <sub>B</sub> [10]	Y <sub>0</sub> [10]	C <sub>R</sub> [10]	Y <sub>1</sub> [10]		
VPA[7]	-	-	-	-	VPB[7]	C <sub>B</sub> [11]	Y <sub>0</sub> [11]	C <sub>R</sub> [11]	Y <sub>1</sub> [11]		



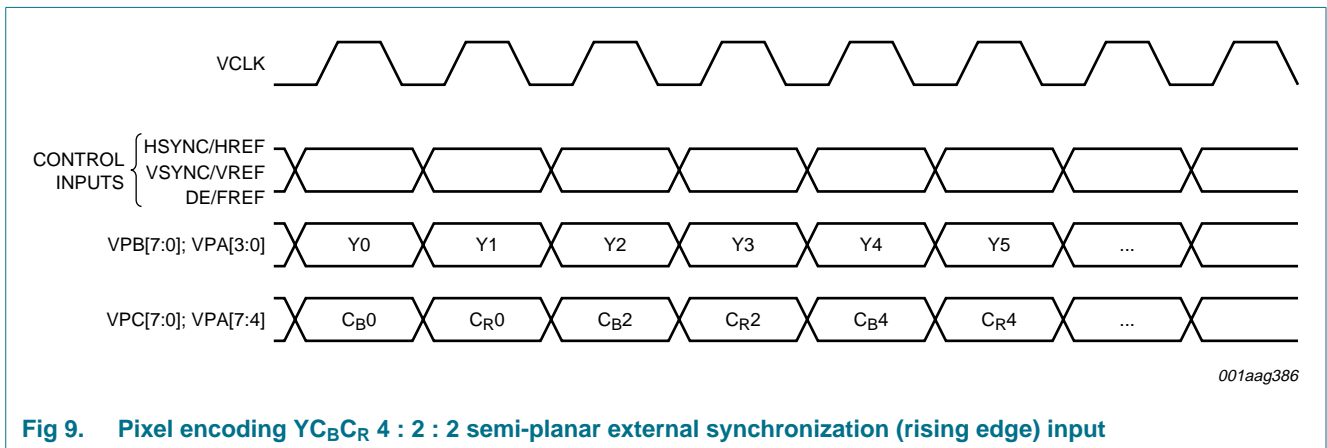
**Fig 8. Pixel encoding YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like embedded synchronization double edge (rising and falling) input**

**Table 12. YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar external synchronization mappings**

YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar external synchronization single edge.

Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 semi-planar		Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 semi-planar		Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 semi-planar		Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2
VPA[0]	Y <sub>0</sub> [0]	Y <sub>1</sub> [0]	VPB[0]	Y <sub>0</sub> [4]	Y <sub>1</sub> [4]	VPC[0]	C <sub>B</sub> [4]	C <sub>R</sub> [4]	HSYNC/HREF	used
VPA[1]	Y <sub>0</sub> [1]	Y <sub>1</sub> [1]	VPB[1]	Y <sub>0</sub> [5]	Y <sub>1</sub> [5]	VPC[1]	C <sub>B</sub> [5]	C <sub>R</sub> [5]	VSYNC/VREF	used
VPA[2]	Y <sub>0</sub> [2]	Y <sub>1</sub> [2]	VPB[2]	Y <sub>0</sub> [6]	Y <sub>1</sub> [6]	VPC[2]	C <sub>B</sub> [6]	C <sub>R</sub> [6]	DE/FREF	used
VPA[3]	Y <sub>0</sub> [3]	Y <sub>1</sub> [3]	VPB[3]	Y <sub>0</sub> [7]	Y <sub>1</sub> [7]	VPC[3]	C <sub>B</sub> [7]	C <sub>R</sub> [7]		
VPA[4]	C <sub>B</sub> [0]	C <sub>R</sub> [0]	VPB[4]	Y <sub>0</sub> [8]	Y <sub>1</sub> [8]	VPC[4]	C <sub>B</sub> [8]	C <sub>R</sub> [8]		
VPA[5]	C <sub>B</sub> [1]	C <sub>R</sub> [1]	VPB[5]	Y <sub>0</sub> [9]	Y <sub>1</sub> [9]	VPC[5]	C <sub>B</sub> [9]	C <sub>R</sub> [9]		
VPA[6]	C <sub>B</sub> [2]	C <sub>R</sub> [2]	VPB[6]	Y <sub>0</sub> [10]	Y <sub>1</sub> [10]	VPC[6]	C <sub>B</sub> [10]	C <sub>R</sub> [10]		
VPA[7]	C <sub>B</sub> [3]	C <sub>R</sub> [3]	VPB[7]	Y <sub>0</sub> [11]	Y <sub>1</sub> [11]	VPC[7]	C <sub>B</sub> [11]	C <sub>R</sub> [11]		



**Fig 9. Pixel encoding YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar external synchronization (rising edge) input**

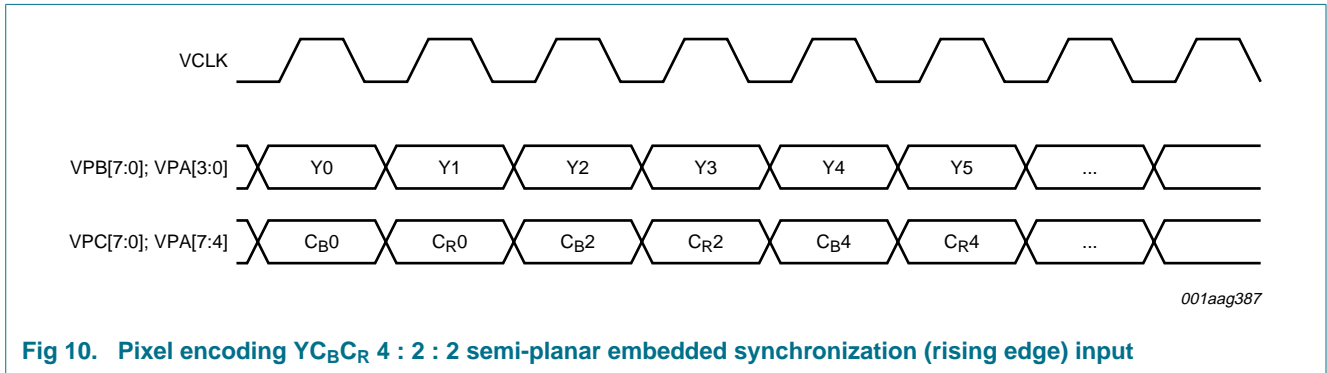


**Table 13. YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar embedded synchronization mappings**

YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar embedded synchronization single edge.

Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 semi-planar		Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 semi-planar		Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2 semi-planar		Pin	YC <sub>B</sub> C <sub>R</sub> 4 : 2 : 2
VPA[0]	Y <sub>0</sub> [0]	Y <sub>1</sub> [0]	VPB[0]	Y <sub>0</sub> [4]	Y <sub>1</sub> [4]	VPC[0]	C <sub>B</sub> [4]	C <sub>R</sub> [4]	HSYNC/HREF	not used
VPA[1]	Y <sub>0</sub> [1]	Y <sub>1</sub> [1]	VPB[1]	Y <sub>0</sub> [5]	Y <sub>1</sub> [5]	VPC[1]	C <sub>B</sub> [5]	C <sub>R</sub> [5]	VSYNC/VREF	not used
VPA[2]	Y <sub>0</sub> [2]	Y <sub>1</sub> [2]	VPB[2]	Y <sub>0</sub> [6]	Y <sub>1</sub> [6]	VPC[2]	C <sub>B</sub> [6]	C <sub>R</sub> [6]	DE/FREF	not used
VPA[3]	Y <sub>0</sub> [3]	Y <sub>1</sub> [3]	VPB[3]	Y <sub>0</sub> [7]	Y <sub>1</sub> [7]	VPC[3]	C <sub>B</sub> [7]	C <sub>R</sub> [7]		
VPA[4]	C <sub>B</sub> [0]	C <sub>R</sub> [0]	VPB[4]	Y <sub>0</sub> [8]	Y <sub>1</sub> [8]	VPC[4]	C <sub>B</sub> [8]	C <sub>R</sub> [8]		
VPA[5]	C <sub>B</sub> [1]	C <sub>R</sub> [1]	VPB[5]	Y <sub>0</sub> [9]	Y <sub>1</sub> [9]	VPC[5]	C <sub>B</sub> [9]	C <sub>R</sub> [9]		
VPA[6]	C <sub>B</sub> [2]	C <sub>R</sub> [2]	VPB[6]	Y <sub>0</sub> [10]	Y <sub>1</sub> [10]	VPC[6]	C <sub>B</sub> [10]	C <sub>R</sub> [10]		
VPA[7]	C <sub>B</sub> [3]	C <sub>R</sub> [3]	VPB[7]	Y <sub>0</sub> [11]	Y <sub>1</sub> [11]	VPC[7]	C <sub>B</sub> [11]	C <sub>R</sub> [11]		



**Fig 10. Pixel encoding YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar embedded synchronization (rising edge) input**

### 8.3 Synchronization

The TDA9981A can be synchronized with Hsync/Vsync external inputs or with extraction of the sync information from embedded sync (SAV/EAV) codes inside the video stream.

#### 8.3.1 Timing extraction generator

This block can extract the synchronization signals Href, Vref and Fref from Start Active Video (SAV) and End Active Video (EAV) in case of embedded synchronization in the data stream. Synchronization signals can be embedded in RGB, YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4, YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar (up to 2 × 12-bit), YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656 and ITU656-like (up to 1 × 12-bit).

#### 8.3.2 Data enable generator

The TDA9981A contains a Data Enable (DE) generator; this can generate an internal DE signal for a system which does not provide one.

### 8.4 Input and output video format

Due to the flexible video input formatter, the TDA9981A can accept a large range of input formats. This flexibility allows the TDA9981A to be compatible with the maximum possible number of MPEG decoders. Moreover, these input formats may be changed in many ways (color space converter, upsampler and downsampler) to be transmitted across the HDMI link. [Table 14](#) gives the possible inputs and outputs.

**Table 14. Use of color space converter, upsampler and downsampler**

Input			Output		
Color space	Format	Channels	Color space	Format	Channels
RGB	4 : 4 : 4	3 × 8-bit	RGB	4 : 4 : 4	3 × 8-bit
			YC <sub>B</sub> C <sub>R</sub>	4 : 2 : 2	2 × 12-bit
			YC <sub>B</sub> C <sub>R</sub>	4 : 4 : 4	3 × 8-bit
YC <sub>B</sub> C <sub>R</sub>	4 : 4 : 4	3 × 8-bit	RGB	4 : 4 : 4	3 × 8-bit
			YC <sub>B</sub> C <sub>R</sub>	4 : 2 : 2	2 × 12-bit
			YC <sub>B</sub> C <sub>R</sub>	4 : 4 : 4	3 × 8-bit
YC <sub>B</sub> C <sub>R</sub>	4 : 2 : 2	up to 1 × 12-bit	YC <sub>B</sub> C <sub>R</sub>	4 : 2 : 2	2 × 12-bit
			YC <sub>B</sub> C <sub>R</sub>	4 : 4 : 4	3 × 8-bit
			RGB	4 : 4 : 4	3 × 8-bit
		up to 2 × 12-bit	YC <sub>B</sub> C <sub>R</sub>	4 : 2 : 2	2 × 12-bit
			YC <sub>B</sub> C <sub>R</sub>	4 : 4 : 4	3 × 8-bit
			RGB	4 : 4 : 4	3 × 8-bit

### 8.5 Upsampler

The incoming YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 (2 × 12-bit) data stream format could be upsampled into a 12-bit YC<sub>B</sub>C<sub>R</sub> 4 : 4 : 4 (3 × 12-bit) data stream by repeating or linearly interpolating the chrominance pixels.

### 8.6 Color space converter

The color space converter is used to convert input video data from one type to another color space (RGB to YC<sub>B</sub>C<sub>R</sub> and YC<sub>B</sub>C<sub>R</sub> to RGB). This block can be bypassed and each coefficient is programmable via the I<sup>2</sup>C-bus register.

$$\begin{bmatrix} Y \setminus G \\ C_B \setminus R \\ C_R \setminus B \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left( \begin{bmatrix} G \setminus Y \\ R \setminus C_B \\ B \setminus C_R \end{bmatrix} + \begin{bmatrix} Oin_{G \setminus Y} \\ Oin_{R \setminus C_B} \\ Oin_{B \setminus C_R} \end{bmatrix} \right) + \begin{bmatrix} Oout_{Y \setminus G} \\ Oout_{C_B \setminus R} \\ Oout_{C_R \setminus B} \end{bmatrix}$$

### 8.7 Downsampler

This block works only with YC<sub>B</sub>C<sub>R</sub> input format; these filters downsample the C<sub>B</sub> and C<sub>R</sub> signals by a factor 2. A delay is added on the G/Y channel, which corresponds to the pipeline delay of the filters, to put the Y channel in phase with the C<sub>B</sub>-C<sub>R</sub> channel.

### 8.8 Audio input format

The TDA9981A is compatible with HDMI 1.2a (DVD support). The TDA9981A can carry audio in I<sup>2</sup>S-bus format (one stereo up to four stereo channels) or in S/PDIF format. S/PDIF or I<sup>2</sup>S-bus format can be selected via the I<sup>2</sup>C-bus. Only one audio format can be used at a time: either S/PDIF or I<sup>2</sup>S-bus. [Table 15](#) shows the audio port allocation.

**Table 15. Audio port configuration**

All audio ports are LV-TTL compatible.

Audio port	I <sup>2</sup> S-bus and S/PDIF input configuration
AP0	WS (word select)
AP1	I <sup>2</sup> S-bus port 0
AP2	I <sup>2</sup> S-bus port 1
AP3	I <sup>2</sup> S-bus port 2
AP4	I <sup>2</sup> S-bus port 3
AP5	MCLK (master clock for S/PDIF)
AP6	S/PDIF input
AP7	AUX (internal test)
ACLK	SCK (I <sup>2</sup> S-bus clock)

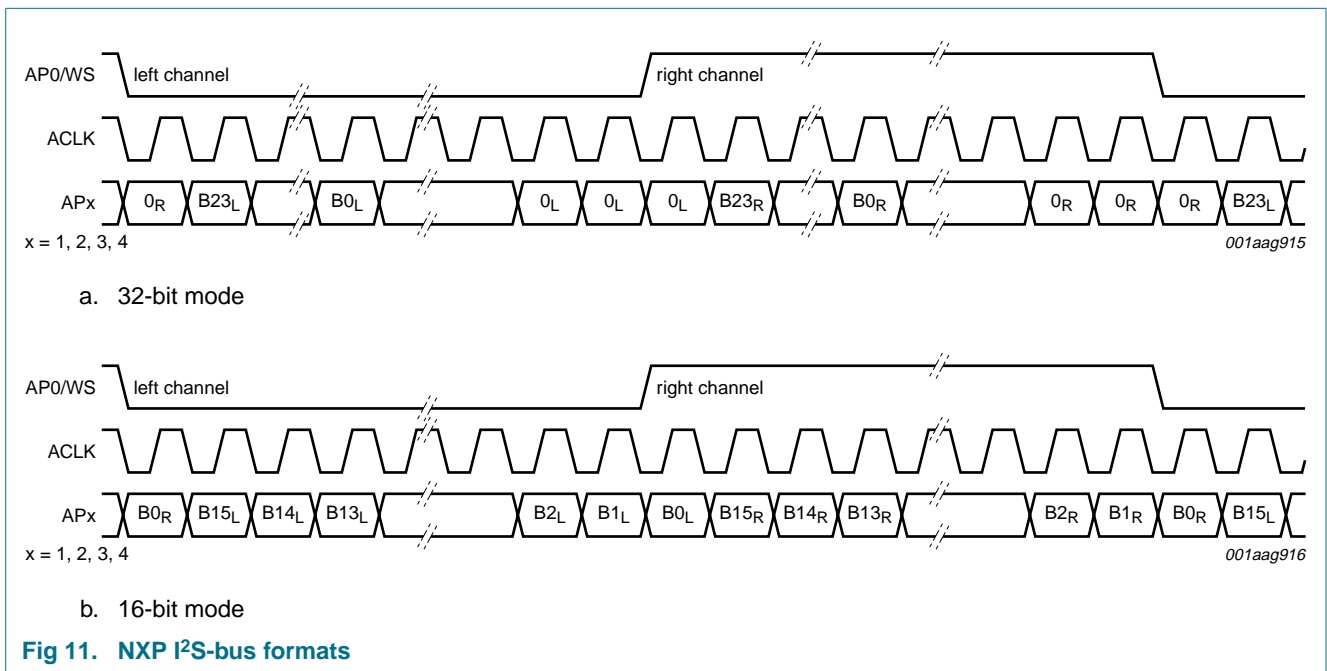
### 8.9 S/PDIF

The audio port AP6 is used for the S/PDIF feature. In this format the TDA9981A supports 2-channel uncompressed PCM data (IEC 60958) layout 0 or compressed bit stream up to 8 multichannels (Dolby Digital, DTS, AC-3, etc.) layout 1. The TDA9981A is able to recover the original clock from the S/PDIF signal (no need for an external clock). In addition it can also use an external clock (MCLK) to decode the S/PDIF signal.

### 8.10 I<sup>2</sup>S-bus

The TDA9981A supports the NXP I<sup>2</sup>S-bus format. There are four I<sup>2</sup>S-bus stereo input channels (AP1 to AP4), which enable 8 uncompressed audio channels to be carried. The I<sup>2</sup>S-bus input interface receives an I<sup>2</sup>S-bus signal including serial data, word select and

serial clock. Various I<sup>2</sup>S-bus formats are supported and can be selected by setting the appropriate bits of the register. The I<sup>2</sup>S-bus input interface can receive up to 24-bit wide audio samples via the serial data input with a clock frequency of at least 32 times the input sample frequency  $f_s$ . Since the I<sup>2</sup>S-bus format is MSB aligned, audio data with an arbitrary precision can be received automatically. Audio samples with a precision better than 24 bits are truncated to 24 bits. If the input clock has a frequency of  $32 \times f_s$ , only 16-bit audio samples can be received. In this case, the 8 LSBs will be set to logic 0. The serial data signal carries the serial baseband audio data, sample by sample left/right interleaved. The word select signal WS indicates whether left or right channel information is transferred over the serial data line. The formats for 16-bit and 32-bit modes are shown in Figure 11.



### 8.11 Power management

The TDA9981A can be powered down via the I<sup>2</sup>C-bus register.

### 8.12 Interrupt controller

Pin INT is used to alert the microcontroller that a critical event concerning the HDMI has occurred (hot plug detect, HDCP authentication error, Bstatus, SHA-1 calculation status, Bcaps ready). These interrupts are maskable.

Hot plug or unplug detect: pin HPD is the hot plug detection pin; it is 5 V input tolerant.

### 8.13 Initialization

Hard reset: after power-up, the TDA9981A is activated by a hard reset via pin RST\_N. However, the TDA9981A has a power-on reset.

**8.14 High-bandwidth digital content protection**

The HDMI transmitter contains an HDCP function which encrypts the transmitted stream content (video and audio); this function can be disabled via the I<sup>2</sup>C-bus. The keys can be stored internally in OTP non-volatile memory or can be loaded via the I<sup>2</sup>C-bus. If the keys are stored internally, the security is maximized.

**8.14.1 Repeater function**

The TDA9981A can be used in a repeater device according to *HDCP 1.1 specification* and *HDMI 1.2a specification*.

The TDA9981A can handle up to 9 devices connected downstream.

**8.14.2 SHA-1**

To deal with the repeater, a SHA-1 calculation is performed by the transmitter and by the downstream repeater. For security purposes and in order to relieve the microcontroller, the SHA-1 has been implemented within the TDA9981A. This calculation is worked out after the transmitter has loaded the KSV list (see *HDCP 1.1 specification*). If the SHA-1 calculated by the transmitter equals the SHA-1 calculated by the repeater, then an interrupt (register INT\_FLAGS\_0, bit SHA-1) is sent.

**8.15 HDMI**

**8.15.1 Output HDMI buffers**

An external resistor must be used to set the HDMI output amplitude. It has to be connected between pin EXT\_SWING and V<sub>DDH(3V3)</sub>.

**8.15.2 Pixel repetition**

To transmit video formats with pixel rates below 25 Msample/s or to increase the number of audio sample packets in each frame, the TDA9981A uses pixel repetition to increase the transmitted pixel clock.

**Table 16. Pixel repetition**

PIX_REP[3]	PIX_REP[2]	PIX_REP[1]	PIX_REP[0]	Pixel repeated
0	0	0	0	no repetition
0	0	0	1	once
0	0	1	0	twice
0	0	1	1	3 times
0	1	0	0	4 times
0	1	0	1	5 times
0	1	1	0	6 times
0	1	1	1	7 times
1	0	0	0	8 times
1	0	0	1	9 times
1	0	1	x	undefined
1	1	x	x	undefined

**8.15.3 HDMI and DVI receiver discrimination**

This information is located in the E-EDID receiver part, in the 'Vendor-Specific Datablock' within the first CEA EDID timing extension. If the 24-bit IEEE registration identifier contains the value 00 0C03h, then the receiver will support HDMI, otherwise the device will be treated as a DVI device. However, the TDA9981A does not have direct access to that information since E-EDID is read by an external microprocessor through the TDA9981A I<sup>2</sup>C-bus gate.

**8.15.4 DDC channel**

The DDC-bus pins DDC\_SDA and DDC\_SCL are 5 V tolerant and can work at standard mode (100 kHz).

**8.15.4.1 E-EDID reading**

In order to get receiver capabilities, the TDA9981A must read the E-EDID of the receiver. This is made possible by temporarily connecting the I<sup>2</sup>C-bus to the DDC lines, so that the microprocessor is able to read full EDID.

**8.15.4.2 HDCP processing**

The DDC channel is used for the HDCP process. In this mode, the DDC channel behavior is based on the I<sup>2</sup>C-bus protocol and the transmitter works as a master.

**8.16 I<sup>2</sup>C-bus interface**

The I<sup>2</sup>C-bus pins I2C\_SDA and I2C\_SCL are 5 V tolerant and can work at fast mode (400 kHz).

**9. I<sup>2</sup>C–bus register definitions**

**9.1 I<sup>2</sup>C-bus protocol**

The registers of the TDA9981A can be accessed via the I<sup>2</sup>C-bus. The TDA9981A is used as a slave device and both the fast mode 400 kHz and the standard mode 100 kHz are supported.

Bits A0 and A1 of the I<sup>2</sup>C-bus device address are externally selected by pins A0 and A1. The I<sup>2</sup>C-bus device address is given in [Table 17](#).

**Table 17. Device address**

Device address							R/W
A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	0	A1	A0	1/0

The I<sup>2</sup>C-bus access format is shown in [Figure 12](#).

For read access, the master writes the address of the TDA9981A, the subaddress to access the specific register and then the data.

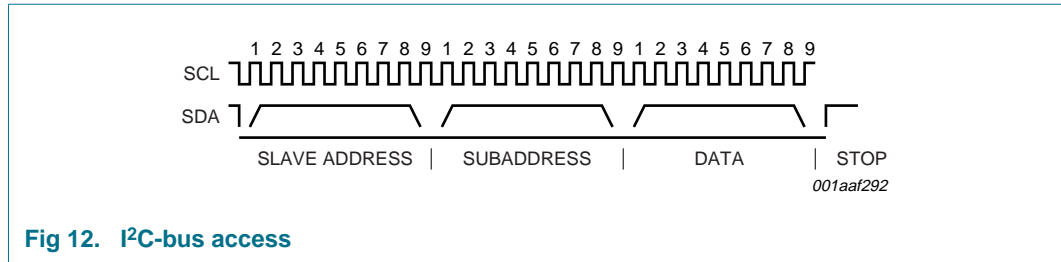


Fig 12. I<sup>2</sup>C-bus access

## 10. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD(3V3)</sub>	supply voltage (3.3 V)		-0.5	+4.6	V
V <sub>DD(1V8)</sub>	supply voltage (1.8 V)		-0.5	+2.5	V
ΔV <sub>DD</sub>	supply voltage difference		-0.5	+0.5	V
T <sub>stg</sub>	storage temperature		-55	+150	°C
T <sub>amb</sub>	ambient temperature		0	85	°C
T <sub>j</sub>	junction temperature		-	125	°C
V <sub>esd</sub>	electrostatic discharge voltage	HBM	-2000	+2000	V

## 11. Thermal characteristics

Table 19. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air; JEDEC 4L board	50.6	K/W
R <sub>th(j-c)</sub>	thermal resistance from junction to case		16.2	K/W

## 12. Static characteristics

**Table 20. Supplies**

$V_{DDA(FRO\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDA(PLL\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDH(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDD(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDC(1V8)} = 1.65\text{ V to }1.95\text{ V}$ ;  $V_{PP} = 0\text{ V}$ ;  $T_{amb} = 0\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ .

Typical values are measured at  $V_{DDA(FRO\_3V3)} = V_{DDA(PLL\_3V3)} = V_{DDH(3V3)} = V_{DDD(3V3)} = 3.3\text{ V}$ ;  $V_{DDC(1V8)} = 1.8\text{ V}$ ;  $V_{PP} = 0\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TDA9981AHL/8 and TDA9981AHL/15</b>						
$V_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply voltage		3.0	3.3	3.6	V
$V_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply voltage		3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.65	1.8	1.95	V
<b>TDA9981AHL/8; up to 81 MHz</b>						
$I_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply current		-	-	0.5	mA
$I_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply current	[1]	-	3.5	4.5	mA
$I_{DDD(3V3)}$	digital supply current (3.3 V)		-	-	1.5	mA
$I_{DDH(3V3)}$	HDMI supply current (3.3 V)		-	14	14.5	mA
$I_{DDC(1V8)}$	core supply current (1.8 V)	[1]	-	94	107.5	mA
$f_{clk(max)}$	maximum clock frequency	[1]	81	-	-	MHz
$P_{cons}$	power consumption	[1]	-	235	288	mW
$P_{tot}$	total power dissipation	[1]	-	369	438	mW
$P_{pd}$	power dissipation in Power-down mode		-	14	19	mW
<b>TDA9981AHL/15; up to 150 MHz</b>						
$I_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply current		-	-	0.5	mA
$I_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply current	[2]	-	4	5	mA
$I_{DDD(3V3)}$	digital supply current (3.3 V)		-	-	3.5	mA
$I_{DDH(3V3)}$	HDMI supply current (3.3 V)		-	14	15	mA
$I_{DDC(1V8)}$	core supply current (1.8 V)	[2]	-	175	200	mA
$f_{clk(max)}$	maximum clock frequency	[2]	150	-	-	MHz
$P_{cons}$	power consumption	[2]	-	381.5	468	mW
$P_{tot}$	total power dissipation	[2]	-	515.5	618	mW
$P_{pd}$	power dissipation in Power-down mode		-	14	19	mW

[1] Worst case: video input format: 720p at 60 Hz (RGB 4 : 4 : 4 embedded sync), video output format: 720p at 60 Hz (YCbCr 4 : 4 : 4).

[2] Video input format: 1080p (RGB 4 : 4 : 4 embedded sync, rising edge), video output format: 1080p (RGB 4 : 4 : 4).



**Table 21. LV-TTL digital inputs and outputs**

$V_{DDA(FRO\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDA(PLL\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDH(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDD(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDC(1V8)} = 1.65\text{ V to }1.95\text{ V}$ ;  $V_{PP} = 0\text{ V}$ ;  $T_{amb} = 0\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ .

Typical values are measured at  $V_{DDA(FRO\_3V3)} = V_{DDA(PLL\_3V3)} = V_{DDH(3V3)} = V_{DDD(3V3)} = 3.3\text{ V}$ ;  $V_{DDC(1V8)} = 1.8\text{ V}$ ;  $V_{PP} = 0\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Not 5 V tolerant inputs: pins HSYNC, VSYNC, AP[7:0], ACLK, TM, A0, A1, VPA[7:0], VPB[7:0], VPC[7:0], VCLK, DE and RST_N</b>						
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$I_{IL}$	LOW-level input current		-1	-	+1	$\mu\text{A}$
$I_{IH}$	HIGH-level input current		-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance		-	4.5	-	pF
<b>5 V tolerant input: pin HPD</b>						
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$C_i$	input capacitance		-	4.5	-	pF
<b>Output: pin INT</b>						
$V_{OL}$	LOW-level output voltage	$C_L = 10\text{ pF}$ ; $I_{OL} = 2\text{ mA}$	-	-	0.4	V

**Table 22. TMDS outputs**

$V_{DDA(FRO\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDA(PLL\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDH(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDD(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDC(1V8)} = 1.65\text{ V to }1.95\text{ V}$ ;  $V_{PP} = 0\text{ V}$ ;  $T_{amb} = 0\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ .

Typical values are measured at  $V_{DDA(FRO\_3V3)} = V_{DDA(PLL\_3V3)} = V_{DDH(3V3)} = V_{DDD(3V3)} = 3.3\text{ V}$ ;  $V_{DDC(1V8)} = 1.8\text{ V}$ ;  $V_{PP} = 0\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TMDS output pins: TX0-, TX0+, TX1-, TX1+, TX2-, TX2+, TXC- and TXC+</b>						
$V_{o(p-p)}$	peak-to-peak output voltage	single output; $R_{ext} = 610\ \Omega$	400	510	600	mV
$V_{OH}$	HIGH-level output voltage	(1 % tolerance) with test load and operating condition as in <i>HDMI</i>	3.125	3.3	3.475	V
$V_{OL}$	LOW-level output voltage	1.2a specification	2.535	2.79	3.065	V

### 13. Dynamic characteristics

**Table 23. Timing characteristics**

$V_{DDA(FRO\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDA(PLL\_3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDH(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDD(3V3)} = 3.0\text{ V to }3.6\text{ V}$ ;  $V_{DDC(1V8)} = 1.65\text{ V to }1.95\text{ V}$ ;  $V_{PP} = 0\text{ V}$ ;  $T_{amb} = 0\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ .

Typical values are measured at  $V_{DDA(FRO\_3V3)} = V_{DDA(PLL\_3V3)} = V_{DDH(3V3)} = V_{DDD(3V3)} = 3.3\text{ V}$ ;  $V_{DDC(1V8)} = 1.8\text{ V}$ ;  $V_{PP} = 0\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Clock inputs: pins VCLK, VPA[7:0], VPB[7:0] and VPC[7:0]; see Figure 13, 14, 16 and 17</b>						
$f_{clk(max)}$	maximum clock frequency	TDA9981AHL/8	81	-	-	MHz
		TDA9981AHL/15	150	-	-	MHz
$t_{su(D)}$	data input set-up time		-0.25	-	-	ns
$t_{h(D)}$	data input hold time		2.20	-	-	ns
$\delta_{clk}$	clock duty cycle		[1] 40	-	60	%
<b>DDC I<sup>2</sup>C-bus; 5 V tolerant; master bus: pins DDC_SDA and DDC_SCL</b>						
$f_{SCL}$	SCL clock frequency	standard mode	-	-	100	kHz
$C_i$	capacitance for each I/O pin		-	7	-	pF
<b>I<sup>2</sup>C-bus; 5 V tolerant; master bus: pins I2C_SDA and I2C_SCL</b>						
$f_{SCL}$	SCL clock frequency	standard mode	-	-	100	kHz
		fast mode	-	-	400	kHz
$C_i$	capacitance for each I/O pin		-	7	-	pF
<b>TMDS output pins: TXC- and TXC+</b>						
$f_{clk(max)}$	maximum clock frequency	TDA9981AHL/8	81	-	-	MHz
		TDA9981AHL/15	150	-	-	MHz
<b>TMDS output pins: TX0-, TX0+, TX1-, TX1+, TX2- and TX2+</b>						
$f_{clk(max)}$	maximum clock frequency	TDA9981AHL/8	810	-	-	MHz
		TDA9981AHL/15	1.5	-	-	GHz

[1]  $\delta_{clk} = t_{clk(H)} / (t_{clk(H)} + t_{clk(L)})$ .

### 13.1 Input format

In [Table 24](#) the port VPA has been mapped to C<sub>B</sub> (YUV space)/B (RGB space), VPB has been mapped to Y (YUV space)/G (RGB space) and VPC has been mapped to C<sub>R</sub> (YUV space)/R (RGB space).

Table 24. Input format

Input pins	Signal	RGB	YUV						
		4 : 4 : 4 <sup>[1]</sup>	4 : 4 : 4 <sup>[2]</sup>	4 : 2 : 2 (semi-planar) <sup>[3]</sup>	4 : 2 : 2 (ITU656-like) <sup>[4]</sup>				
<b>Video port A</b>									
VPA[0]	C <sub>B</sub> [0]/B[0]	B[0]	C <sub>B</sub> [0]	Y <sub>0</sub> [0]	Y <sub>1</sub> [0]	C <sub>B</sub> [0]	Y <sub>0</sub> [0]	C <sub>R</sub> [0]	Y <sub>1</sub> [0]
VPA[1]	C <sub>B</sub> [1]/B[1]	B[1]	C <sub>B</sub> [1]	Y <sub>0</sub> [1]	Y <sub>1</sub> [1]	C <sub>B</sub> [1]	Y <sub>0</sub> [1]	C <sub>R</sub> [1]	Y <sub>1</sub> [1]
VPA[2]	C <sub>B</sub> [2]/B[2]	B[2]	C <sub>B</sub> [2]	Y <sub>0</sub> [2]	Y <sub>1</sub> [2]	C <sub>B</sub> [2]	Y <sub>0</sub> [2]	C <sub>R</sub> [2]	Y <sub>1</sub> [2]
VPA[3]	C <sub>B</sub> [3]/B[3]	B[3]	C <sub>B</sub> [3]	Y <sub>0</sub> [3]	Y <sub>1</sub> [3]	C <sub>B</sub> [3]	Y <sub>0</sub> [3]	C <sub>R</sub> [3]	Y <sub>1</sub> [3]
VPA[4]	C <sub>B</sub> [4]/B[4]	B[4]	C <sub>B</sub> [4]	C <sub>B</sub> [0]	C <sub>R</sub> [0]	L	L	L	L
VPA[5]	C <sub>B</sub> [5]/B[5]	B[5]	C <sub>B</sub> [5]	C <sub>B</sub> [1]	C <sub>R</sub> [1]	L	L	L	L
VPA[6]	C <sub>B</sub> [6]/B[6]	B[6]	C <sub>B</sub> [6]	C <sub>B</sub> [2]	C <sub>R</sub> [2]	L	L	L	L
VPA[7]	C <sub>B</sub> [7]/B[7]	B[7]	C <sub>B</sub> [7]	C <sub>B</sub> [3]	C <sub>R</sub> [3]	L	L	L	L
<b>Video port B</b>									
VPB[0]	Y[0]/G[0]	G[0]	Y[0]	Y <sub>0</sub> [4]	Y <sub>1</sub> [4]	C <sub>B</sub> [4]	Y <sub>0</sub> [4]	C <sub>R</sub> [4]	Y <sub>1</sub> [4]
VPB[1]	Y[1]/G[1]	G[1]	Y[1]	Y <sub>0</sub> [5]	Y <sub>1</sub> [5]	C <sub>B</sub> [5]	Y <sub>0</sub> [5]	C <sub>R</sub> [5]	Y <sub>1</sub> [5]
VPB[2]	Y[2]/G[2]	G[2]	Y[2]	Y <sub>0</sub> [6]	Y <sub>1</sub> [6]	C <sub>B</sub> [6]	Y <sub>0</sub> [6]	C <sub>R</sub> [6]	Y <sub>1</sub> [6]
VPB[3]	Y[3]/G[3]	G[3]	Y[3]	Y <sub>0</sub> [7]	Y <sub>1</sub> [7]	C <sub>B</sub> [7]	Y <sub>0</sub> [7]	C <sub>R</sub> [7]	Y <sub>1</sub> [7]
VPB[4]	Y[4]/G[4]	G[4]	Y[4]	Y <sub>0</sub> [8]	Y <sub>1</sub> [8]	C <sub>B</sub> [8]	Y <sub>0</sub> [8]	C <sub>R</sub> [8]	Y <sub>1</sub> [8]
VPB[5]	Y[5]/G[5]	G[5]	Y[5]	Y <sub>0</sub> [9]	Y <sub>1</sub> [9]	C <sub>B</sub> [9]	Y <sub>0</sub> [9]	C <sub>R</sub> [9]	Y <sub>1</sub> [9]
VPB[6]	Y[6]/G[6]	G[6]	Y[6]	Y <sub>0</sub> [10]	Y <sub>1</sub> [10]	C <sub>B</sub> [10]	Y <sub>0</sub> [10]	C <sub>R</sub> [10]	Y <sub>1</sub> [10]
VPB[7]	Y[7]/G[7]	G[7]	Y[7]	Y <sub>0</sub> [11]	Y <sub>1</sub> [11]	C <sub>B</sub> [11]	Y <sub>0</sub> [11]	C <sub>R</sub> [11]	Y <sub>1</sub> [11]
<b>Video port C</b>									
VPC[0]	C <sub>R</sub> [0]/R[0]	R[0]	C <sub>R</sub> [0]	C <sub>B</sub> [4]	C <sub>R</sub> [4]	L	L	L	L
VPC[1]	C <sub>R</sub> [1]/R[1]	R[1]	C <sub>R</sub> [1]	C <sub>B</sub> [5]	C <sub>R</sub> [5]	L	L	L	L
VPC[2]	C <sub>R</sub> [2]/R[2]	R[2]	C <sub>R</sub> [2]	C <sub>B</sub> [6]	C <sub>R</sub> [6]	L	L	L	L
VPC[3]	C <sub>R</sub> [3]/R[3]	R[3]	C <sub>R</sub> [3]	C <sub>B</sub> [7]	C <sub>R</sub> [7]	L	L	L	L
VPC[4]	C <sub>R</sub> [4]/R[4]	R[4]	C <sub>R</sub> [4]	C <sub>B</sub> [8]	C <sub>R</sub> [8]	L	L	L	L
VPC[5]	C <sub>R</sub> [5]/R[5]	R[5]	C <sub>R</sub> [5]	C <sub>B</sub> [9]	C <sub>R</sub> [9]	L	L	L	L
VPC[6]	C <sub>R</sub> [6]/R[6]	R[6]	C <sub>R</sub> [6]	C <sub>B</sub> [10]	C <sub>R</sub> [10]	L	L	L	L
VPC[7]	C <sub>R</sub> [7]/R[7]	R[7]	C <sub>R</sub> [7]	C <sub>B</sub> [11]	C <sub>R</sub> [11]	L	L	L	L

[1] Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 45h; VIP\_CNTRL\_2 = 01h.

[2] Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 45h; VIP\_CNTRL\_2 = 01h.

[3] Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 14h.

[4] Register VIP\_CNTRL\_0 = 23h; VIP\_CNTRL\_1 = 50h; VIP\_CNTRL\_2 = 00h.

### 13.2 Example of supported video

The TDA9981A supports all EIA/CEA-861B, ATSC video input formats.

**Table 25. Timing parameters for EIA/CEA-861B**

Format nr.	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition
<b>59.94 Hz systems</b>							
1 (VGA)	640 × 480p	59.9401	800	525	31.4685	25.174825	1
2, 3	720 × 480p	59.9401	858	525	31.4685	27	1
4	1280 × 720p	59.9401	1650	750	44.955	74.175824	1
5	1920 × 1080i	59.9401	2200	1125	33.7163	74.175824	1
6, 7 (NTSC)	720 × 480i	59.9401	858	525	15.7343	13.5	2
8, 9	720 × 240p	59.9401	858	262	15.7043	13.474286	2
8, 9	720 × 240p	59.9401	858	263	15.7642	13.525714	2
10, 11	720 × 480i	59.9401	858	525	15.7343	13.5	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
12, 13	720 × 240p	59.9401	858	262	15.7043	13.474286	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
12, 13	720 × 240p	59.9401	858	263	15.7642	13.525714	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
14, 15	1440 × 480p	59.9401	1716	525	31.4685	54	2
16 <sup>[1]</sup>	1920 × 1080p	59.9401	2200	1125	67.4326	148.35165 <sup>[1]</sup>	1
<b>60 Hz systems</b>							
1 (VGA)	640 × 480p	60	800	525	31.5	25.2	1
2, 3	720 × 480p	60	858	525	31.5	27.27	1
4	1280 × 720p	60	1650	750	45	74.25	1
5	1920 × 1080i	60	2200	1125	33.75	74.25	1
6, 7 (NTSC)	720 × 480i	60	858	525	15.75	13.5135	2
8, 9	720 × 240p	60	858	262	15.72	13.48776	2
8, 9	720 × 240p	60	858	263	15.78	13.53924	2
10, 11	720 × 480i	60	858	525	15.75	13.5135	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
12, 13	720 × 240p	60	858	262	15.72	13.48776	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
12, 13	720 × 240p	60	858	263	15.78	13.53924	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
14, 15	1440 × 480p	60	1716	525	31.5	54.054	2
16 <sup>[1]</sup>	1920 × 1080p	60	2200	1125	67.5	148.5 <sup>[1]</sup>	1
<b>50 Hz systems</b>							
17, 18	720 × 576p	50	864	625	31.25	27	1
19	1280 × 720p	50	1980	750	37.5	74.25	1
20	1920 × 1080i	50	2640	1125	28.125	74.25	1
21, 22 (PAL)	720 × 576i	50	864	625	15.625	13.5	2
23, 24	720 × 288p	50	864	312	15.6	13.4784	2
23, 24	720 × 288p	50	864	313	15.65	13.5216	2

Table 25. Timing parameters for EIA/CEA-861B ...continued

Format nr.	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition
23, 24	720 × 288p	50	864	314	15.7	13.5648	2
25, 26	720 × 576i	50	864	625	15.625	13.5	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
27, 28	720 × 288p	50	864	312	15.6	13.4784	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
27, 28	720 × 288p	50	864	313	15.65	13.5216	4, 5, 7 <sup>[1]</sup> , 8 <sup>[1]</sup> , 10 <sup>[1]</sup>
27, 28	720 × 288p	50	864	314	15.7	13.5648	2
29, 30	1440 × 576p	50	1728	625	31.25	54	1
31 <sup>[1]</sup>	1920 × 1080p	50	2640	1125	56.25	148.5 <sup>[1]</sup>	1
<b>Various systems</b>							
32	1920 × 1080p	23.976	2750	1125	26.973	74.175824	1
32	1920 × 1080p	24	2750	1125	27	74.25	1
33	1920 × 1080p	25	2640	1125	28.125	74.25	1
34	1920 × 1080p	29.97	2200	1125	33.716	74.175824	1
34	1920 × 1080p	30	2200	1125	33.75	74.25	1

[1] Only for TDA9981AHL/15.

Table 26. Timing parameters for PC standards below 150 MHz

Standard	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition
	640 × 350p	85.080	832	445	37.861	31.500	-
	640 × 400p	85.080	832	445	37.861	31.500	-
	720 × 400p	85.039	936	446	37.927	35.500	-
0.31M3 VGA	640 × 480p	59.940	800	525	31.469	25.175	-
	640 × 480p	72.809	832	520	37.861	31.500	-
	640 × 480p	75.000	840	500	37.500	31.500	-
	640 × 480p	85.008	832	509	43.269	36.000	-
0.48M3 SVGA	800 × 600p	56.250	1024	625	35.156	36.000	-
	800 × 600p	60.317	1056	628	37.879	40.000	-
	800 × 600p	72.188	1040	666	48.077	50.000	-
	800 × 600p	75.000	1056	625	46.875	49.500	-
	800 × 600p	85.061	1048	631	53.674	56.250	-
0.48M3-R	800 × 600p	119.972	960	636	76.302	73.250	-
0.41M9	848 × 480p	60.000	1088	517	31.020	33.750	-
0.79M3 XGA	1024 × 768p	60.004	1344	806	48.363	65.000	-
	1024 × 768p	70.069	1328	806	56.476	75.000	-
	1024 × 768p	75.029	1312	800	60.023	78.750	-
	1024 × 768p <sup>[1]</sup>	84.997	1376	808	68.677	94.500	-
	1024 × 768i	86.957	1264	817	35.522	44.900	-

Table 26. Timing parameters for PC standards below 150 MHz ...continued

Standard	Format	V frequency (Hz)	H total	V total	H frequency (kHz)	Pixel frequency (MHz)	Pixel repetition
0.79M3-R XGA <sup>[1]</sup>	1024 × 768p <sup>[1]</sup>	119.989	1184	813	97.551	115.500	-
1.00M3 <sup>[1]</sup>	1152 × 864p <sup>[1]</sup>	75.000	1600	900	67.500	108.000	-
0.98M9-R	1280 × 768p	59.995	1440	790	47.396	68.250	-
	1280 × 768p <sup>[1]</sup>	119.798	1440	813	97.396	140.250	-
0.98M9	1280 × 768p	59.870	1664	798	47.776	79.500	-
	1280 × 768p <sup>[1]</sup>	74.893	1696	805	60.289	102.250	-
	1280 × 768p <sup>[1]</sup>	84.837	1712	809	68.633	117.500	-
1.02MA-R	1280 × 800p	59.910	1440	823	49.306	71.000	-
	1280 × 800p <sup>[1]</sup>	119.909	1440	847	101.563	146.250	-
1.02MA <sup>[1]</sup>	1280 × 800p <sup>[1]</sup>	59.810	1680	831	49.702	83.500	-
	1280 × 800p <sup>[1]</sup>	74.934	1696	838	62.795	106.500	-
	1280 × 800p <sup>[1]</sup>	84.880	1712	843	71.554	122.500	-
1.23M3 <sup>[1]</sup>	1280 × 960p <sup>[1]</sup>	60.000	1800	1000	60.000	108.000	-
	1280 × 960p <sup>[1]</sup>	85.002	1728	1011	85.938	148.500	-
1.31M4 SXGA <sup>[1]</sup>	1280 × 1024p <sup>[1]</sup>	60.020	1688	1066	63.981	108.000	-
	1280 × 1024p <sup>[1]</sup>	75.025	1688	1066	79.976	135.000	-
1.04M9 <sup>[1]</sup>	1360 × 768p <sup>[1]</sup>	60.015	1792	795	47.712	85.500	-
1.04M9-R <sup>[1]</sup>	1360 × 768p <sup>[1]</sup>	119.967	1520	813	97.533	148.250	-
1.47M3-R <sup>[1]</sup>	1400 × 1050p <sup>[1]</sup>	59.948	1560	1080	64.744	101.000	-
1.47M3 <sup>[1]</sup>	1400 × 1050p <sup>[1]</sup>	59.978	1864	1089	65.317	121.750	-
1.29MA-R <sup>[1]</sup>	1440 × 900p <sup>[1]</sup>	59.901	1600	926	55.469	88.750	-
1.29MA <sup>[1]</sup>	1440 × 900p <sup>[1]</sup>	59.887	1904	934	55.935	106.500	-
	1440 × 900p <sup>[1]</sup>	74.984	1936	942	70.635	136.750	-
1.76MA-R <sup>[1]</sup>	1680 × 1050p <sup>[1]</sup>	59.883	1840	1080	64.674	119.000	-
1.76MA <sup>[1]</sup>	1680 × 1050p <sup>[1]</sup>	59.954	2240	1089	65.290	146.250	-

[1] Only for TDA9981AHL/15.

13.3 Timing diagrams

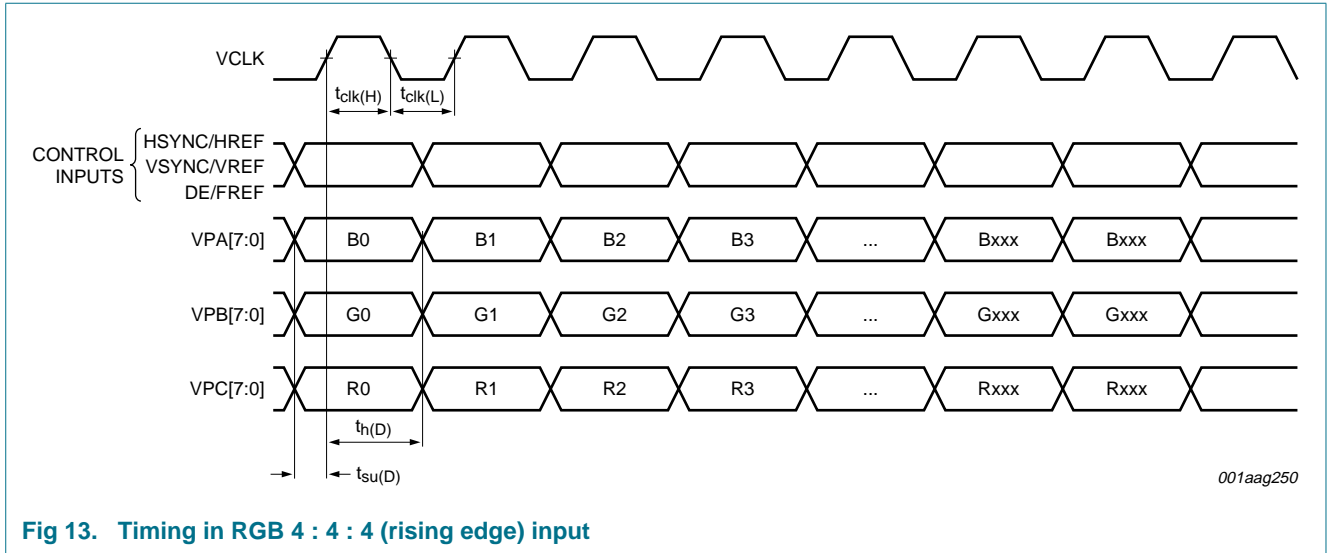


Fig 13. Timing in RGB 4 : 4 : 4 (rising edge) input

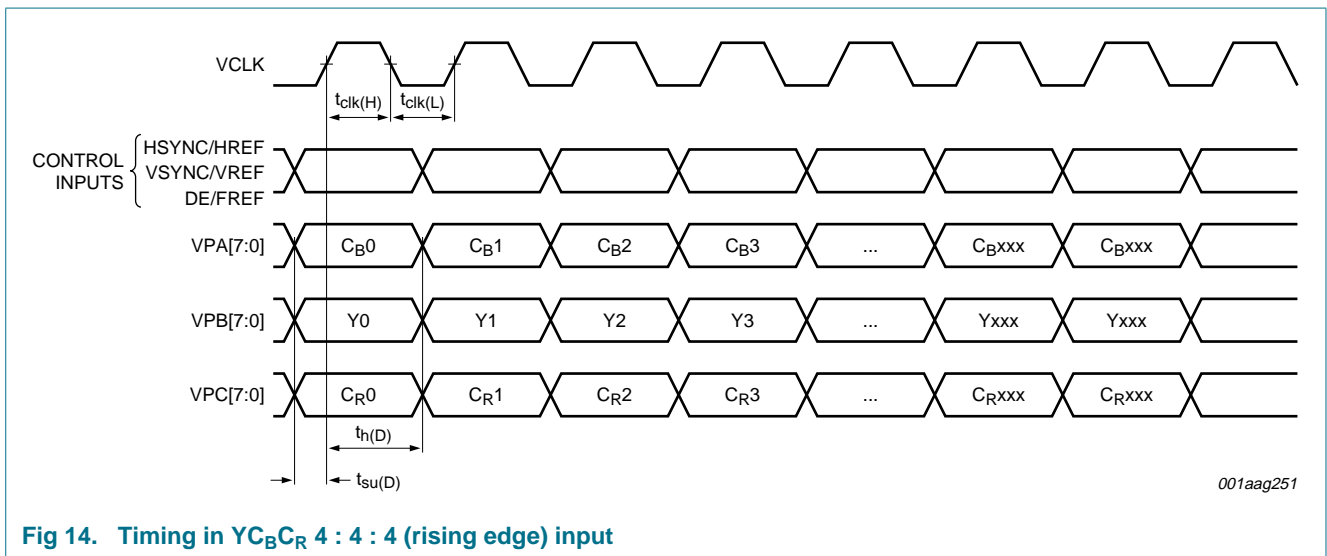


Fig 14. Timing in YCbCr 4 : 4 : 4 (rising edge) input

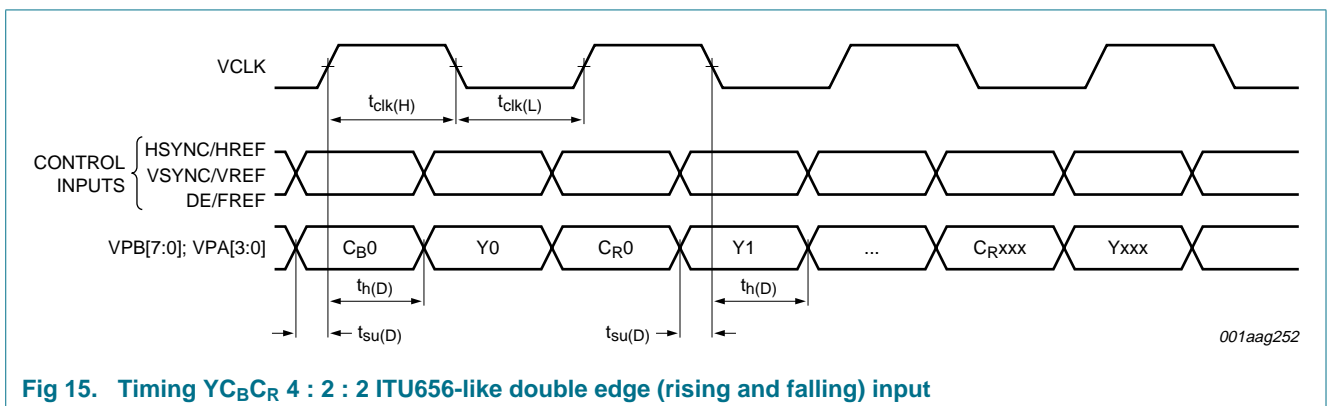


Fig 15. Timing YCbCr 4 : 2 : 2 ITU656-like double edge (rising and falling) input

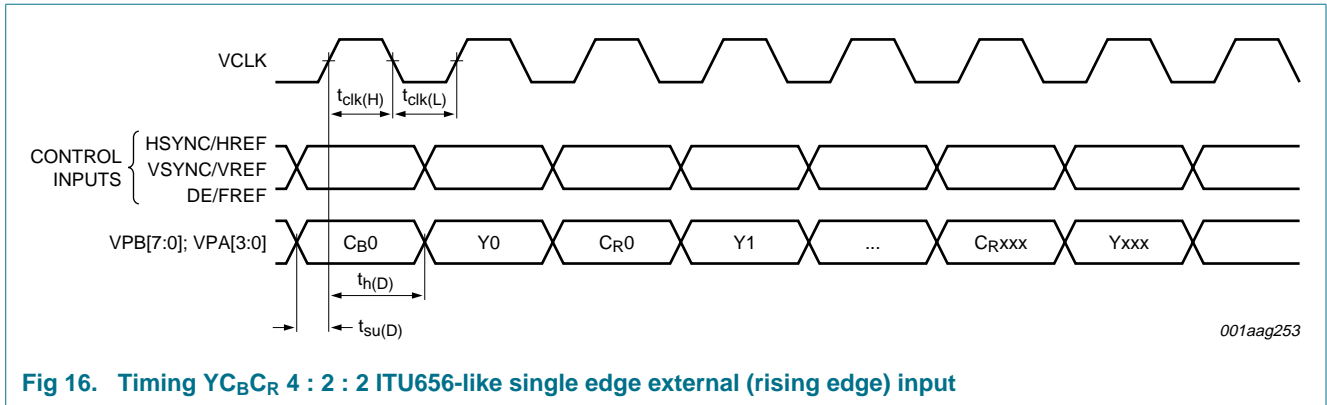


Fig 16. Timing YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 ITU656-like single edge external (rising edge) input

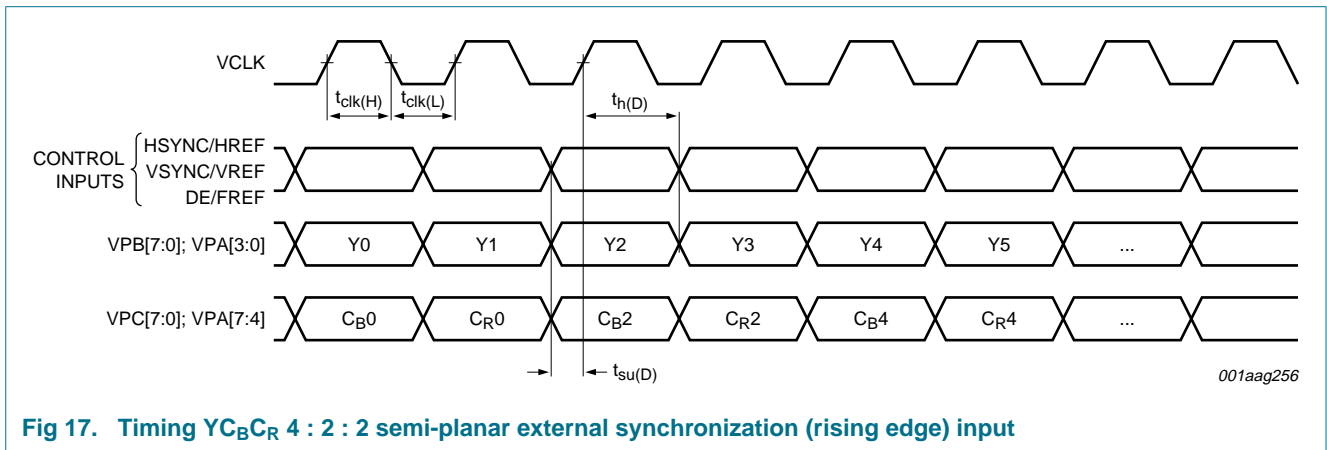


Fig 17. Timing YC<sub>B</sub>C<sub>R</sub> 4 : 2 : 2 semi-planar external synchronization (rising edge) input



### 14. Application information

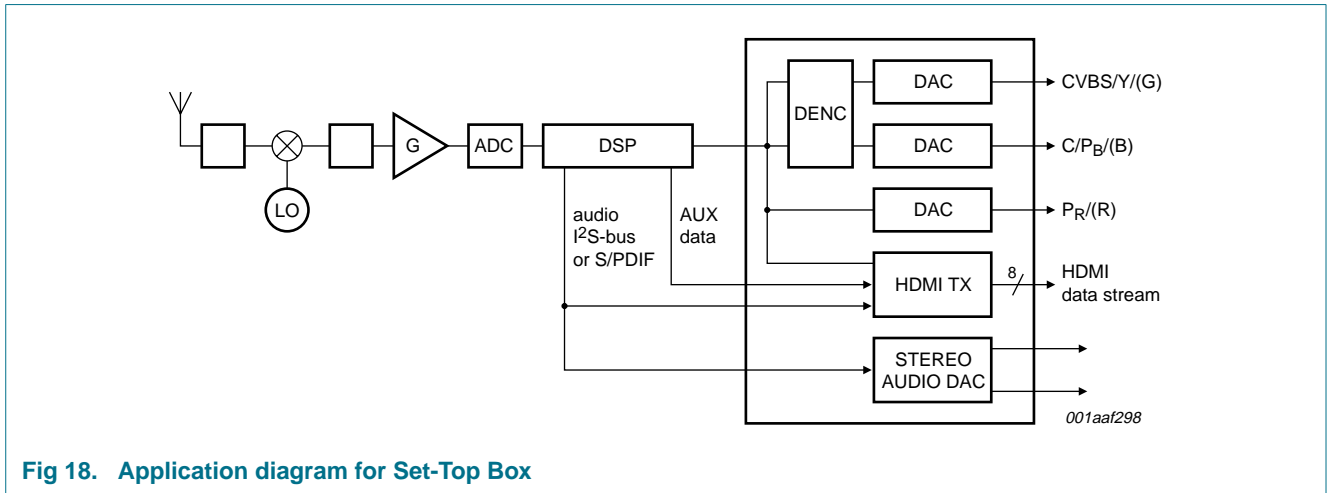


Fig 18. Application diagram for Set-Top Box

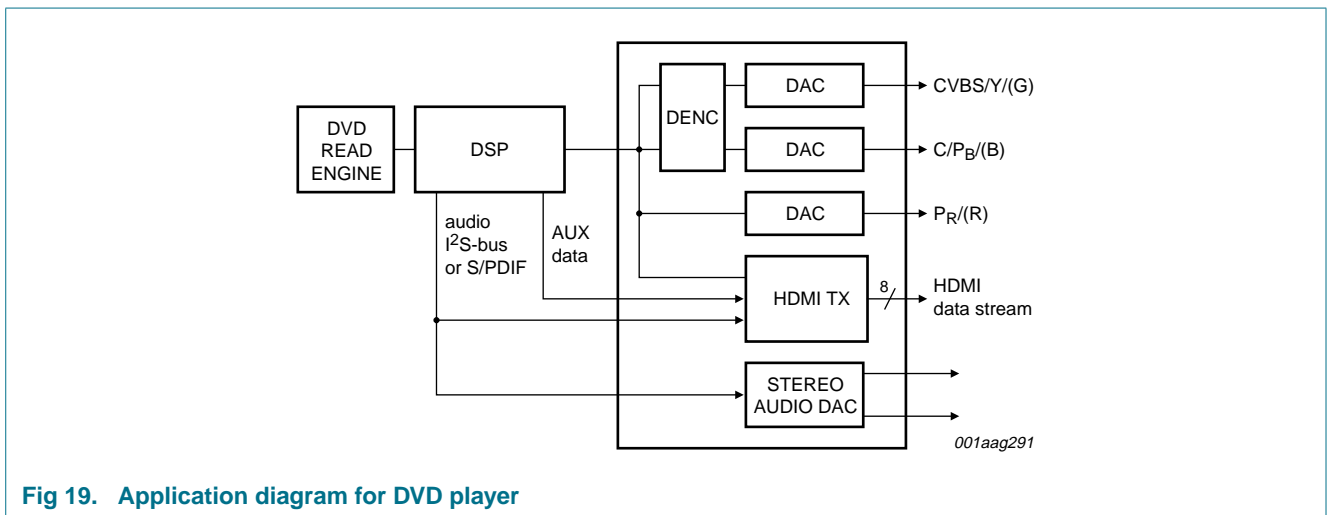


Fig 19. Application diagram for DVD player

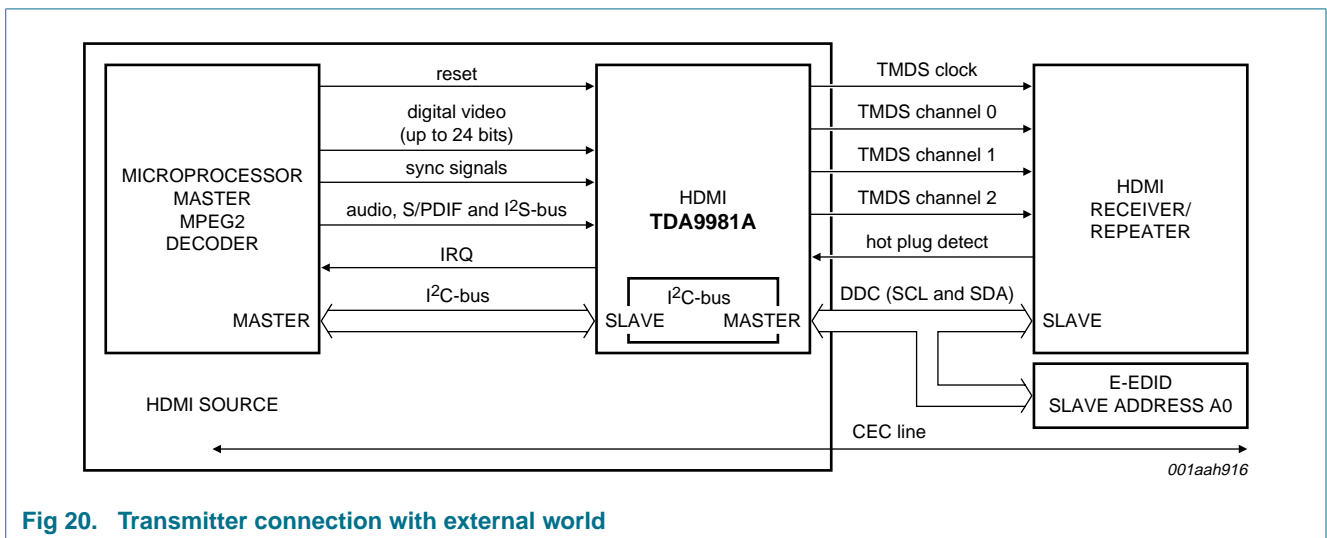


Fig 20. Transmitter connection with external world

15. Package outline

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm

SOT315-1

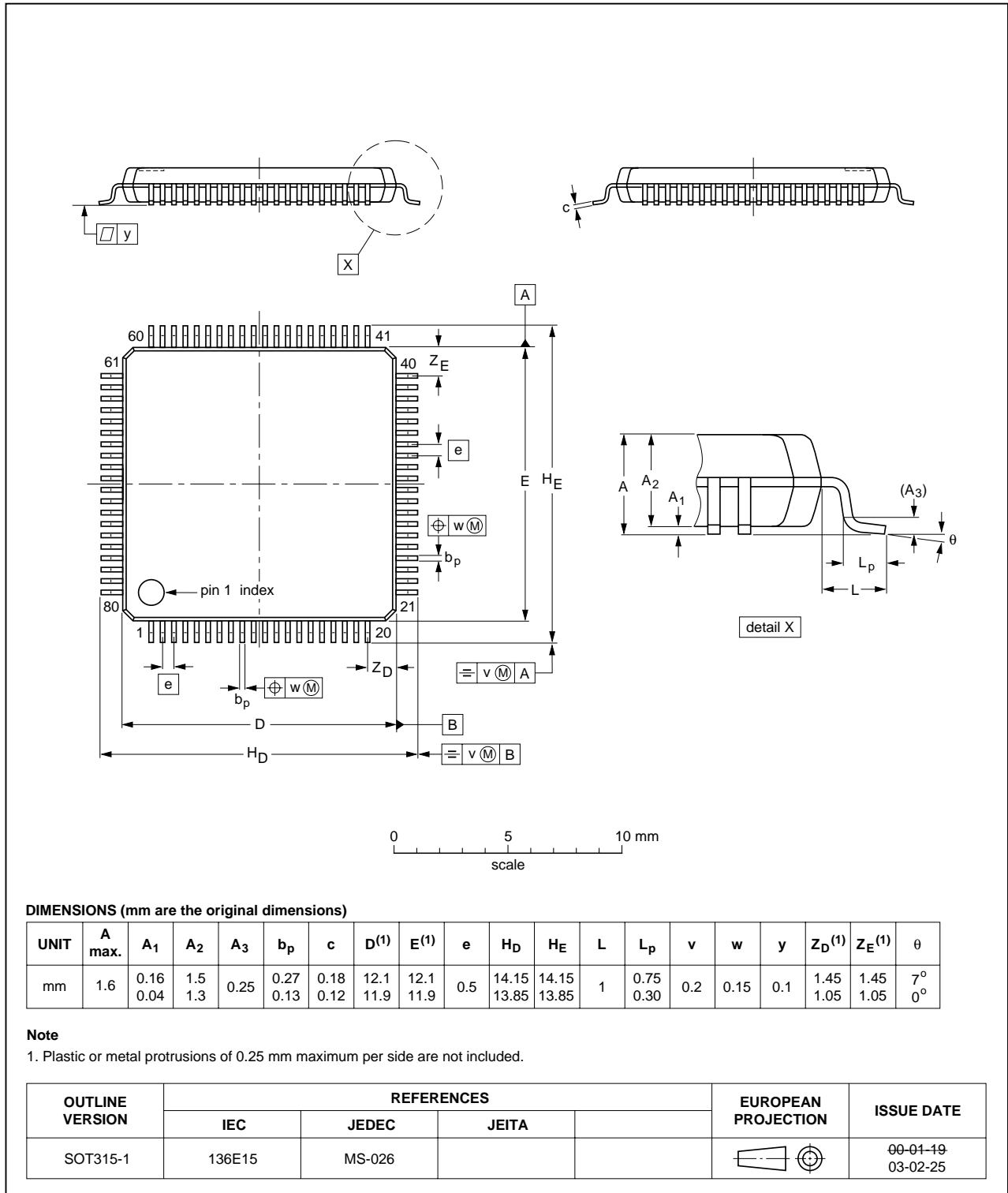


Fig 21. Package outline SOT315-1 (LQFP80)

## 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 22](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 27](#) and [28](#)

**Table 27. SnPb eutectic process (from J-STD-020C)**

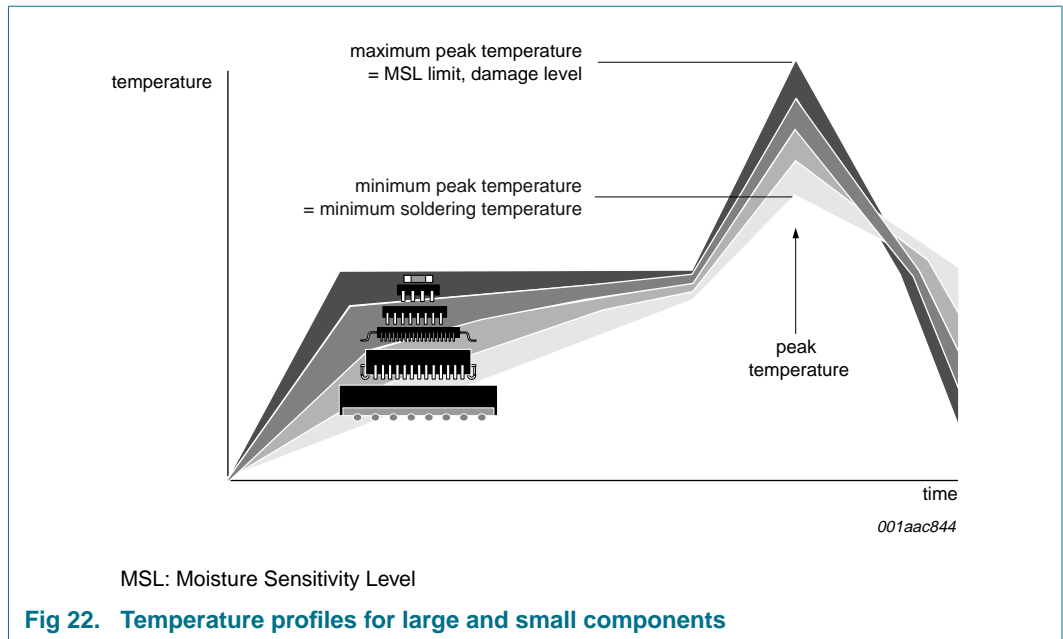
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 28. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 22](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 17. Soldering: additional information

The package of this device supports the reflow soldering process only.

## 18. Abbreviations

**Table 29. Abbreviations**

Acronym	Description
AC-3	Active Coding-3
ADC	Analog-to-Digital Converter
AV	Audio Video
CEC	Consumer Electronics Control
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
DDC	Display Data Channel
DENC	Digital video ENCoder
DSP	Digital Signal Processor
DTS	Digital Theater Systems
DVD	Digital Versatile Disc
DVI	Digital Visual Interface
EAV	End of Active Video
E-EDID	Enhanced Extended Display Identification Data
HBM	Human Body Model
HDCP	High-bandwidth Digital Content Protection

Table 29. Abbreviations ...continued

Acronym	Description
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
HPD	Hot Plug Detect
IRQ	Interrupt ReQuest
KSV	Key Selection Vector
LO	Local Oscillator
L-PCM	Linear Pulse-Code Modulation
LSB	Least Significant Bit
LV-TTL	Low-Voltage Transistor-Transistor Logic
MSB	Most Significant Bit
OTP	One-Time Programmable
PAL	Phase Alternating Line
PCM	Pulse-Code Modulation
PLL	Phase-Locked Loop
PVR	Personal Video Recorder
RGB	Red, Green, Blue
SAV	Start of Active Video
SHA-1	Secure Hash Algorithm 1
STB	Set-Top Box
S/PDIF	Sony/Philips Digital Interface
TMDS	Transition Minimized Differential Signaling
Tx	Transmitter
XGA	Extended Graphics Array
YUV	color space used by the NTSC and PAL systems
YCbCr	color space originally defined by the ITU-R BT.601

## 19. Revision history

Table 30. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9981A_1	20080519	Product data sheet	-	-

## 20. Legal information

### 20.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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