UBA20261/2

600 V and 350 V power IC for step dimmable CFLs

Rev. 2 — 10 October 2011 Product data sheet

1. General description

The UBA20261/2 are high-voltage power integrated circuits designed to drive and control high powered self-ballasted Compact Fluorescent Lamp (CFL) lighting applications operating at mains supply voltages of 120 V or 230 V. The IC includes a half-bridge power circuit consisting of two NMOST power MOSFETs, an advanced feature for step dimming and a lamp current controlled boost feature for boosting cold (amalgam) CFLs.

The controller contains a CFL half-bridge drive function, a high-voltage level-shift circuit with integrated bootstrap diode, an oscillator function, a current control function for preheat and burn, a timer function and protection circuits. The UBA20261/2 are supplied using the dV/dt current charge supply circuit from the half-bridge circuit.

Remark: The mains voltages given in this data sheet are AC voltages.

2. Features and benefits

2.1 Half-bridge features

- UBA20261: two internal 350 V, 1 Ω, maximum 5 A NMOST half-bridge power MOSFETs
- UBA20262: two internal 600 V, 3 Ω, maximum 2.7 A NMOST half-bridge power MOSFETs
- Integrated high-voltage level-shifter function with integrated bootstrap diode

2.2 Preheat and ignition features

- Coil saturation protection during ignition
- Adjustable saturation protection level
- Adjustable preheat time
- Adjustable preheat current
- Ignition lamp current detection

2.3 Lamp boost features

- Adjustable boost timing
- Fixed boost current ratio of 1.5
- Gradually boost to burn transition timing

2.4 Dim features

- 4-level step dimming adjustment using a standard on/off mains switch
- Adjustable memory retention time for step dimming
- Adjustable minimum dimming level

2.5 Protection

- OverTemperature Protection (OTP)
- Capacitive Mode Protection (CMP)
- OverPower Protection (OPP)
- OverCurrent Protection (OCP) in both boost and burn states
- Power-down function

2.6 Other features

- Current controlled operation in both boost and burn state
- External power-down option

3. Applications

- UBA20261: Step-dimmable compact fluorescent lamps at power levels between 5 W and 20 W operating at 120 V mains voltage
- UBA20262: Step-dimmable compact fluorescent lamps at power levels between 5 W and 20 W operating at 230 V mains voltage

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
UBA20261T/N1	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
UBA20262T/N1	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

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5. Block diagram

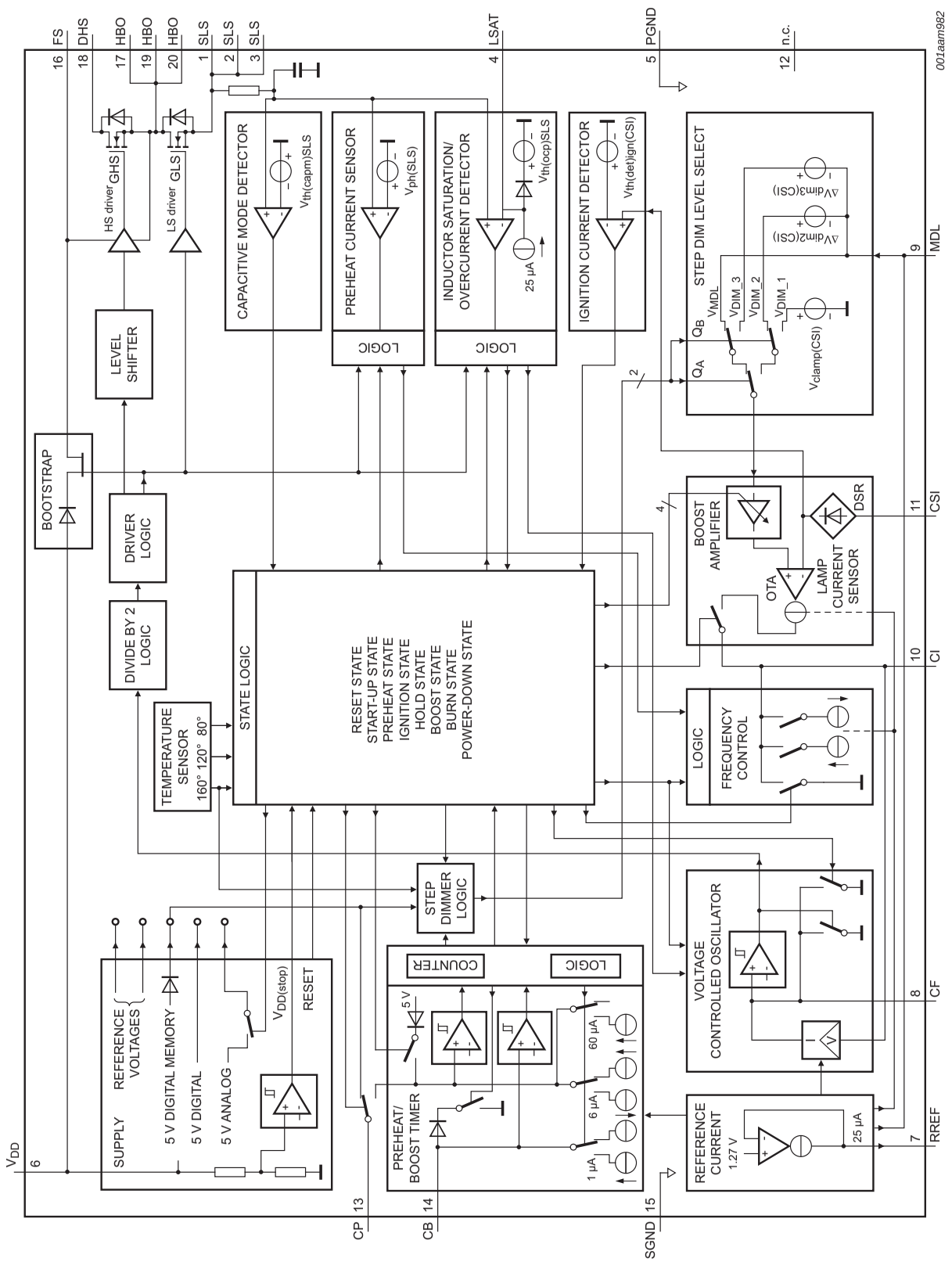

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

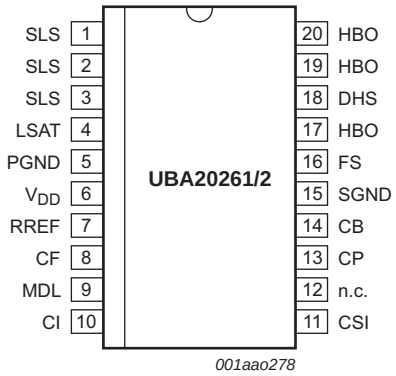

Fig 2. Pin configuration for UBA20261/2 (SOT109-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
SLS	1, 2, 3	source low-side switch[1]
LSAT	4	coil saturation level input
PGND	5	power ground[2]
V_{DD}	6	low voltage supply
RREF	7	internal reference current input
CF	8	voltage controlled oscillator capacitor
MDL	9	minimum dimming level input
CI	10	voltage controlled oscillator input integrating capacitor
CSI	11	current feedback sense input
n.c.	12	not connected
CP	13	preheat timing capacitor
CB	14	boost timing capacitor
SGND	15	signal ground[2]
FS	16	floating supply voltage
HBO	17, 19, 20	half-bridge output; open output[3]
DHS	18	high-voltage supply; drain high-side switch

[1] The SLS pins are internally connected.

[2] The PGND and SGND pins are internally connected.

[3] The HBO pins are internally connected.

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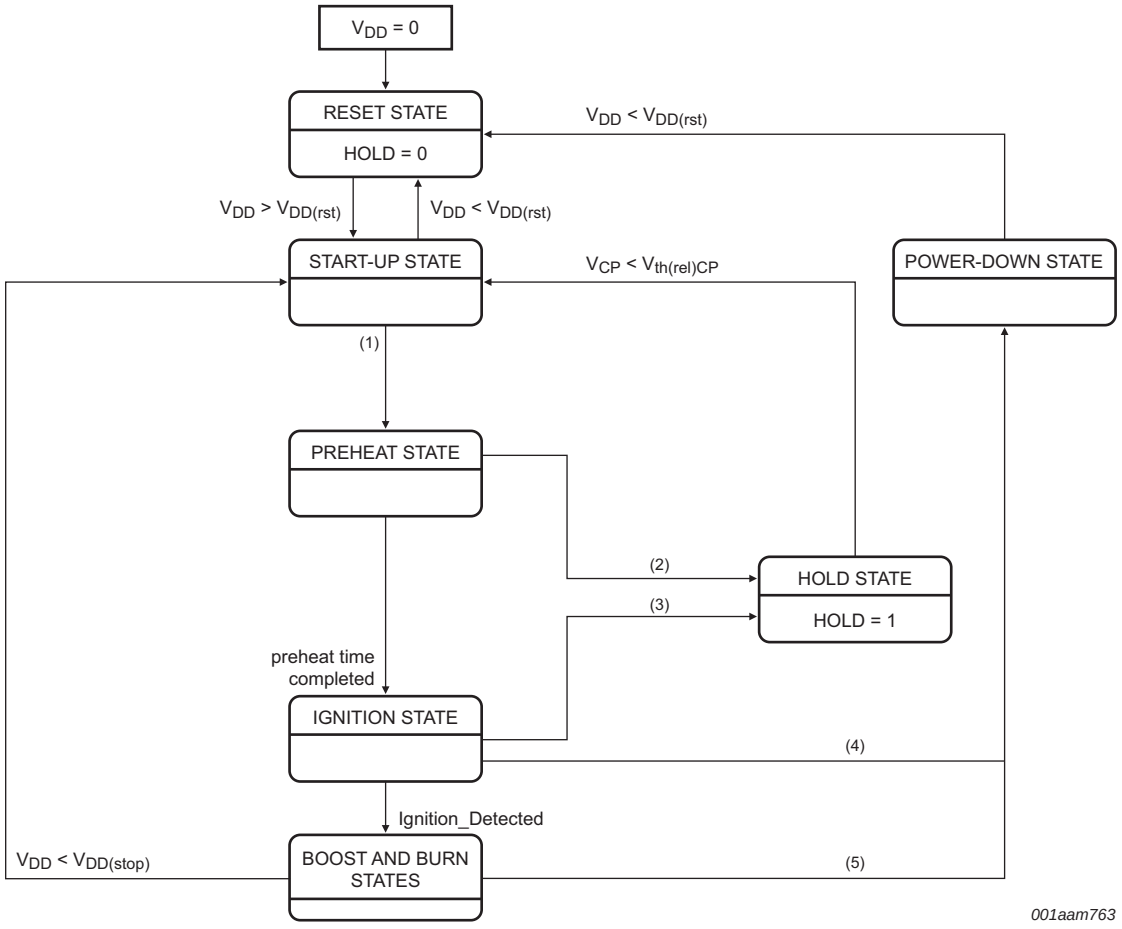
7. Functional description

The UBA20261/2 are ICs with integrated half-bridge MOSFETs in self-ballasted high-power CFLs. The UBA20261/2 have no dimming control input but instead, four preset fixed dimming levels. Only minor adjustment of the presets is possible.

The UBA20261/2 are rated up to a maximum continuous rectified mains voltage of 350 V or 500 V, respectively and lamp power-up to 20 W. The UBA20261/2 includes all functions necessary for preheat, ignition and boost operation of the lamp. In addition, the IC includes the four-step dimming feature and several protective features to safeguard CFL operation. The controller states are shown in Figure 3.



(1) $V_{DD} < V_{DD(start)}$ and (HOLD = 0 OR $V_{CP} < V_{th(rel)CP}$).

(2) $V_{DD} < V_{DD(stop)}$.

(3) (End of ignition time AND HOLD = 0) OR $V_{DD} < V_{DD(stop)}$.

(4) End of ignition time AND HOLD = 1.

(5) $V_{CP} < V_{th(pd)CP}$, OR overcurrent fault time > $^{1}/_{10}\, t_{ph}$ OR $f_{bridge(max)}$ detected in capacitive mode.

Fig 3. State diagram

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7.1 Lamp start-up cycle

7.1.1 Reset state

The UBA20261/2 are in the reset state when the supply voltage on the V_{DD} pin is below the $V_{DD(rst)}$ level. In the reset state, part of the internal supply is turned off and all registers, counters and timers are undefined. The hold state latch is reset and both the high and low side power transistors are non-conductive.

During power-up, the low voltage supply capacitor on the V_{DD} pin is charged through the external start-up resistor. The start-up state is entered when the voltage on the V_{DD} pin is above the $V_{DD(rst)}$ level. The UBA20261/2 enters the reset state when the supply voltage on the V_{DD} pin drops below $V_{DD(rst)}$.

7.1.2 Start-up state

The start-up state is entered by charging the low voltage supply capacitor on the V_{DD} pin through the external start-up resistor. At start-up, the High-Side (HS) transistor is non-conductive and the Low-Side (LS) transistor is conductive to enable charging of the bootstrap capacitor. This capacitor supplies the HS driver and Level shifter circuit connected between the FS and HBO pin. A DC reset circuit is integrated into the HS driver. This circuit ensures that below the FS pin lockout voltage, the output voltage $V_{GHS} - V_{HBO}$ is zero.

When the start-up state is entered, the circuit only starts oscillating when the low voltage supply (V_{DD}) reaches the $V_{DD(start)}$ value. The circuit always starts oscillating at $f_{bridge(max)}$. The circuit enters the preheat state as soon as the capacitor connected to the CP pin is charged above the $V_{th(CP)max}$ voltage level. To keep oscillating, V_{DD} must be above $V_{DD(stop)}$ and below the $V_{DD(clamp)}$ upper limit.

During the start-up state, the voltage on the CF pin is zero and on the CB pin is close to zero. The voltage on the CP pin rises just above $V_{th(CP)max}$ during the start-up state as shown in Figure 9.

7.1.3 Preheat state

After starting at $f_{bridge(max)}$, the frequency decreases by charging capacitor C_{CI} using an output current circuit. The preheat current sensor circuit controls the current output circuit, until the momentary value of the voltage across sense resistor R_{SLS} reaches the fixed preheat voltage level (SLS pin). At this level, the current of the preheat current sensor reaches the charge and discharge balanced state on capacitor C_{CI} to set the half-bridge frequency.

The preheat time consists of eight saw-tooth pulses at the CP pin. The preheat time begins as soon as the capacitor on the CP pin is charged above $V_{th(CP)max}$ value. During the preheat time, the current feedback sensor circuit (input CSI pin) is disabled.

To increase noise immunity, an internal filter of 30 ns is included at the SLS pin.

If the level on the V_{DD} pin drops below $V_{DD(stop)}$ during preheat, the preheat state is immediately stopped and the circuit enters the hold state. The hold state delays a new preheat cycle by a fixed delay time. A fixed voltage drop on the preheat capacitor C_{CP} and the fixed discharge current on the CP pin are used to set the delay time.

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New preheat cycles start after the CP pin level slowly discharges until $V_{CP} < V_{th(rel)CP}$ and recharges above $V_{th(CP)max}$ provided $V_{DD} > V_{DD(start)}$ (see Figure 5).

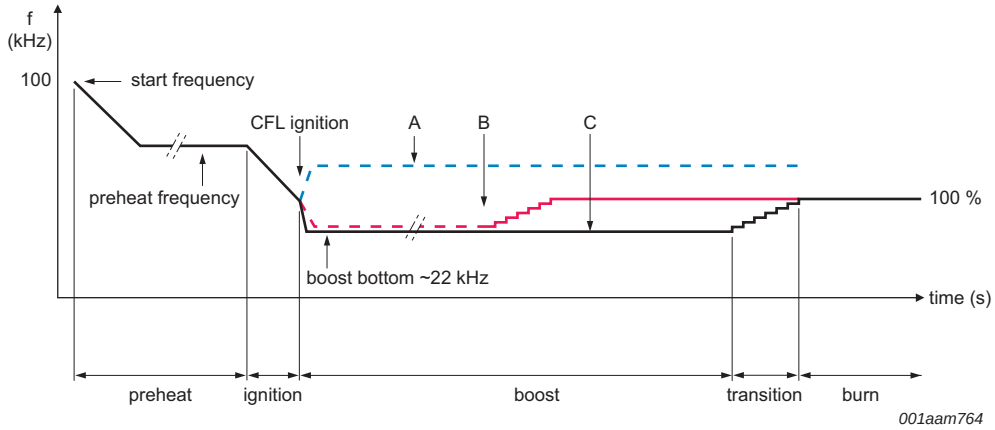

Fig 4. CFL frequency from start to burn state

7.1.4 Ignition state

After the preheat state has been completed, the ignition state is entered. In the ignition state, the frequency sweeps down on the CI pin due to capacitor C_{CI} charging at a fixed current as shown in Figure 4. During this continuous decrease in frequency, the circuit approaches the resonant frequency of the resonant tank (L2, C5). This action causes a high voltage across the lamp to ignite the lamp. The ignition current sensor circuit which monitors the voltage over resistor R_{CSI} (see Figure 12) detects lamp ignition.

If the voltage on pin CSI is above the typical ignition detection threshold voltage level of 0.6 V, lamp ignition is detected. The system changes from ignition state to either the boost or burn state.

If ignition not is detected, the frequency drops further to the minimum half-bridge frequency $f_{bridge(min)}$ frequency. To avoid repeated ignition attempts and overheating of the application due to lamp damage, the IC only tries to ignite the lamp twice after power-up. The ignition attempt counter increments at the end of the ignition enabling time when the lamp ignition threshold voltage on the CSI pin is not exceeded. The ignition enabling time is typically $\frac{1}{4}$ of the preheat time t_{ph}. If a second ignition attempt also exceeds the ignition time-out period, the IC enters the power-down state (see Figure 5).

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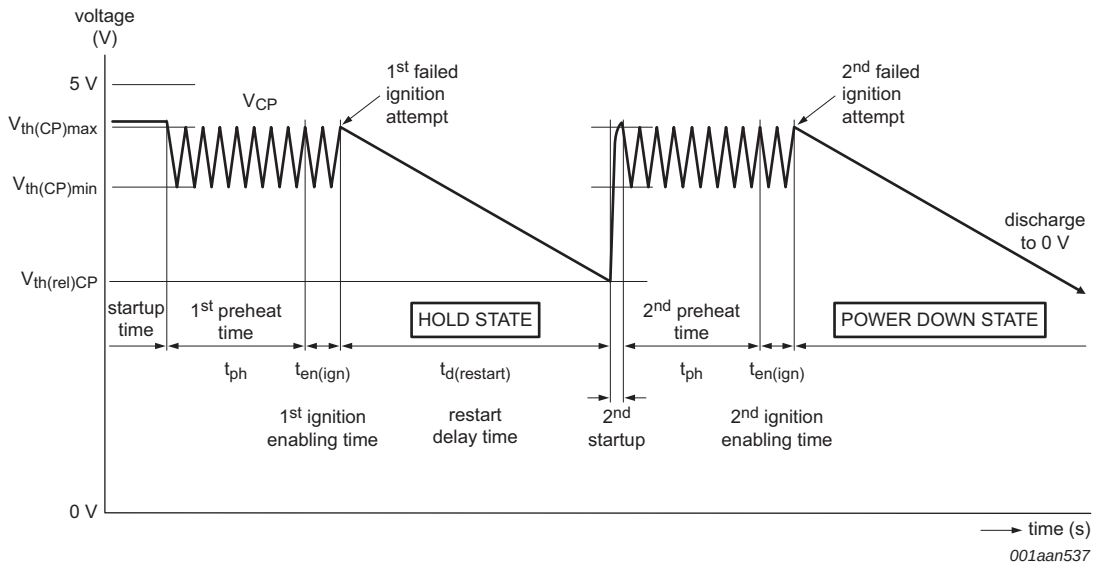

Fig 5. Retry cycle

7.1.5 Boost state and transition to burn state

When ignition is detected, by measuring lamp current on the CSI pin, the circuit enters the boost state. Figure 7 shows the boost and burn state in more detail. In the boost state, the nominal burn state lamp current can be increased with a fixed boost ratio of 1.5 : 1. This ratio boosts the slow luminescence increase of a cold amalgam CFL lamp, provided the IC is in the DIM_1 mode. If the IC is at a temperature ($T_{j(bp)bst}$) before entering the boost state, the burn state is bypassed.

A boost timing circuit is included to determine the boost time and transition to burn time. The circuit consists of a clock generator comprising C_{CB}, $R_{ext(RREF)}$ and a 64-step counter. When the timer is not operating, C_{CB} is discharged below the $V_{th(CB)min}$ level of 1.1 V. This voltage, approximately 0.6 V, is still higher than the level at which the comparator on C_{CB} detects if the CB pin is shorted to ground.

The boost time consists of 63 saw-tooth pulses on the CB pin, automatically followed by the transition time at the CP pin. The 32 saw-tooth pulses form the transition time from boost to burn and enables a smooth transition between the current controlled boost and burn state. The total transition time is approximately four times the preheat time (see Figure 6).

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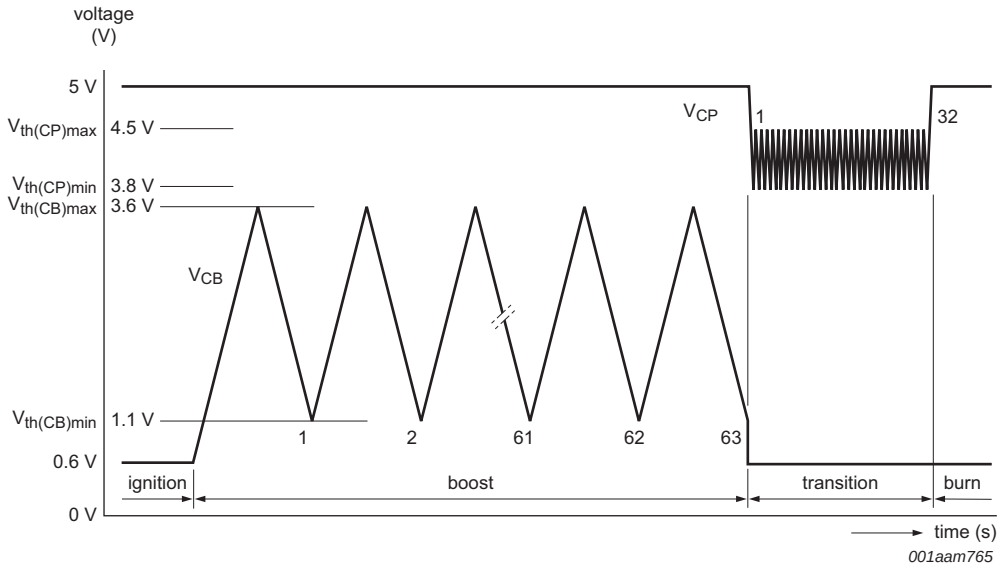

Fig 6. Boost timing

In the boost state, a lamp current feedback control is implemented to improve lamp stability (see Section 7.1.6). The lamp current has a fixed ratio of 1.5 compared to the burn state to boost the slow luminescence increase of a cold CFL lamp. In the boost to burn transition time, there is a slow 15-step ratio decrease from 1.5 down to 1. The preheat timer is reused for the transition to burn time and the boost ratio is gradually decreased in 15 steps from 1.5 to 1, within 32 saw-tooth pulses on the CP pin. Using the application values for C_{CB} and $R_{ext(RREF)}$, a boost time of more than 300 s is possible. In addition to boost bypass at a temperature of $T_{j(bp)bst}$ (≈ 80 °C), a temperature protection function is implemented during boost state of $T_{j(end)bst}$ (≈ 120 °C). If the temperature passes this level during boost, the transition timer is immediately started to enter the burn state faster. Effectively this reduces the boost time (see Figure 4 [B]).

The boost state current boost does not start in dim modes DIM_2, DIM_3 or MDL (see Figure 4 [A]).

Remark: If the CB pin is short circuited to ground, the boost function is disabled. In such a situation, the bottom frequency $f_{bridge(min)}$ is 1.8 times higher than the boost bottom frequency $f_{bridge(bst)min}$.

7.1.6 Burn state

After the boost state or when it is bypassed, the burn state starts. The lamp current sensor circuit remains enabled (see Figure 4[A]). The voltage across sense resistor R_{CSI}, is measured by the CSI (Current Sense Input) pin. It is then passed through a Double-Sided Rectifier (DSR) circuit and fed towards an Operational Transconductor Amplifier (OTA).

When the RMS voltage on the CSI pin reaches the actual internal reference level, the lamp current sensor circuit takes over control of the lamp current. The internal current output of the OTA is transferred using an integrator on the CI pin to the input for Voltage Controlled Oscillator (VCO). The VCO regulates the frequency and as a result, the lamp current.

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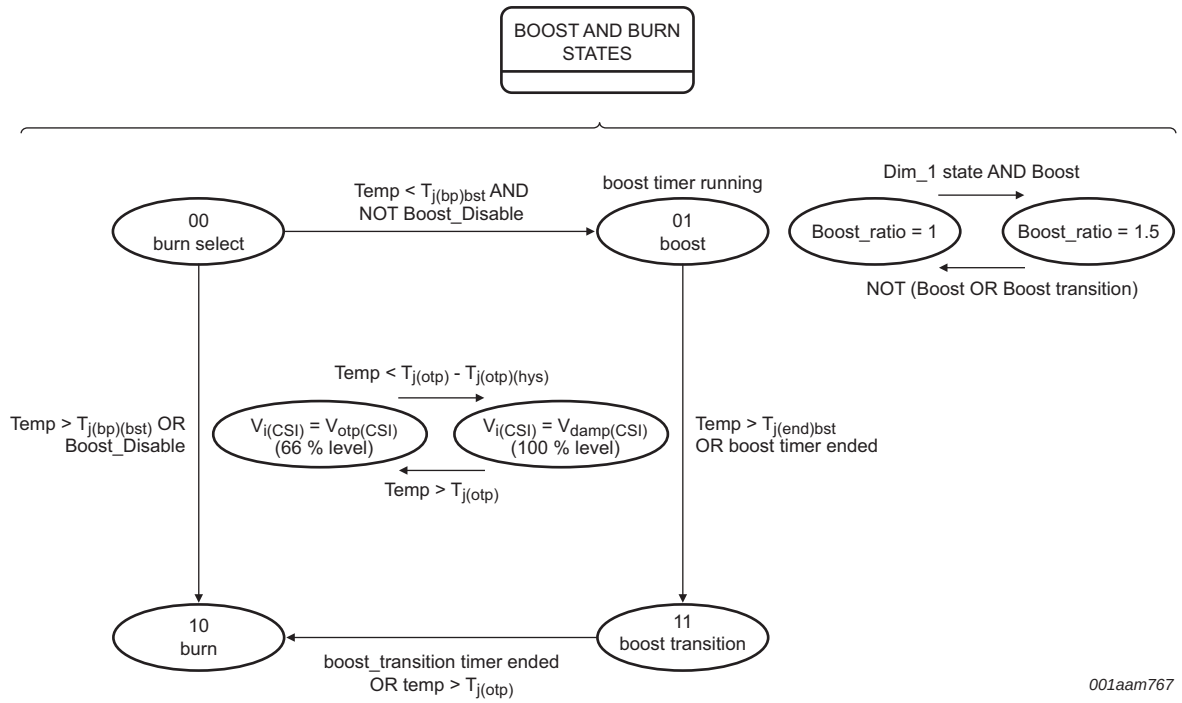

Fig 7. Boost and burn state machine

7.1.7 Hold state

The hold state is a special state that reduces lamp flicker at deep dim levels, on or near dim and ignition threshold levels. The IC enters the hold state after an ignition failure or when the low supply voltage V_{DD} drops below $V_{DD(stop)}$ in the ignition or preheat states (see Figure 3).

A repeated drop in supply voltage below $V_{DD(stop)}$ in preheat or ignition states, does not increment the ignition attempt counter. The hold state is entered, delaying a new preheat cycle with the same time delay/mechanism by the hold state retention time as shown in Figure 5.

When CP is below $V_{th(rel)CP}$, the IC is released from the hold state and moves to the start-up state as shown in Figure 3. Alternatively, the hold state ends when the supply voltage drops below $V_{DD(rst)}$ and the IC is reset.

With a 470 nF capacitor on the CP pin, the typical hold state retention delay is between 1 s and 1.7 s. This delay is dependent on where the preheat cycle was cut-off on the rising or falling edge of the preheat timing. The retention time for a failed ignition always starts from the top of the rising edge on the CP pin (see Figure 5).

In the hold state, a hold state latch is set (hold state latch = 1) and the oscillator is stopped. In addition, the HS transistor is non-conductive and the LS transistor is conducting.

The voltage on the V_{DD} pin alternates between $V_{DD(start)}$ and $V_{DD(stop)}$ until the voltage on the CP pin reaches $V_{th(rel)CP}$ (see Figure 5). The alternating supply voltage is caused by the current drawn by the IC supply pin V_{DD}. The supply current is less than 220 μA, when

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the supply voltage V_{DD} rises between $V_{DD(stop)}$ and $V_{DD(start)}$. Typically, the supply current is 2 mA when V_{DD} falls between $V_{DD(start)}$ and $V_{DD(stop)}$. More current is drawn during the fall in V_{DD} because the internal analog supply is turned on when $V_{DD} > V_{DD(start)}$. This function enables the comparators to monitor the voltage on the CP pin and if the supply voltage V_{DD} falls below $V_{DD(stop)}$.

7.2 Oscillation and timing

7.2.1 Oscillator control

The internal oscillator is a VCO which generates a saw-tooth waveform between the $V_{th(CF)max}$ level and 0 V. Capacitor C_{CF}, resistor $R_{ext(RREF)}$ and the voltage on the CI pin determine the saw-tooth frequency. $R_{ext(RREF)}$ and C_{CF} determine the minimum and maximum switching frequencies. Their ratio is internally fixed. Two ratios are available, the ratio between $f_{bridge(max)}$ and $f_{bridge(min)}$ is 2.5 and the ratio between $f_{bridge(max)}$ and $f_{bridge(bst)min}$ is 4.6. The saw-tooth frequency is twice the half-bridge frequency.

Transistors HS (Q1) and LS (Q2) are switched to conducting at a duty cycle of approximately 50 %. An overview of the oscillator signal and driver signals is shown in Figure 8. The oscillator starts oscillating at $f_{bridge(max)}$. The non-overlap time between the gate driver signals V_{GLS} and V_{GHS} is t_{no}.

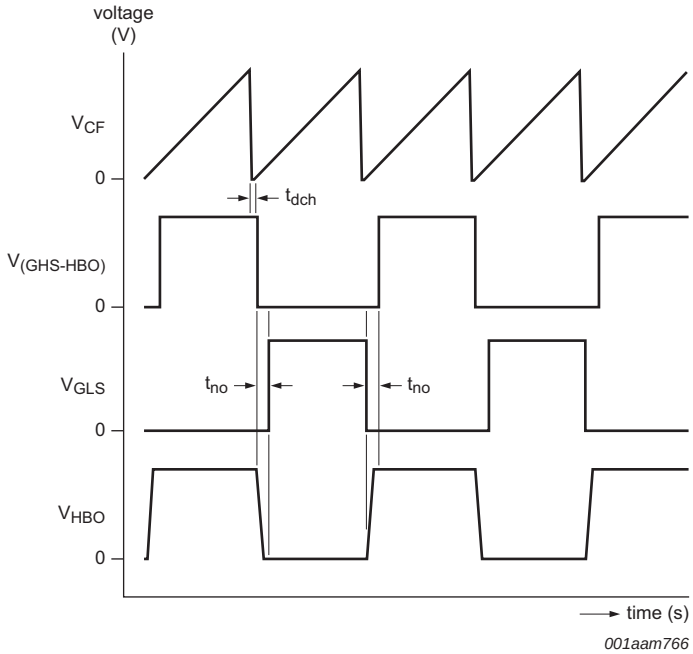

Fig 8. Saw-tooth, gate driver and half-bridge output signals

7.2.2 Combined timing circuit

A combined timing circuit is used to determine the preheat time, ignition enabling time and overcurrent time (see Figure 9). C_{CP}, $R_{ext(RREF)}$ and the counter comprise the clock generator circuit. When the timer is not running, C_{CP} is charged to 5 V. The timing circuit

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starts operating after the start-up state when the V_{DD} supply voltage has reached $V_{DD(start)}$ and the voltage on the CP pin passes $V_{th(CP)max}$. The preheat time consists of eight saw-tooth pulses on the CP pin as shown in Figure 9.

The maximum ignition enabling time after the preheat phase is two complete saw-tooth pulses. During the boost and burn state, part of the timer is used to generate the maximum overcurrent time (more than one half of the saw-tooth pulse). If a continuous overcurrent is detected, the timer starts.

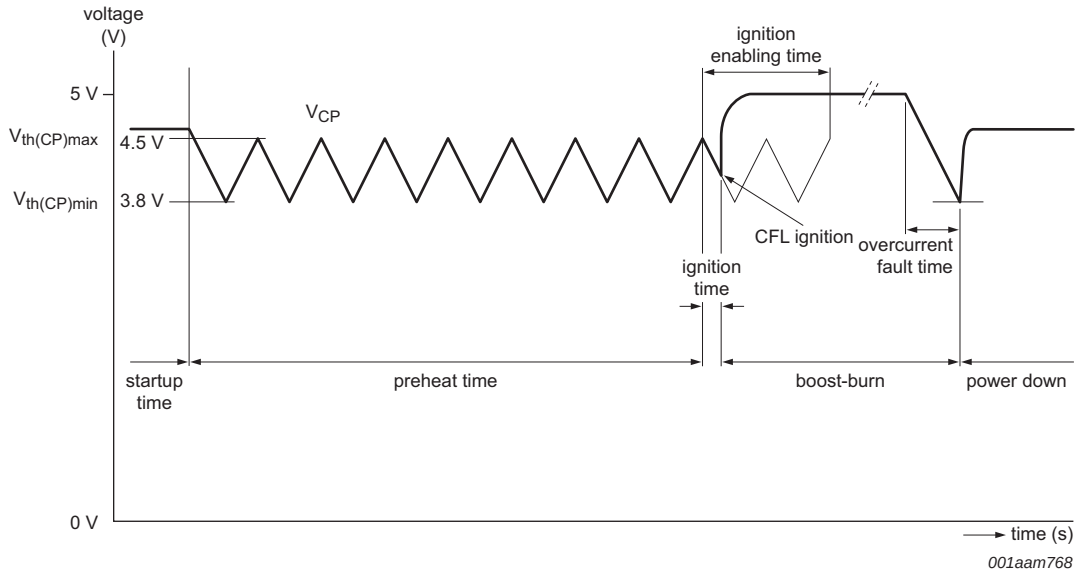

Fig 9. Timing diagram for preheat, ignition and overcurrent

7.3 Step dimming

The UBA20261/2 uses the step dimming method of dimming a lamp load. This method enables the lamp to operate in four different light output level modes including full power. The four different dim level modes can be selected by toggling the supply voltage which is made possible by toggling the mains voltage switch.

To change the dim step, the low supply voltage must be above $V_{DD(start)}$. In addition, the voltage must drop below $V_{DD(rst)}$, irrespective of whether the IC is in the preheat, ignition, boost or burn states (see Figure 10).

The discharge time of capacitor C_{CP} (while the V_{DD} power supply is off) sets step memory retention time. When the voltage on the CP pin drops below $V_{ret(dim)CP}$ (2 V typical), the step memory is lost. The next time the supply is powered on, the lamp turns on at full brightness. Using the default components, the retention time is ± 3 s. The retention time calculation can be found in Section 11 on page 23.

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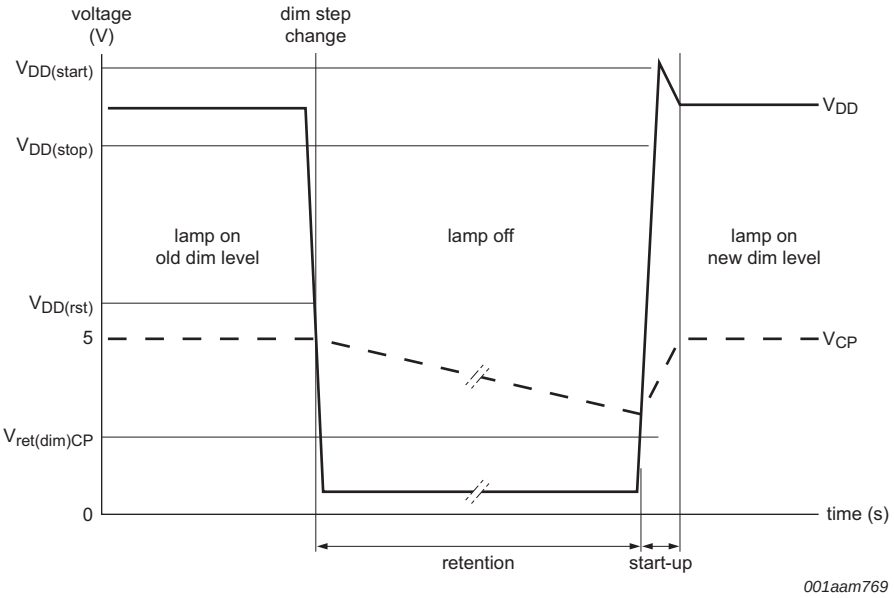

Fig 10. Supply voltage cycle for dim step change

Four internal references determine the actual internal set point levels used for the different step dim levels. Depending on the selected dim level, the current control feedback loop regulates the voltage on the CSI pin. In this way, it ensures that $V_{i(CSI)}$ is equal to one of the selected internal set point voltages. The sequence of the four dim steps shown in Figure 11 is as follows:

- The lamp is switched off longer than the memory retention time: the IC starts up in the DIM_1 mode (lamp is 100 % on, no dimming)
- After lamp off/on toggling, the IC twice enters DIM_2 mode: the lamp is dimmed to approximately 66 % (1) of its initial light output
- The next lamp off/on toggling, the IC enters DIM_3 mode: the lamp is dimmed approximately 33 % (1) of its initial light output
- Toggling the lamp off/on again: the IC enters the MDL (Minimum Dimming Level) mode. This level equals approximately 10 % (1) of the initial light output
- Renewed toggling enters the DIM_1 mode again.

Where (1) = R_{MDL} = 2 kΩ

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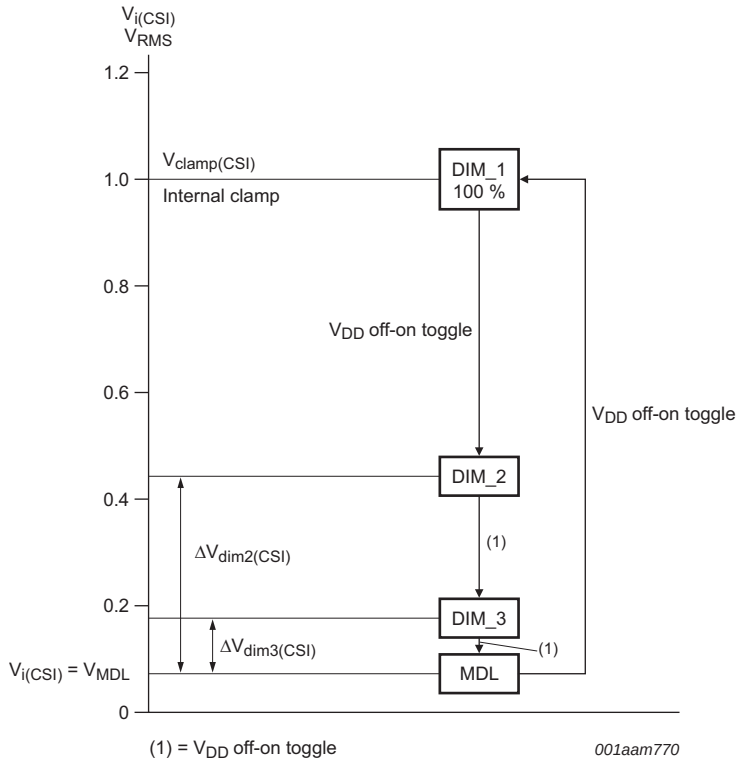

Fig 11. Voltage on the CSI pin as function of dim step

As the internal step reference voltages are independent from the mains voltage, the lamp current output is kept constant. Making the lamp current output not susceptible to line voltage fluctuations. The MDL level sets the minimum lamp current level and is adjusted using the MDL pin. An accurate minimum dimming voltage level is set using an internal reference current and an external resistor R_{MDL}. The internal reference current is derived from the internal band gap reference circuit and resistor $R_{ext(RREF)}$. The other two step dimming levels are set at a fixed voltage offset referenced to the adjusted MDL level. This means that these levels shift by the same voltage as the MDL shifts. When the MDL level is at the default level, the light output in DIM_2, DIM_3 and MDL modes is approximately 66 %, 33 % and 5 % from nominal.

7.4 Protection functions and Power-down mode

7.4.1 Coil saturation protection

CSP is integrated into the IC to allow the use of small CFL lamps and use of small coils. Saturation of these coils is detected and excessive overcurrent due to saturation is prevented. CSP is only enabled during the ignition state. A cycle-by-cycle control mechanism is used to limit voltages and currents in the resonant circuit when there is no or delayed ignition. It prevents coil saturation, limits high peak currents and the dissipation in the half-bridge power transistors.

Coil saturation is detected by monitoring the voltage across the R_{SLS} resistor. A trigger is generated when this voltage exceeds the $V_{th(sat)SLS}$ level. When saturation is detected, a fixed current $\Delta I_{o(sat)CF}$ is injected into the C_{CF} capacitor to shorten the half-bridge

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switching cycle. The injected current is maintained until the end of the switching cycle. This action immediately increases the half-bridge switching frequency. Additionally, for each successive cycle that coil saturation is detected, capacitor C_{CI} discharges enabling ignition time-out detection in the ignition state.

CSP is triggered when the voltage on the SLS pin exceeds $V_{th(sat)SLS}$ (typically 2.5 V). The voltage $V_{i(SLS)}$ on the SLS pin is determined by the external resistor R_{SLS} value and also sets the preheat current.

Using an internal reference source current and external resistor R_{LSAT}, an accurate setting for the coil saturation threshold level $V_{th(sat)SLS}$ is possible. When resistor R_{LSAT} is not mounted, the $V_{th(sat)SLS}$ level is internally clamped at 2.5 V. It is mandatory for stability reasons to connect C_{LSAT} in parallel to R_{LSAT} even when R_{LSAT} is not mounted.

7.4.2 Overcurrent protection

OCP is active in both the burn and boost states but not during boost transition. Overcurrent is detected, when the peak voltage of the absolute value across the current sense resistor connected to the SLS pin exceeds the OCP reference level $V_{th(ocp)SLS}$. A current $I_{o(CP)}$ is then sunk from the capacitor connected to the CP pin for the next full cycle.

If overcurrent is not present at the end of this cycle, the current is disabled. A current, equal to $I_{o(CP)}$ is sourced to the CP pin instead. If overcurrent occurs in more than half the number of cycles, a net discharging of the capacitor connected to the CP pin occurs. When the voltage on the CP pin drops below $V_{th(CP)min}$, the IC enters Power-down mode. During a continuous overcurrent condition, the overcurrent fault time of $t_{fault(oc)}$ takes $\pm \frac{1}{9} t_{ph}$ after which the IC enters Power-down mode. The $V_{th(ocp)SLS}$ level is the same as the $V_{th(sat)SLS}$ level during the ignition state.

7.4.3 Overpower protection

OPP is active in the boost and burn state. The lamp current is limited and regulated in all dim step states to the internal dim step reference voltage levels. These reference voltage levels are derived from an internal reference voltage. Consequently, supply voltage fluctuations in the mains supply voltage during overvoltage situations do not affect these reference voltage levels.

When the lamp is in the first dim mode (no dimming), the current is limited and regulated to the nominal lamp current. In addition, in the boost state, the first dim mode boosted by a factor of 1.5.

7.4.4 Capacitive mode protection

CMP is active in the ignition, burn and boost states and during boost transition. The signal across resistor R_{SLS} also provides information about the half-bridge switching behavior. When conditions are normal, the current flows from the LS transistor source to the half-bridge when the LS transistor is switched on. This results in a negative voltage on the SLS pin.

As the circuit yields to capacitive mode, the voltage becomes smaller and eventually reverses polarity. CMP prevents this action by checking if the voltage on the SLS pin is above the $V_{th(capm)SLS}$ level.

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If the voltage across resistor R_{SLS} is above the $V_{th(capm)SLS}$ threshold when the LS transistor is switched on, the circuit assumes that it is in capacitive mode. When capacitive mode is detected, the currents from the OTA, which normally regulate the lamp current, are disabled. Then the capacitive mode sink current $I_{o(CI)}$ is enabled.

The capacitive mode sink current starts to discharge the capacitor/resistor circuitry on the CI pin and as a result, gradually increases the half-bridge frequency. Discharging continues for the remainder of the current switching cycle ensuring the total current on the CI pin is equal to the sink current. If capacitive mode persists, the action is repeated until capacitive mode is no longer detected. If capacitive mode is no longer detected, the OTA takes over the regulation again.

If the conditions causing capacitive mode persist, OTA regulates the system back towards capacitive mode and the protection takes over again. The system operates on the edge of capacitive mode.

When in the boost and burn states, the half-bridge load is capacitive at higher frequencies, CMP eventually drives the half-bridge to the maximum frequency $f_{bridge(max)}$. This causes the IC to enter Power-down mode.

7.4.5 Overtemperature protection

The OTP circuit is designed to prevent the device from overheating in hazardous environments. The circuit is triggered when the temperature exceeds the maximum temperature value $T_{j(otp)}$. OTP changes the lamp current to the level equal to the $V_{otp(CSI)}$ level. This condition remains until the temperature decreases by $\pm$ 20 °C = $T_{j(otp)hys}$. After this decrease in temperature, the lamp current level returns to the nominal level.

7.4.6 Power-down mode

Power-down mode is entered when:

- The overcurrent time exceeds the maximum overcurrent fault time $t_{fault(oc)}$ or if the overcurrent occurs in more than half the number of cycles when $V_{th(CP)min}$ is reached
- If during boost or burn state, $f_{bridge(max)}$ is reached due to capacitive mode detection
- two consecutive failed lamp ignition attempts

In Power-down mode, the oscillator is stopped, the HS transistor is non-conductive and the LS transistor is conductive. The V_{DD} supply is internally clamped. The circuit is released from Power-down mode by lowering the low voltage supply below $V_{DD(rst)}$ (mains switch reset).

An option is available which enables the IC to enter Power-down mode using external logic. The external power-down option is only available when the IC is in the boost or burn state. The CP pin is used to enable the external power-down option. When the CP pin is connected using a 10 kΩ resistor to the PGND pin or the SGND pin, V_{CP} is pulled below $V_{th(pd)CP}$. The IC then enters Power-down mode.

Remark: Do not connect the CP pin directly to pins PGND or SGND. Always connect in series to pins PGND or SGND with a 10 kΩ resistor. This action avoids the IC being not starting up because of excessive currents flowing during the reset and start-up states.

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8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
General					
$R_{ext(RREF)}$	external resistance on pin RREF	fixed nominal value 33 kΩ	30	36	kΩ
SR	slew rate	on pins HBO with respect to PGND	–4	+4	V/ns
T_j	junction temperature		–40	+150	°C
T_{amb}	ambient temperature	P = 0.8 W	–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
Currents					
$I_{i(CF)}$	input current on pin CF		0	200	μA
I_{DM}	peak drain current	UBA20261;			
		HS; $T_j < T_{j(max)}$; $I_{DM} = I_{DHS} = I_{HBO}$	-	5	A
		LS; $T_j < T_{j(max)}$; $I_{DM} = I_{HBO} = I_{o(SLS)}$	-	5	A
		UBA20262;			
		HS; $T_j < T_{j(max)}$; $I_{DM} = I_{DHS} = I_{HBO}$	-	2.7	A
		LS; $T_j < T_{j(max)}$; $I_{DM} = I_{HBO} = I_{o(SLS)}$	-	2.7	A
I_D	drain current	UBA20261:			
		HS; RMS current at P = 0.5 W; $T_j = T_{j(max)}$; $I_D = I_{DHS} = I_{HBO}$	-	0.54	A
		LS; RMS current at P = 0.5 W; $T_j = T_{j(max)}$; $I_D = I_{HBO} = I_{o(SLS)}$	-	0.54	A
		UBA20262:			
		HS; RMS current at P = 0.5 W; $T_j = T_{j(max)}$; $I_D = I_{DHS} = I_{HBO}$	-	0.31	A
		LS; RMS current at P = 0.5 W; $T_j = T_{j(max)}$; $I_D = I_{HBO} = I_{o(SLS)}$	-	0.31	A
Voltages					
V_{DHS}	voltage on pin DHS	UBA20261:			
		operating at T_{amb} = 25 °C	-	350	V
		operating at T_{amb} = –25 °C	-	340	V
		UBA20262:			
		operating	-	500	V
		during 1 s	-	600	V
V_{FS}	voltage on pin FS	with respect to HBO	–0.3	+14	V
V_{DD}	supply voltage		–0.3	+14	V
$V_{i(CSI)}$	input voltage on pin CSI		–5	+5	V
$V_{i(SLS)}$	input voltage on pin SLS		–6	+6	V
V_{CI}	voltage on pin CI		0	3.5	V
V_{LSAT}	voltage on pin LSAT		0	5	V
V_{MDL}	voltage on pin MDL	LPF used as input pin	0	5	V

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Table 3. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
ESD					
V_{ESD}	electrostatic discharge voltage	human body model:	−2000	+2000	V
		all pins, except pins 16, 17, 18, 19 and 20			
		pins 16, 17, 18, 19 and 20	−1000	+1000	V
		charged device model:	−400	+400	V
		all pins			

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; SO20 package on JEDEC 2S 2P board	56	K/W

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10. Characteristics

Table 5. Characteristics

V_{DD} = 13 V; $V_{FS} - V_{HBO}$ = 13 V; T_{amb} = 25 °C; settings according to default setting (see Table 6 on page 26), all voltages referenced to PGND and SGND, positive currents flow into the UBA20261/2, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Start-up state							
Pin V_{DD}							
$V_{DD(rst)}$	reset supply voltage	HS switch = off; LS switch = on		5.7	6.2	6.7	V
$V_{DD(stop)}$	stop supply voltage			9.6	10	10.4	V
$V_{DD(start)}$	start supply voltage			11.9	12.4	12.9	V
$V_{DD(hys)}$	hysteresis of supply voltage	start-stop		2.2	2.4	2.6	V
$V_{DD(clamp)}$	clamp supply voltage	$I_{DD(clamp)}$ = 5 mA		13	13.4	13.8	V
$I_{DD(clamp)}$	clamp supply current	$V_{DD(clamp)}$ = 14 V		20	30	-	mA
$I_{DD(startup)}$	start-up supply current	V_{DD} = 9 V		-	190	220	µA
$I_{DD(pd)}$	power-down supply current	V_{DD} = 9 V		-	190	220	µA
I_{DD}	supply current	default setting; $V_{CI} = V_{CI(clamp)}$; V_{CB} = 0 V	[1]	-	1.6	2	mA
High-voltage supply							
Pins DHS, HBO and FS							
I_{leak}	leakage current	UBA20261: 300 V on high-voltage pins		-	-	30	µA
		UBA20262: 500 V on high-voltage pins		-	-	30	µA
Voltage controlled oscillator							
Output pin CI							
$V_{CI(max)}$	maximum voltage on pin CI			2.7	3	3.3	V
$V_{hr(CI)}$	headroom voltage on pin CI	$V_{clamp(CI)} = V_{hr(CI)} + V_{CI(max)}$; burn and boost state		-	80	-	mV
Output pin CF							
$f_{bridge(min)}$	minimum bridge frequency	C_{CF} = 100 pF; $V_{CI} = V_{clamp(CI)}$; V_{CB} = 0 V	[2]	38	40	42	kHz
$f_{bridge(max)}$	maximum bridge frequency	C_{CF} = 100 pF; V_{CI} = 0 V	[2]	88	100	112	kHz
$f_{bridge(bst)min}$	minimum boost bridge frequency	C_{CF} = 100 pF; $V_{CI} = V_{clamp(CI)}$	[2]	21	22	23	kHz
t_{no}	non-overlap time	V_{HBO} rising edge		1.3	1.5	1.7	µs
		V_{HBO} falling edge		1.3	1.5	1.7	µs
$V_{th(CF)max}$	maximum threshold voltage on pin CF	$C_{ext(CF)}$ = 100 pF; $V_{CI} = V_{clamp(CI)}$; V_{CB} = 0 V		2.4	2.5	2.6	V
$I_{o(bst)CF}$	boost output current on pin CF	V_{CF} = 1.5 V; $V_{CB} = V_{clamp(CI)}$		−12.3	−11.8	−11.3	µA
$I_{o(CF)min}$	minimum output current on pin CF	V_{CF} = 1.5 V; V_{CB} = 0 V; $V_{CI} = V_{clamp(CI)}$		−22.8	−21.8	−20.8	V
$I_{o(CF)max}$	maximum output current on pin CF	V_{CF} = 1.5 V; V_{CB} = 0 V		−67	−60	−53	µA

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Table 5. Characteristics *...continued*

V_{DD} = 13 V; $V_{FS} - V_{HBO}$ = 13 V; T_{amb} = 25 °C; settings according to default setting (see Table 6 on page 26), all voltages referenced to PGND and SGND, positive currents flow into the UBA20261/2, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power transistors							
R_{on}	on-state resistance	UBA20261:					
		HS; I_{DHS} = 1.1 A; T_j = 25 °C		-	1	1.3	Ω
		LS; I_{HBO} = 1.1 A; T_j = 25 °C		-	1	1.3	Ω
		UBA20262:					
		HS; I_{DHS} = 1.1 A; T_j = 25 °C		-	3	3.6	Ω
		LS; I_{HBO} = 1.1 A; T_j = 25 °C		-	3	3.6	Ω
$R_{on(150)}/R_{on(25)}$	on-state resistance ratio (150 °C to 25 °C)	R_{on} at T_j = 150 °C / R_{on} at T_j = 25 °C		-	1.7	-	
Boot strap diode							
V_F	forward voltage	bootstrap diode; I_{FS} = 5 mA; ($V_F = V_{DD} - V_{FS}$)		1.3	1.7	2.1	V
Preheat current sensor							
Input pin SLS							
$I_{I(SLS)}$	input current on pin SLS	$V_{i(SLS)}$ = 0.4 V		-	-	1	µA
$V_{ph(SLS)}$	preheat voltage on pin SLS		[3]	0.57	0.60	0.63	V
Output pin CI							
$I_{o(source)CI}$	source output current on pin CI	V_{CI} = 2 V; $V_{i(SLS)}$ < 0.6 V		–10.6	–9.6	–8.6	µA
$I_{o(sink)CI}$	sink output current on pin CI	V_{CI} = 2 V; $V_{i(SLS)}$ < 0.6 V		26	29	32	µA
Preheat timer, ignition timer and overcurrent fault timer							
t_{ph}	preheat time	C_{CP} = 470 nF; $R_{ext(RREF)}$ = 33 kΩ		-	0.93	-	s
$t_{en(ign)}$	ignition enable time	C_{CP} = 470 nF; $R_{ext(RREF)}$ = 33 kΩ		-	0.22	-	s
$t_{fault(oc)}$	overcurrent fault time	C_{CP} = 470 nF; $R_{ext(RREF)}$ = 33 kΩ; initial voltage V_{CP} = 5 V		-	0.1	-	s
$t_{ret(dim)}$	dimming retention time	C_{CP} = 470 nF; $R_{ext(RREF)}$ = 33 kΩ; initial voltage V_{CP} = 5 V		-	2.8	-	s
$I_{o(CP)}$	output current on pin CP	V_{CP} = 4.1 V; source (–); sink (+)		5.5	5.9	6.3	µA
$I_{ret(dim)CP}$	dimming retention current on pin CP	Current into pin CP; V_{DD} = 0 V; initial V_{CP} = 5 V		-	0.5	-	µA
$V_{th(CP)min}$	minimum threshold voltage on pin CP	V_{CF} = 0 V, V_{CI} = 2 V		-	3.8	-	V
$V_{th(CP)max}$	maximum threshold voltage on pin CP	V_{CF} = 0 V, V_{CI} = 2 V		-	4.5	-	V
$V_{hys(CP)}$	hysteresis voltage on pin CP			0.6	0.7	0.8	V
$I_{pu(CP)}$	pull-up current on pin CP	V_{CP} = 3.8 V		-	–60	-	µA
$V_{ret(dim)CP}$	dimming retention voltage on pin CP	V_{DD} = 0 V		-	2	-	V
$V_{th(pd)CP}$	power-down threshold voltage on pin CP	burn state; 10 kΩ connected in series		-	1	-	V
$V_{th(rel)CP}$	release threshold voltage on pin CP	hold state		-	2.7	-	V

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Table 5. Characteristics *...continued*

V_{DD} = 13 V; $V_{FS} - V_{HBO}$ = 13 V; T_{amb} = 25 °C; settings according to default setting (see Table 6 on page 26), all voltages referenced to PGND and SGND, positive currents flow into the UBA20261/2, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Boost timer						
Pin CB						
t_{bst}	boost time	C_{CB} = 470 nF; T_j < 80 °C	-	148	-	s
$I_{o(CB)}$	output current on pin CB	V_{CB} = 2.35 V; source (–); sink (+)	0.8	1	1.2	µA
$V_{th(CB)min}$	minimum threshold voltage on pin CB		-	1.1	-	V
$V_{th(CB)max}$	maximum threshold voltage on pin CB		-	3.6	-	V
$V_{hys(CB)}$	hysteresis voltage on pin CB		2.3	2.5	2.7	V
$T_{j(bp)bst}$	boost bypass junction temperature	T_j sensed at end of ignition time	65	80	95	°C
$T_{j(end)bst}$	boost end junction temperature	T_j during boost time	105	120	135	°C
$I_{det(dis)bst}$	boost disable detection current	V_{CB} = 0 V	–30	–25	–20	µA
$t_{t(bst-burn)}$	transition time from boost to burn	C_{CP} = 470 nF; T_j < 80 °C	-	3.6	-	s
Pin CSI						
N_{LCBR}	lamp current boost ratio	$V_{i(CSI)}$ in boost state versus $V_{i(CSI)}$ in burn state; default start-up state (no dimming)	1.4	1.5	1.6	V
Coil saturation protection and overcurrent detection						
Input: pin SLS						
$V_{th(sat)SLS}$	saturation threshold voltage on pin SLS	ignition state; R_{LSAT} = 47 kΩ	1.10	1.18	1.25	V
$V_{th(ocp)SLS}$	overcurrent protection threshold voltage on pin SLS	ignition state; R_{LSAT} = 47 kΩ	1.10	1.18	1.25	V
t_{leb}	leading edge blanking time	detection disabled for first part of GLS time	-	800	-	ns
Input: pin LSAT:						
$I_{source(LSAT)}$	source current on pin LSAT	V_{LSAT} = 1.2 V	–26.3	–25	–23.7	µA
$V_{clamp(LSAT)}$	clamp voltage on pin LSAT	R_{LSAT} = ∞; C_{LSAT} = 1 nF	2.3	2.5	2.7	V
Output pin CI						
$I_{o(sink)CI}$	sink output current on pin CI	V_{CI} = 2 V; $V_{i(SLS)}$ > $V_{th(sat)SLS}$; cycle clocked	26	29	32	µA
Output: pin CF:						
$\Delta I_{o(sat)CF}$	saturation output current difference on pin CF	V_{CF} = 1.5 V; ignition state; LS switch = on	-	160	-	µA
Ignition current detection						
Input pin CSI						
$V_{th(det)ign(CSI)}$	ignition detection threshold voltage on pin CSI	[3]	0.55	0.6	0.65	V
$t_{w(det)ign(min)}$	minimum ignition detection pulse width	$V_{th(det)ign(CSI)}$ = 0.75 V square pulse	685	885	1085	ns

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Table 5. Characteristics *...continued*

V_{DD} = 13 V; $V_{FS} - V_{HBO}$ = 13 V; T_{amb} = 25 °C; settings according to default setting (see Table 6 on page 26), all voltages referenced to PGND and SGND, positive currents flow into the UBA20261/2, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Capacitive mode detection							
Input pin SLS							
$V_{th(capm)SLS}$	capacitive mode threshold voltage on pin SLS		[4]	–15	–5	0	mV
Output pin CI							
$I_{o(sink)CI}$	sink output current on pin CI	$V_{i(SLS)} > V_{th(capm)SLS}$; V_{CI} = 2 V; ignition state or boost and burn state		26	29	32	µA
Lamp current sensor and dimming control							
Input pin CSI							
$R_{i(CSI)}$	input resistance on pin CSI	$V_{i(CSI)}$ = 1 V		1	-	-	MΩ
		$V_{i(CSI)}$ = –1 V		40	50	60	kΩ
$V_{i(CSI)}$	input voltage on pin CSI	rectification linear for operation		–2.5	-	+2.5	V
		minimum dim level; $R_{ext(RREF)}$ = 33 kΩ; R_{MDL} = 2 kΩ		44	50	56	mV
$V_{clamp(CSI)}$	clamping voltage on pin CSI	RMS voltage; clamp active; default start-up burn state; 100 % on		-	1	-	V
$\Delta V_{dim2(CSI)}$	dimming 2 voltage difference on pin CSI	RMS voltage; offset from $V_{i(CSI)}$ at DIM_2 compared to MDL		330	350	370	mV
$\Delta V_{dim3(CSI)}$	dimming 3 voltage difference on pin CSI	RMS voltage; offset from $V_{i(CSI)}$ at DIM_3 compared to MDL		90	100	110	mV
Output pin CI							
$I_{o(CI)}$	output current on pin CI	burn state; source and sink; V_{CI} = 2 V; source (–) and sink (+)		85	95	105	µA
Input pin MDL (minimum dimming level)							
$I_{source(MDL)}$	source current on pin MDL			–26.3	–25	–23.7	µA
V_{MDL}	voltage on pin MDL	$R_{ext(RREF)}$ = 33 kΩ; R_{MDL} = 2 kΩ		-	50	-	mV
Temperature protection							
$T_{j(otp)}$	overtemperature protection junction temperature			145	160	170	°C
$T_{j(otp)hys}$	hysteresis overtemperature protection junction temperature			10	20	30	°C
Input pin CSI							
$V_{otp(CSI)}$	overtemperature protection voltage on pin CSI	RMS voltage; $R_{ext(RREF)}$= 33 kΩ; R_{MDL} = 2 kΩ; $T_j > T_{j(opt)} - T_{j(hys)(otp)}$		380	400	420	mV

[1] See Table 6 on page 26 for the default setting.

[2] The half-bridge output switching frequency (HBO). The saw-tooth frequency on pin CF is twice as high.

[3] Data sampling of $V_{ph(SLS)}$ is performed at the end of the LS power MOSFET conduction period in preheat state.

[4] Data sampling of $V_{th(capm)SLS}$ is performed at the start of conduction of the LS power MOSFET, in all states with oscillator active.

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11. Application information

11.1 Design equations

All described equations are only valid for $R_{ext(RREF)}$ = 33 kΩ.

11.1.1 C_{CP} related timing equations

- **Preheat time**

$$t_{ph} = \frac{C_{CP}}{I_{o(CP)}} \times (16 \times V_{hys(CP)} + 5 - V_{th(CP)max}) \quad (1)$$

- **Ignition enabling time**

$$t_{en(ign)} = \frac{C_{CP}}{I_{o(CP)}} \times 4 \times V_{hys(CP)} \quad (2)$$

- **Overcurrent fault time**

$$t_{fault(oc)} = \frac{C_{CP}}{I_{o(CP)}} \times (5 - V_{th(CP)min}) \quad (3)$$

- **Transition to burn time**

$$t_{t(bst-burn)} = \frac{C_{CP}}{I_{o(CP)}} \times (64 \times V_{hys(CP)} + 5 - V_{th(CP)max}) \quad (4)$$

- **Retain time step dimming**

$$t_{ret(dim)} = \frac{C_{CP}}{I_{ret(dim)CP}} \times (5 - V_{ret(dim)CP}) \quad (5)$$

- **Restart delay time**

$$t_{d(restart)} = C_{CP} \times \frac{(V_{th(CP)max} - V_{th(rel)CP})}{I_{restart(CP)}} \quad (6)$$

Where $I_{restart(CP)}$ = 0.5 μA (typical).

11.1.2 C_{CB} related timing equation

- **Boost time**

$$t_{bst} = \frac{C_{CB}}{I_{o(CB)}} \times (126 \times V_{hys(CB)} + V_{th(CB)min} - 0.6) \quad (7)$$

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11.1.3 $C_{(CF)}$ related frequency equations

- **Maximum bridge frequency**

$$f_{bridge(max)} = \frac{0.5}{\frac{C_{CF} + C_{par}}{I_{o(CF)max}} \times V_{th(CF)max} + t_{dch}} \quad (8)$$

Where C_{par} = 4.7 pF and t_{dch} = 0.4 µs.

- **Minimum bridge frequency with disabled boost**

$$f_{bridge(min)} = \frac{0.5}{\frac{C_{CF} + C_{par}}{I_{o(CF)min}} \times V_{th(CF)max} + t_{dch}} \quad (9)$$

- **Minimum bridge frequency with enabled boost**

$$f_{bridge(bst)min} = \frac{0.5}{\frac{C_{CF} + C_{par}}{I_{o(bst)CF}} \times V_{th(CF)max} + t_{dch}} \quad (10)$$

11.1.4 R_{SLS} related preheat current

$$I_{ph(M)} = \frac{V_{ph(SLS)}}{R_{SLS}} \quad (11)$$

$$I_{ph(RMS)} \approx \frac{V_{ph(SLS)}}{R_{SLS} \times \sqrt{3}} \quad (12)$$

11.1.5 R_{MDL} related minimum dimming level

- **MDL threshold voltage**

$$V_{MDL} = R_{MDL} \times I_{source(MDL)} \quad (13)$$

11.1.6 R_{LSAT} related saturation and overcurrent threshold level

- **Saturation threshold voltage**

$$V_{th(sat)SLS} = V_{th(ocp)SLS} = R_{LSAT} \times I_{source(LSAT)} \quad (14)$$

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11.2 Application Diagram

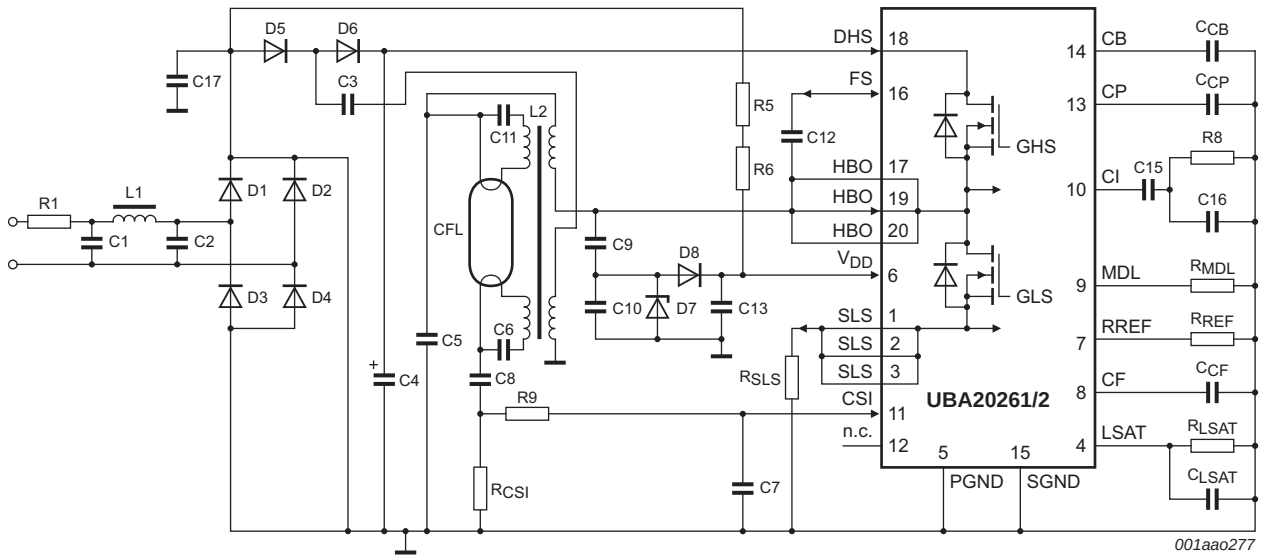

Fig 12. UBA20261/2 default application diagram

Detailed in Table 6 is a list of typical application components. See Figure 12.

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Table 6. Typical application components a 230 V (AC) mains application

Reference	Component		Description
	UBA20261	UBA20262	
R1	4.7 Ω	10 Ω	2 W fusible resistor
R5, R6	120 kΩ	220 kΩ	
R8	560 Ω	2.2 kΩ	
R9	1 kΩ	1 kΩ	
R_{REF}	33 kΩ; 1 %	33 kΩ; 1 %	
R_{SLS}	1 Ω	1.2 Ω	adjust for preheat current
R_{MDL}	1 kΩ	1 kΩ	adjust for minimum lamp current
R_{CSI}	6.19 Ω	6.19 Ω	adjust for nominal lamp current
R_{LSAT}	100 kΩ	100 kΩ	
C1	47 nF; 400 V	47 nF; 630 V	
C2	22 nF; 400 V	22 nF; 630 V	
C3	47 nF; 250 V	47 nF; 400 V	
C4	22 μF; 250 V	6.8 μF; 400 V	
C5	6.8 nF; 1 kV	4.7 nF; 1 kV	lamp capacitor
C6	68 nF; 250 V	68 nF; 250 V	
C7	100 pF	100 pF	
C8	22 nF; 400 V	47 nF; 400 V	
C9	560 pF; 500 V	560 pF; 500 V	V_{DD} charge pump capacitor
C10	not mounted	not mounted	
C11	68 nF; 250 V	68 nF; 250 V	
C12	100 nF	100 nF	
C13	470 nF	470 nF	
C15	220 nF	220 nF	
C16	not mounted	not mounted	
C17	220 nF; 400 V	220 nF; 400 V	
C_{CB}	150 nF	150 nF	
C_{CP}	330 nF	330 nF	
C_{CF}	100 pF; 2 %	100 pF; 2 %	
C_{LSAT}	1 nF	1 nF	
D1 to D4	1N4007	1N4007	
D5; D6	1N4937	1N4937	
D7	BZX84JC12	BZX84JC12	
D8	BAS20	BAS20	
L1	4.7 mH	4.7 mH	mains filter inductor; I_{SAT} = 300 mA
L2	Würth Elektronik: 760800031	Würth Elektronik: 7608000902	Respectively: 1000/1.3/1.3 / 22 μH and 2000/1.3/1.3/ 22 μH lamp inductor

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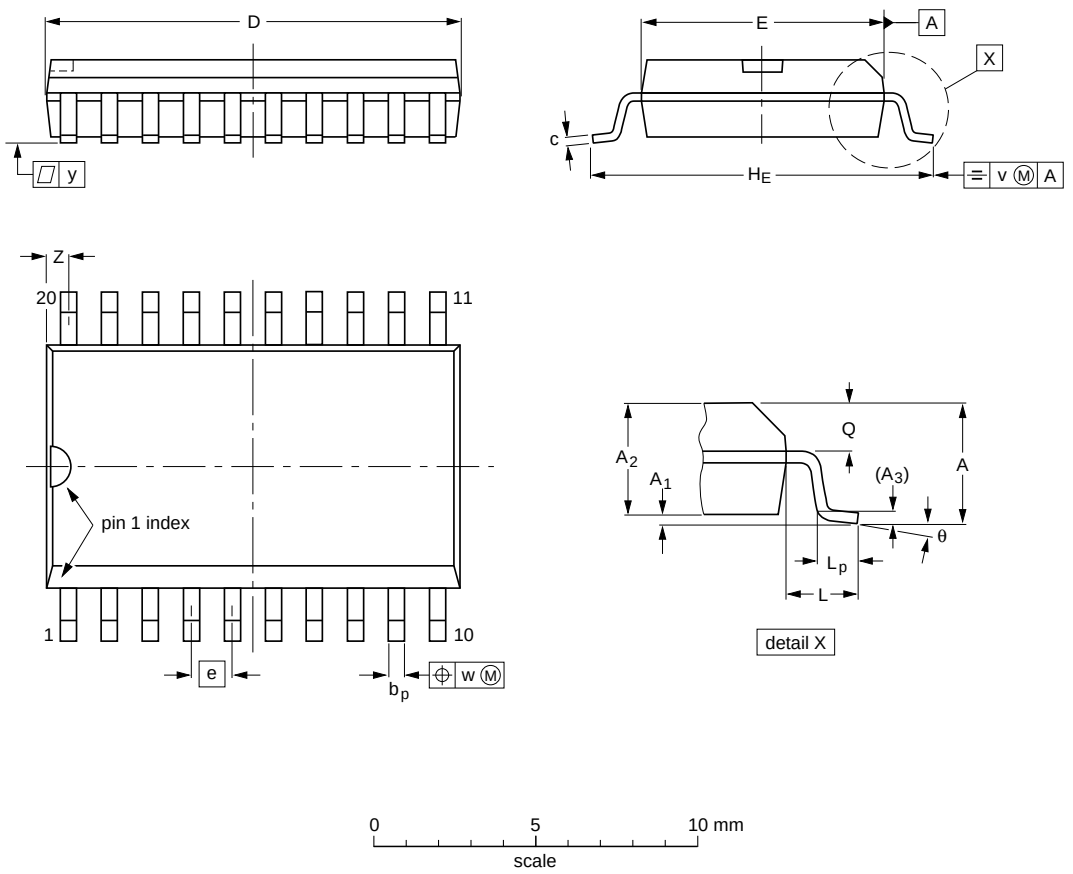
12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT163-1 (SO20)

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13. Abbreviations

Table 7. Abbreviations

Acronym	Description
CFL	Compact Fluorescent Lamp
CMP	Capacitive Mode Protection
DSR	Double-Sided Rectifier
ESD	ElectroStatic Discharge
HS	High-Side
LS	Low-Side
MDL	Minimum Dimming Level
OCP	OverCurrent Protection
OPP	OverPower Protection
OTA	Operational Transconductance Amplifier
OTP	OverTemperature Protection
RMS	Root Mean Square
SR	Slew Rate
UVLO	UnderVoltage LockOut
VCO	Voltage Controlled Oscillator

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14. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA20261_UBA20262 v. 2	20111010	Product data sheet	-	UBA20261_UBA20262 v. 1
UBA20261_UBA20262 v. 1	20110909	Preliminary data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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