UBA3077HN

Three-channel switched-mode LED driver

Rev. 1 — 8 February 2011 Objective data sheet

1. General description

The UBA3077HN is a high efficiency LED driver in an HVQFN40 package for general LED lighting or backlighting LCD displays.

Operating from a supply of 10 V to 42 V, it can drive up to 3 strings of 20 LEDs each. The low voltage circuitry is powered by an external 5 V voltage supply.

The chip can operate autonomously or be controlled via a 400 kHz I^2C-bus.

The peak current in each string is fixed by an external resistor. Three independent Pulse-Width Modulated (PWM) signals are available for dimming purposes. These PWM signals are delivered either directly by the graphic processor (direct control mode) to the pins PWM1, PWM2 and PWM3, or generated on-board based on data sent via the I^2C-bus interface.

Each LED string is supplied by its own boost converter delivering an output voltage from V_{IN} up to 75 V. The switching frequency is 500 kHz.

A power saving mode is entered when all PWM signals stay LOW for a period longer than 1 s.

Several protection mechanisms are available: overvoltage, short-circuit and open LED, overcurrent, UnderVoltage LockOut (UVLO) and overtemperature with an advanced adaptive protection. An error self-recovery (hiccup) mechanism is available with programmable delay time via an external capacitor.

2. Features and benefits

- Three-channel LED backlight driver
- ±2 % absolute LED current accuracy and channel-to-channel matching
- External power supply voltage from 10 V to 42 V and 5 V for low voltage circuitry
- Constant 500 kHz frequency peak current mode control
- Low value output capacitor (2 μF)
- Accurate internal oscillator
- Up to 150 mA per channel
- Peak LED current programmable with external resistor
- Three boost converters from V_{IN} up to 75 V output voltage
- High efficiency up to 90 %
- 14-bit PWM dimming (either defined by system-generated PWMs, or internally generated) from 2.0 kHz to 24 kHz (duty cycle from 0.1 % to 100 %)
- All power FETs integrated

- Possible control by I²C-bus with 2-bit address plus a common address for simultaneous configuration of several devices
- OverVoltage Protection (OVP)
- Adaptive thermal protection
- Power-On-Reset (POR)
- Open LED detection
- LX slope limited at 4 V/ns
- Hiccup delay programmable via an external capacitor
- Dedicated reference voltage input for host interface signals
- 2.5 A coil current limitation
- UVLO
- Short-circuit protection
- OverCurrent Protection (OCP) if external resistor value is wrong
- Programmable LED current rise time limitation (250 ns or 500 ns)
- Automatic low-power mode switching if PWM LOW period is too long

3. Applications

- General LED lighting
- Display LED backlight for TV/computing applications: Content Active Backlight Control (CABC)

4. Quick reference data

Table 1. Quick reference data

$V_{DD(24V)}$ = 24 V; $V_{DD(5V)}$ = 5 V; $V_{DD(IO)}$ = 5 V; T_{amb} = 0 °C to 80 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(24V)}$	supply voltage (24 V)	pin V_{IN}	10	24	42	V
$V_{DD(5V)}$	supply voltage (5 V)	pin V_{DD} with I_{DD} < 35 mA	4.5	5	5.5	V
$V_{DD(IO)}$	input/output supply voltage	pin $V_{DD(IO)}$ with $I_{DD(IO)}$ < 1 mA	1.62	-	5.5	V
$I_{DD(24V)}$	supply current (24 V)		-	100	-	μA
$I_{DD(5V)}$	supply current (5 V)	Sleep mode; internal CCO on	-	2	2.8	mA
		Active mode; internal CCO on; 150 mA I_{LED}; 100 % PWM duty cycle; all 3 channels active	-	21	-	mA
$I_{DD(IO)}$	input/output supply current	24 kHz PWM	-	-	100	μA
$V_{ref(IREF)}$	reference voltage on pin IREF	pin IREF	0.98	1.00	1.02	V
V_O	output voltage	pins V_{OUT1}, V_{OUT2} and V_{OUT3}	$V_{DD(24V)}$	-	75	V
V_{FB}	voltage on pin FB	PWM on; static with 100 % PWM duty cycle	-	0.9	1.2	V
I_{LED}	LED current	pin FB; R_{IREF} = 2667 Ω; R_{IREF} accuracy = 0.1 %; PWMn = HIGH	147	150	153	mA
$t_{w(PWM)H}$	HIGH level PWM pulse width	internal PWM generator; external PWM signal	417	-	-	ns
R_{DSon}	drain-source on-state resistance		-	0.5	1	Ω

Table 1. Quick reference data

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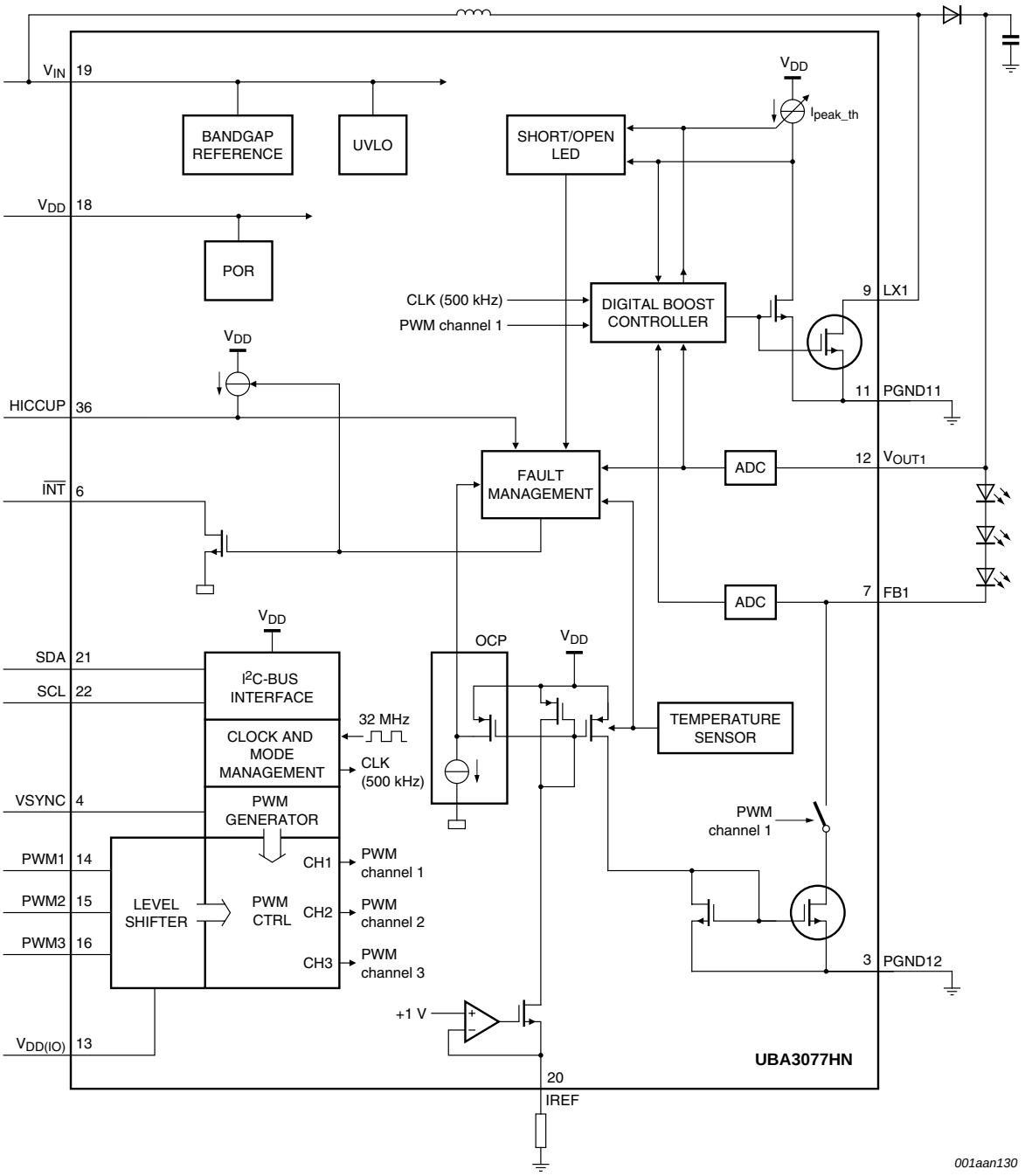
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{sw}	switching frequency	DC-to-DC	400	500	600	kHz
δ_{max}	maximum duty cycle	DC-to-DC	-	-	80	%
$V_{th(ovp)}$	overvoltage protection threshold voltage	pins V_{OUT1}, V_{OUT2}, V_{OUT3}	75	77	85	V
T_{amb}	ambient temperature	operating	0	-	80	°C
$T_{th(otp)}$	overtemperature protection threshold temperature	die junction temperature	-	150	-	°C

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
UBA3077HN	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

6. Block diagram



Only channel 1 is shown.

Fig 1. UBA3077HN block diagram

7. Pinning information

7.1 Pinning

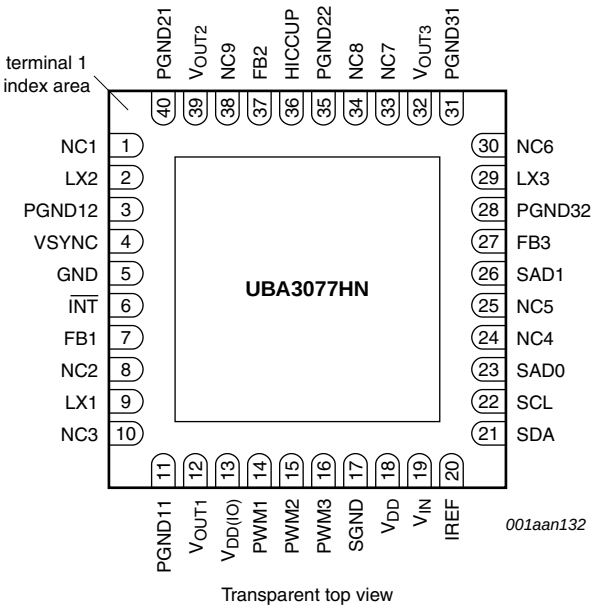


Fig 2. Pin configuration (HVQFN40)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Reset state	Description
NC1	1	-	-	not connected (leave unconnected)
LX2	2	power	-	channel 2 boost converter switch output
PGND12	3	supply	-	channel 1 LED current source ground
VSYNC	4	input	-	PWM duty cycle value update signal in I^2C-bus mode
GND	5	input	-	connect to the global ground
$\overline{INT}$	6	output	H	interrupt signal to the host (open-drain)
FB1	7	power	-	channel 1 LED current source output
NC2	8	-	-	not connected (leave unconnected)
LX1	9	power	-	channel 1 boost converter switch output
NC3	10	-	-	not connected (leave unconnected)
PGND11	11	supply	-	channel 1 boost converter switch ground
V_{OUT1}	12	power	-	channel 1 boost converter output voltage
$V_{DD(IO)}$	13	supply	-	reference and supply voltage for the host interface signals (from 1.8 V to 5 V)
PWM1	14	input	-	channel 1 PWM input signal

Table 3. Pin description *...continued*

Symbol	Pin	Type	Reset state	Description
PWM2	15	input	-	channel 2 PWM input signal
PWM3	16	input	-	channel 3 PWM input signal
SGND	17	supply	-	ground of low power circuitry
V_{DD}	18	supply	-	5 V supply voltage
V_{IN}	19	supply	-	power supply voltage
IREF	20	output	-	connection for an external precision resistor defining the current in the LED channels
SDA	21	input/output	H	I^2C-bus serial data input/output (open-drain)
SCL	22	input	H	I^2C-bus serial clock input
SAD0	23	input	-	I^2C-bus slave address selection 0
NC4	24	-	-	not connected (leave unconnected)
NC5	25	-	-	not connected (leave unconnected)
SAD1	26	input	-	I^2C-bus slave address selection 1
FB3	27	power	-	channel 3 LED current source output
PGND32	28	supply	-	channel 3 LED current source ground
LX3	29	power	-	channel 3 boost converter switch output
NC6	30	-	-	not connected (leave unconnected)
PGND31	31	supply	-	channel 3 boost converter switch ground
V_{OUT3}	32	power	-	channel 3 boost converter output voltage
NC7	33	-	-	not connected (leave unconnected)
NC8	34	-	-	not connected (leave unconnected)
PGND22	35	supply	-	channel 2 LED current source ground
HICCUP	36	output	-	connection for an external capacitor determining the delay for automatic fault recovery
FB2	37	power	-	channel 2 LED current source output
NC9	38	-	-	not connected (leave unconnected)
V_{OUT2}	39	power	-	channel 2 boost converter output voltage
PGND21	40	supply	-	channel 2 boost converter switch ground

8. Functional description

8.1 Supply

The UBA3077HN high voltage circuitry requires a nominal supply voltage of 24 V on pin V_{IN}. The allowed voltage range is 10 V to 42 V.

The UBA3077HN low voltage circuitry requires a supply voltage of 5 V on pin V_{DD}.

Pins V_{DD} and V_{IN} have a built-in POR function. The POR threshold (falling edge) and hysteresis is respectively 3.8 V and 200 mV on pins V_{DD} and V_{IN}.

If POR occurs on pin V_{IN}, the band gap and all internal references are shutdown. This inhibits Active mode, however the register content is preserved while V_{DD} is above the V_{DD} POR threshold.

The digital circuitry is reset and all register content cleared to default values only if a V_{DD} POR occurs.

The system interface signals (PWM1, PWM2 and PWM3) are referenced to $V_{DD(IO)}$ delivered by the system. $V_{DD(IO)}$ is typically in the range 1.8 V to 5 V.

8.2 I²C-bus protocol

The UBA3077HN features a slave mode I²C-bus interface.

The I²C-bus interface is a 2-wire serial interface developed by NXP Semiconductors to communicate between different ICs or modules. The I²C-bus interface comprises an SDA line and an SCL line. Both lines must be connected to V_{DD} via a pull-up resistor when connected to the output stages of a device. Data transfer may only be initiated when the bus is not busy. The UBA3077HN I²C-bus characteristic is in accordance with the 400 kbit/s Fast-mode I²C-bus specification.

Remark: Details of the I²C-bus standard are available in document *UM10204, "I²C-bus specification and user manual", version 0.3, June 2007*, which can be downloaded from the NXP Semiconductors web site www.nxp.com.

8.2.1 I²C-bus protocols for UBA3077HN read and write sequences

The read sequence may use a repeated start condition during the sequence to avoid the bus being released during the communication. The sequences can be used to read or write either a single data byte or a sequence of data bytes.

Sequences for write and read for both single bytes and burst mode are shown respectively in Figure 3 and Figure 4.

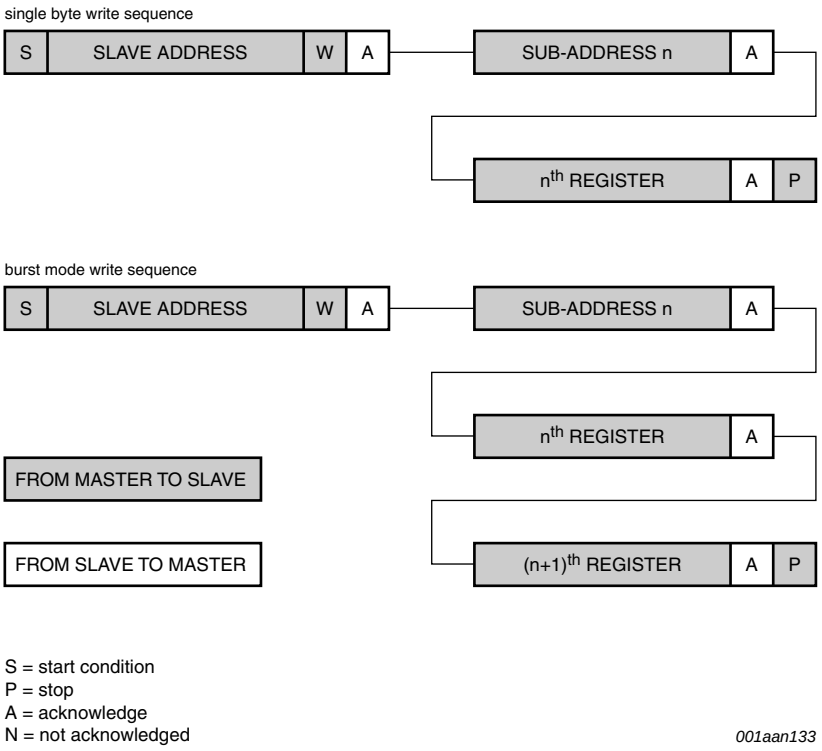


Fig 3. I^2C-bus write sequence

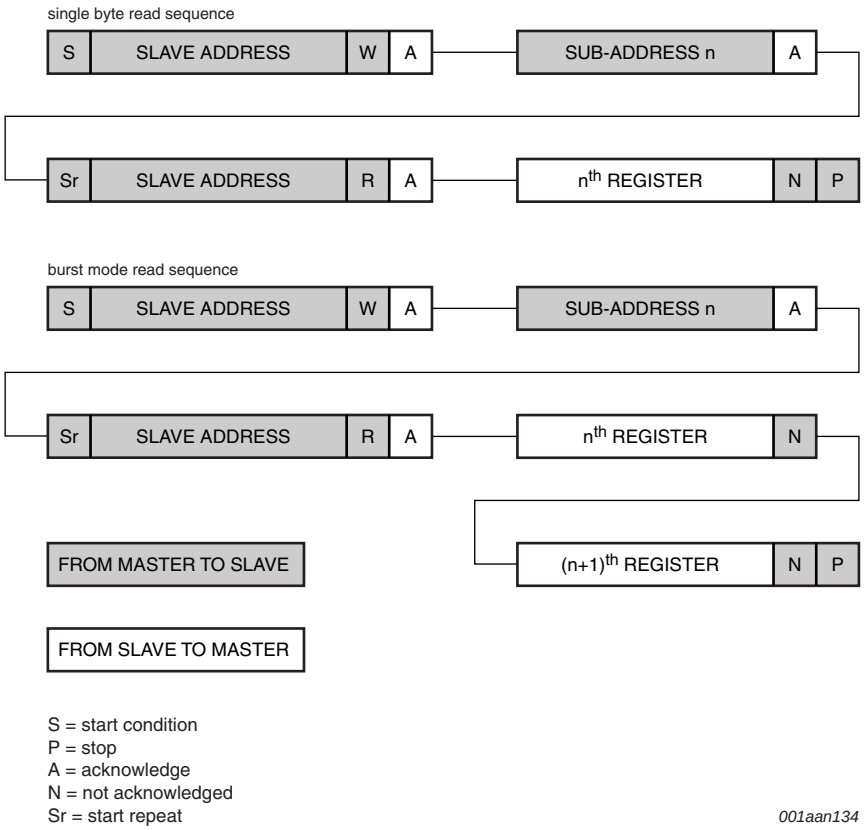


Fig 4. I²C-bus read sequence

8.2.2 Addressing

Each UBA3077HN in an I²C-bus system is activated when it receives a valid address. The address must always be sent as the first byte after the start condition in the I²C-bus protocol.

Up to four UBA3077HNs can be controlled by the same I²C-bus using pins SAD0 and SAD1 which define the two LSBs of the address.

Table 4. I²C-bus address

Address							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
0	1	1	0	0	SAD1	SAD0	1/0

One 7-bit address byte is required. The last bit of the address byte is the read/write bit and must always be set according to the required operation. The 7-bit I²C-bus address can be either: 0110000b (30h), 0110001b (31h), 0110010b (32h), or 0110011b (33h). The 7-bit address plus the R/W bit create an 8-bit write address of either 60h, 62h, 64h or 66h and a read address of either 61h, 63h, 65h or 67h.

The second byte sent to the UBA3077HN is the subaddress of a specific register.

All UBA3077HNs connected to the I²C-bus in the application acknowledge address 68h. This feature allows the PWM duty cycle of all channels to be changed simultaneously.

8.2.3 Data

The data byte(s) are sent after the subaddress is sent. The data byte(s) are defined in Figure 3 and Figure 4. An acknowledge is given after each data byte, and the subaddress automatically increments to the next, allowing burst mode in both read and write operation.

A description of the data that can be programmed in the registers is given in the register map in Section 8.2.4.

8.2.4 Register map

The UBA3077HN has 7 user-accessible registers.

Table 5. Register descriptions

Address	Register	Bit	Symbol	Access	Value at reset	Description
00h	PWM MSB	7 to 0	PWM[13:6]	R/W	0000 0000	8 MSB of the 14-bit PWM duty cycle
01h	PWM LSB	7 to 6	RESERVED	-	-	-
		5 to 0	PWM[5:0]	R/W	00 0000	6 LSB of the 14-bit PWM duty cycle
02h	Control	7	ADAPT_THERMP	R/W	1	deactivates adaptive thermal protection if set to 0
		6	RESERVED	-	-	-
		5	PWM_SHIFT	R/W	0	0: no phase shift PWM
						1: 120° phase shift PWM
		4	RESERVED	-	-	-
		3	ILED_SLOPE	R/W	0	0: 250 ns (10 % to 90 %)
						1: 500 ns (10 % to 90 %)
		2	STR3_EN	R/W	1	string 3 enabled
		1	STR2_EN	R/W	1	string 2 enabled
		0	STR1_EN	R/W	1	string 1 enabled
03h	Status	7	OCP	R/W	0	overcurrent status (write 1 to clear)
		6	SHORTP3	R/W	0	channel 3 LED short status (write 1 to clear)
		5	SHORTP2	R/W	0	channel 2 LED short status (write 1 to clear)
		4	SHORTP1	R/W	0	channel 1 LED short status (write 1 to clear)
		3	OVP3	R/W	0	channel 3 overvoltage status (write 1 to clear)
		2	OVP2	R/W	0	channel 2 overvoltage status (write 1 to clear)
		1	OVP1	R/W	0	channel 1 overvoltage status (write 1 to clear)
		0	THERMP	R/W	0	OTP status (write 1 to clear)
04h	Thermal	7 to 3	Chip ID	R	-	ID value: 01000
		2 to 0	TSENSOR[2:0]	R	000	$120 + (TSENSOR[2:0]) \times 4 \leq T_j < 120 + (TSENSOR[2:0] + 1) \times 4$
05h	Fractional clock division	7 to 0	PLLLSB[7:0]	R/W	10000000	PWM PLL LSB division code

Table 5. Register descriptions

Address	Register	Bit	Symbol	Access	Value at reset	Description
06h	Clock division	7	VSYNCPOL	R/W	0	0: VSYNC signal active HIGH
						1: VSYNC signal active LOW
		6	PWMSEL	R/W	0	0: external PWM selected (direct control mode)
						1: I^2C-bus PWM selected
		5	VSYNC_EN	R/W	0	0: immediate PWM duty cycle value change
						1: PWM duty cycle value change on VSYNC signal state as defined by VSYNCPOL
		4	RESERVED	-	-	-
		3 to 0	PLLMSB[3:0]	R/W	0010	PWM PLL MSB division code

8.3 State diagram

The UBA3077HN has the following modes:

- Reset
- Sleep
- Active
- Adaptive thermal
- Hiccup

8.4 Reset mode

The chip enters the reset state at power start-up phase or as soon as V_{DD} falls below the V_{DD} POR threshold voltage (V_{POR}). All registers are cleared to their default value.

If V_{DD} is below the rising edge threshold voltage, the UBA3077HN remains in Reset mode.

8.5 Sleep mode

If all PWM input signals or internally generated PWM signals based on register settings stay LOW for more than 1 s, the circuit enters Sleep mode. In this mode, the boost converters are off and the chip activity is reduced to decrease the current consumption to less than 2.8 mA.

When one of the PWM signals re-activates, the UBA3077HN enters Active mode provided that a protection has not been triggered.

8.6 Active mode

This is the normal operating mode where all supply conditions are correct and no abnormal event detected.

In Active mode, the I^2C-bus interface and all registers are fully accessible. DC-to-DC boost converter and LED current sources are operational and react to PWM signals as requested.

All protection circuits are on and continuously monitor for abnormal events.

8.7 Adaptive thermal mode

In Active mode, whenever the die temperature exceeds 120 °C, the chip can automatically enter Adaptive thermal mode. This mode can be disabled via the I^2C-bus interface.

At each 4 °C step increase in junction temperature above 120 °C, the peak LED current is reduced by 3 % independently of the duty cycle. This avoids having to deactivate the backlight suddenly if required, for example if the die overheats. The die temperature can be read via the I^2C-bus.

When the temperature falls below 120 °C, the chip reverts to Active mode.

8.8 Hiccup mode

When a fault is detected, the appropriate protection is triggered; see Section 8.12. The fault is indicated by pin $\overline{INT}$ pulled LOW and the protection status register set accordingly. In response, a constant current source starts charging the external Hiccup capacitor. The protection is maintained until the voltage on pin HICCUP reaches V_{DD} − 0.7 V. This duration is determined by a fixed 300 μs per 1 nF of the hiccup capacitor value at a V_{DD} of 5 V. A fixed recovery time of 200 μs is added after all faults have disappeared, for re-calibration in case an OverTemperature Proctection (OTP) or OCP event has occurred.

If the error is still present after the hiccup period, the hiccup restarts. If the error is removed, the $\overline{INT}$ line is cleared and the chip reverts to normal operation. The protection status register content is not automatically cleared.

The external controller can force the protection status to be cleared at any time via the I^2C-bus interface. This is done by writing FFh into the protection status register at address 03h.

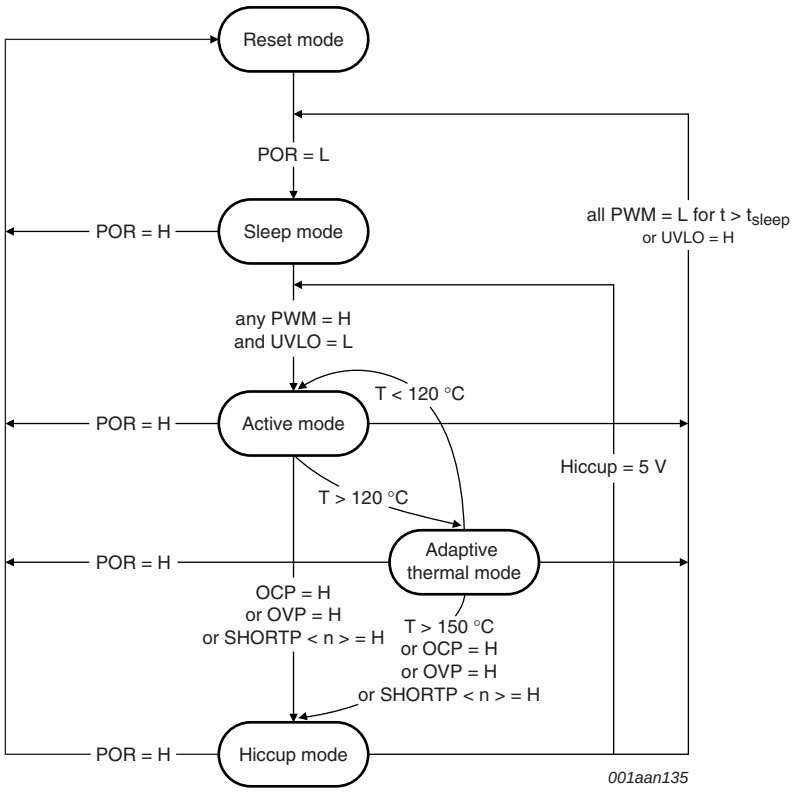


Fig 5. State diagram

8.9 Boost converter

The boost converter is designed to handle a boost ratio from 1 to 4 with an input voltage from 10 V to 42 V (24 V nominal). The maximum output voltage is 75 V which is suitable for a string of up to 20 LEDs.

The UBA3077HN embeds a 0.6 Ω on-resistance MOSFET switch. It operates with a 500 kHz fixed switching frequency derived from an internal oscillator. An embedded slope compensation module ensures stability in Continuous Conduction Mode (CCM).

The LED string is supplied by a low-side current source with PWM dimming. A feedback loop monitors the voltage at the output of the current source and controls the DC-to-DC output voltage V_{OUT}. This loop ensures a minimum voltage headroom of 800 mV for the current source.

The UBA3077HN is specifically designed for operating with an output capacitor value of 2 μF. This allows audio noise to be removed by a high quality capacitor.

8.10 PWM control

8.10.1 Direct control

After a POR, the UBA3077HN is ready to work in direct control mode by default, accepting PWM signals on pins PWM1, PWM2 and PWM3 and amplifying them to the corresponding channels. The UBA3077HN supports a PWM frequency up to 24 kHz.

In direct control mode (bit PWMSEL set to logic 0), if control register 02h bit PWM_SHIFT is set to logic 0, all three PWMn inputs directly control channels 1, 2 and 3 respectively in a transparent manner. If bit PWM_SHIFT is set to logic 1, only input PWM1 is considered and PWM2 and PWM3 are overridden internally. Channel 1 is then driven by the signal on pin PWM1 while channel 2 and channel 3 are driven by the signal on pin PWM1 phase-shifted by 120° and 240° respectively. An internal PLL, based on the internal CCO, is used to determine, on-the-fly, the PWM1 frequency and to execute the phase shift.

8.10.1.1 I²C-bus based control

If bit PWMSEL is set to logic 1, the PWM dimming control signals are generated on-chip, overriding the signal on inputs PWM1, PWM2 and PWM3. The characteristics of these PWM control signals are set via the I²C-bus interface. The PWM frequency range is 2.0 kHz to 24 kHz and the control signal is common to all channels. The phase between channels is controllable using bit PWM_SHIFT.

The PWM frequency is set with the following formula:

f_{PWM} = 32 MHz / (K × 210)

K = PLLMSB[3:0] + 1 + PLLLSB[7:0] / 256, limited to 16 (maximum)

The minimum PWM signal pulse-width is 1 % of the 24 kHz period: 417 ns.

The PWM duty cycle changes according to the value of registers PWM MSB (address 00h) and PWM LSB (address 01h). The duty cycle changes either immediately if a value change occurs (VSYNC_EN bit set to logic 0) or is synchronized with the VSYNC input signal (VSYNC_EN bit set to logic 1). In the latter case, the change occurs when VSYNC signal is HIGH (bit VSYNCPOL set to logic 0) or is LOW (bit VSYNCPOL set to logic 1).

By default, all three channels are driven by an identical PWM signal. The three internally generated PWM control signals to the three channels can be phase shifted equally by 120 ° by setting control register (address 02h) PWM_SHIFT bit to logic 1.

8.11 LED current sources

The LED current generation path is fully integrated. This helps minimize the BOM cost while still providing an LED current that has good accuracy (2 % maximum at 150 mA).

The UBA3077HN provides an accurate 1 V voltage reference from which a current reference is derived using an external resistor R_{IREF}.

This reference is accurately copied and multiplied at a ratio of 400, resulting in an LED current equal to 400 / R_{IREF} in each of the 3 channels. The DC-to-DC boost converter design, including heat dissipation capability, allows a maximum current of 150 mA per channel. The accuracy of the LED current decreases at lower LED current values.

Current switching is implemented by an integrated PWM switch. To avoid problems with ringing due to parasitic inductance present on the LED string, the rise time is programmable to two possible values: 250 ns (default) and 500 ns. These values represent the LED current 10 % to 90 % transition time.

8.12 Protection circuits

Several protection circuits are integrated to protect the device and the application against defects. If a defect is detected, the converters and LED current source switching are inhibited, and the interrupt line is immediately pulled LOW. The exact nature of the defect is stored in register 03h and accessible via the I^2C-bus interface enabling the system to decide the correct action to take.

The UBA3077HN's embedded protection circuits are: overvoltage/open LED string (OVP), DC-to-DC overload/LED string short to ground (SHORTP), overtemperature (OTP) and overcurrent (OCP).

DC-to-DC and PWM deactivation occurs on channel n and bits SHORTPn or OVPn are set if a SHORTP or OVP event occurs on channel n. Whereas THERMP and OCP events act on all channels at the same time.

Fault recovery operation is described at Section 8.8.

8.12.1 OVP (open LED string)

A dedicated OVP is implemented per channel. It monitors and signals if the output voltage (V_{OUT}) exceeds the predefined limit (77 V typical). This protection is also triggered if the LED string is cut (open LED string).

If this fault occurs, the status bit(s) OVP 1, 2 and/or 3 are set in the protection status register accordingly and both the related DC-to-DC converter and LED current source are stopped immediately.

8.12.2 LED string shorted to ground protection

A dedicated LED string shorted to ground protection is implemented per channel. If this fault occurs, the voltage at pin FB of the faulty channel remains below 0.9 V whereas a current continues to flow through the LED string. To compensate, the DC-to-DC converters try to transfer as much energy as possible leading to the peak coil current exceeding the maximum limit (coil saturation current). This triggers the protection.

If this fault occurs, the status bit(s) SHORTP 1, 2 and/or 3 are set in the protection status register accordingly and both the related DC-to-DC converter and LED current source are stopped immediately.

8.12.3 OverTemperature Protection (OTP)

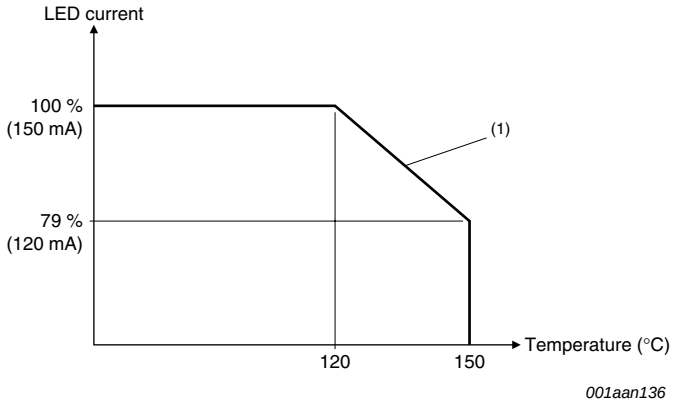
In normal operation, at an ambient temperature up to 80 °C, the die temperature must not exceed 120 °C.

Above 120 °C, UBA3077HN features an adaptive temperature protection.

Internally, the chip senses the junction temperature of the die. When higher than 120 °C, the actual junction temperature is stored in Thermal register 04h bits TSENSOR[2:0] and the adaptive thermal protection is triggered (default configuration). This thermal information can be read by the application via the I^2C-bus.

Figure 6 shows if the adaptive thermal protection is active, the peak LED current is progressively decreased in 3 % steps at each 4 °C increase in temperature above 120 °C.

If the chip temperature exceeds 150 °C, the chip enters the Hiccup mode, all DC-to-DC converters and LED current sources are disabled and the THERMP flag is set in the 03h status register. Normal operation resumes only when the chip temperature is below 120 °C.



(1) At each 4 °C step increase in temperature the LED current is reduced by 3 %.

Fig 6. Adaptive thermal protection

8.12.4 OCP

This protection is triggered if the reference current I_{REF} is too high making the peak LED current exceed 650 mA (±15 % accuracy).

If this protection is triggered, the OCP flag is set in the 03h Status register and all boost converters and current sources are disabled.

This occurs typically if the value of R_{IREF} is too low.

8.12.5 UVLO

If the voltage on pin V_{IN} ($V_{DD(24V)}$) falls below the UVLO threshold level (UVLO), the device stops operating. Normal operation resumes only when $V_{DD(24V)}$ is above the rising UVLO threshold. All register settings are maintained while $V_{DD(5V)}$ is above the POR falling threshold level.

This protection does not generate an interrupt on the $\overline{INT}$ line and is not flagged in the Status register.

8.12.6 POR

A voltage supervisor constantly monitors the supplies to pins V_{DD} and V_{IN}. If the voltage on pin V_{DD} and/or pin V_{IN} voltage falls below the falling POR threshold level, the chip enters the reset state and cannot operate or be configured. All register values are then set to their default value.

The chip can be programmed again when the voltage on pin V_{DD} and/or pin V_{IN} is above the POR rising threshold value.

8.12.7 Peak current limit

To avoid inductor saturation, the device is equipped with a peak current limit function which limits the peak inductor current to 2.5 A. If this occurs, a short-circuit protection is triggered and bit SHORTP of the faulty channel is set to logic 1 in the 03h Status register.

8.12.8 Interrupt line

Interrupt pin $\overline{INT}$ is an active LOW open-drain output. Multiple devices can be connected as a wired OR using the same interrupt line to the external control logic. On the interrupt line, only one pull-up resistor is required in the complete system.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Voltages referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(24V)}$	supply voltage (24 V)		–0.5	+45	V
$V_{DD(5V)}$	supply voltage (5 V)		–0.5	+6	V
$V_{DD(IO)}$	input/output supply voltage		–0.5	+6	V
V_{IH}	HIGH-level input voltage	PWM1, PWM2, PWM3, SCL, SDA, SAD0, SAD1	–0.5	+6	V
		LX1, LX2, LX3, VOUT1, VOUT2, VOUT3, FB1, FB2, FB3	–0.5	+85	V
V_{GND}	ground supply voltage	SGND, PGND11, PGND12, PGND13, PGND21, PGND22, PGND23	–0.5	+0.5	V
P_{tot}	total power dissipation	continuous; T_{amb} = 80 °C, forced convection	-	2.2	W
T_j	junction temperature		–40	+150	°C
T_{stg}	storage temperature		–40	+150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); all pins	–2	+2	kV
		Machine Model (MM); all pins	–100	+100	V
		filed charged device model (FCDM); all pins	–500	+500	V

10. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	<tbd>	K/W

[1] The junction to ambient thermal resistance is dependent on the board layout, PCB material application, and environmental conditions.

11. Characteristics

Table 8. Characteristics

V_{IN} = 24 V; V_{DD} = 5 V; $V_{DD(IO)}$ = 5 V; T_{amb} = 0 °C to 80 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General voltage levels						
$V_{DD(24V)}$	supply voltage (24 V)	pin V_{IN}	10	24	42	V
$V_{DD(5V)}$	supply voltage (5 V)	pin V_{DD} with $I_{DD(5V)}$ < 35 mA	4.5	5	5.5	V
$V_{DD(IO)}$	input/output supply voltage	pin $V_{DD(IO)}$ with $I_{DD(IO)}$ < 1 mA	1.62	-	5.5	V
V_{UVLO}	undervoltage lockout voltage	$V_{DD(24V)}$ falling edge	7.8	8.3	8.7	V
		$V_{DD(24V)}$ rising edge	8.35	8.9	9.35	V
V_{POR}	power-on reset voltage	$V_{DD(5V)}$ falling edge	2.4	3.6	4.3	V
		$V_{DD(5V)}$ rising edge	2.6	3.7	4.5	V
V_{hys}	hysteresis voltage	for UVLO on $V_{DD(24V)}$ rising edge	550	600	650	mV
		for POR on $V_{DD(5V)}$ rising edge	50	100	200	mV
General current levels						
$I_{DD(24V)}$	supply current (24 V)		-	100	-	µA
$I_{DD(5V)}$	supply current (5 V)	Sleep mode; internal CCO on	-	2	2.8	mA
		Active mode; internal CCO on; 150 mA I_{LED}; 100 % PWM duty cycle; all 3 channels active	-	21	-	mA
$I_{DD(IO)}$	input/output supply current	24 kHz PWM	-	-	100	µA
$I_{leak(LX)}$	leakage current on pin LX	Sleep mode	-	-	10	µA
Pin IREF						
$V_{ref(IREF)}$	reference voltage on pin IREF	pin IREF	0.98	1.00	1.02	V
$R_{ext(IREF)}$	external resistor on pin IREF		2667	-	-	Ω
Pin HICCUP						
V_{HICCUP}	voltage on pin HICCUP		0	-	$V_{DD(5V)}$	V
I_{HICCUP}	current on pin HICCUP		9.5	13	16.5	µA
High power LED parameters (for the 3 channels)						
V_O	output voltage	pins V_{OUT1}, V_{OUT2} and V_{OUT3}	$V_{DD(24V)}$	-	75	V
N_{VBR}	voltage boost ratio		1	-	4	
V_{FB}	voltage on pin FB	PWM on; static with 100 % PWM duty cycle	-	0.9	1.2	V
I_{LED}	LED current	pin FB; R_{IREF} = 2267 Ω; R_{IREF} accuracy = 0.1 %; PWMn = HIGH	147	150	153	mA
		PWMn = LOW; V_{FBn} = 75 V; leakage current	-	-	5	µA

Table 8. Characteristics *...continued*

V_{IN} = 24 V; V_{DD} = 5 V; $V_{DD(IO)}$ = 5 V; T_{amb} = 0 °C to 80 °C, unless otherwise specified.

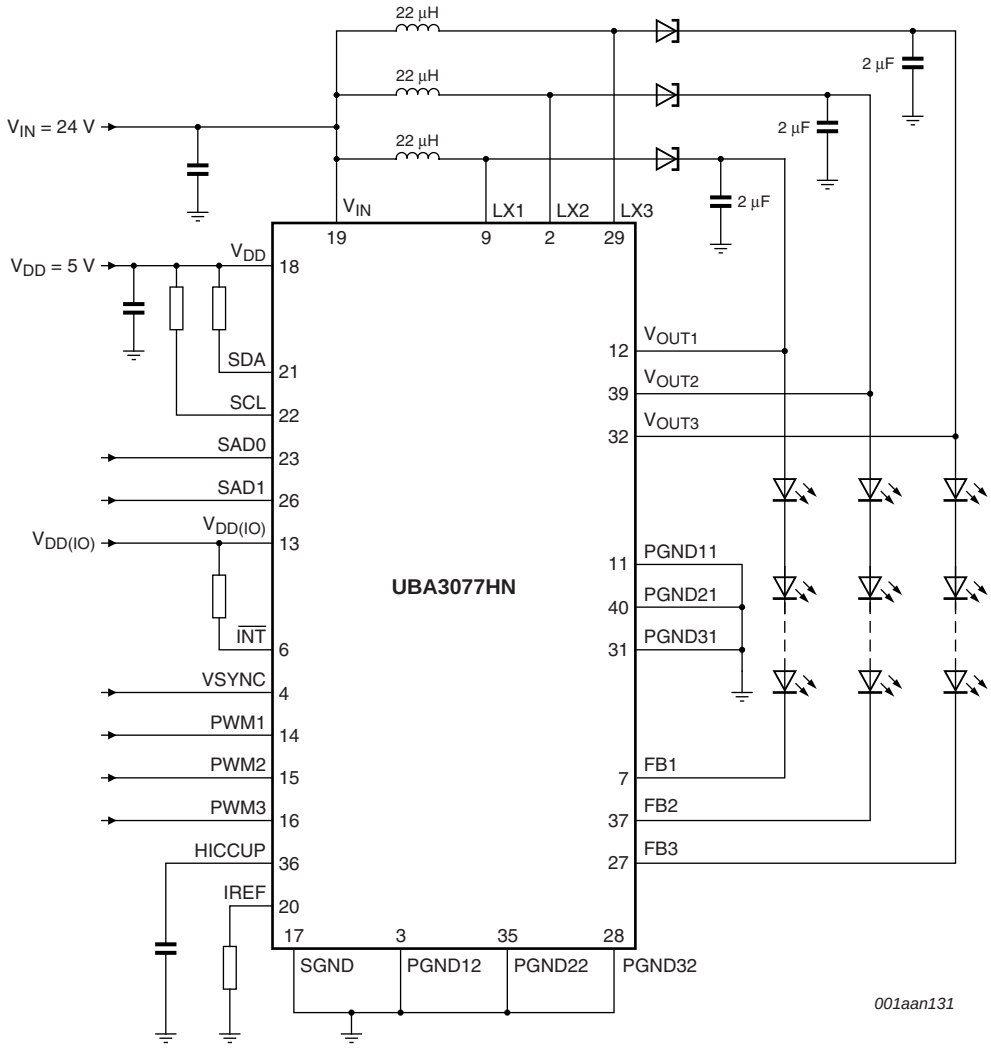
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{r(I)LED}$	LED current rise time	bit ILED_SLOPE = 0; 10 % to 90 % of I_{LED}	200	250	300	ns
		bit ILED_SLOPE = 1; 10 % to 90 % of I_{LED}	400	500	600	ns
$t_{f(I)LED}$	LED current fall time		-	300	-	ns
PWM signals						
f_{PWM}	PWM frequency	internal PWM generator; external PWM signal	2.0	-	24	kHz
δ_{PWM}	PWM duty cycle	internal PWM generator; external PWM signal	0.1	-	100	%
$t_{w(PWM)H}$	HIGH level PWM pulse width	internal PWM generator; external PWM signal	417	-	-	ns
φ_{PWM}	PWM phase shift	internal PWM generator; CLK_SEL[1:0] = 01	100	120	140	deg
$t_{d(sleep)}$	sleep mode delay time	pins PWM1, PWM2, PWM3 inactive (LOW)	1	-	3.5	s
Power MOSFETs						
R_{DSon}	drain-source on-state resistance		-	0.5	1	Ω
Timing						
f_{sw}	switching frequency	DC-to-DC	400	500	600	kHz
δ_{max}	maximum duty cycle	DC-to-DC	-	-	80	%
I²C-bus interface						
V_{IL}	LOW-level input voltage		-	-	0.5	V
V_{IH}	HIGH-level input voltage		2	-	$V_{DD(5V)}$	V
V_{OL}	LOW-level output voltage	I_{sink} = 3 mA	0	-	0.3	V
f_{SCL}	SCL clock frequency		-	-	400	kHz
Digital levels: pins VSYNC, PWM1, PWM2 and PWM3						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD(IO)}$	-	$V_{DD(IO)}$	V
Digital levels: pins SAD0 and SAD1						
V_{IL}	LOW-level input voltage		0	-	0.5	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD(5V)}$	-	$V_{DD(5V)}$	V
Digital levels: pin $\overline{INT}$						
V_{OL}	LOW-level output voltage	I_{sink} = 3 mA	0	-	0.3	V
I_{IH}	HIGH-level input current		0	-	0.5	µA
Protection and limitations						
$I_{th(ocp)}$	overcurrent protection threshold current	pin IREF	1.35	1.65	1.85	mA
$V_{th(ovp)}$	overvoltage protection threshold voltage	pins V_{OUT1}, V_{OUT2}, V_{OUT3}	75	77	85	V

Table 8. Characteristics *...continued*

V_{IN} = 24 V; V_{DD} = 5 V; $V_{DD(IO)}$ = 5 V; T_{amb} = 0 °C to 80 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{lim(L)M}$	peak inductor current limit	on pin LXn	2	2.5	3	A
T_{amb}	ambient temperature	operating	0	-	80	°C
$T_{th(otp)}$	overtemperature protection threshold temperature	die junction temperature	-	150	-	°C

12. Application information

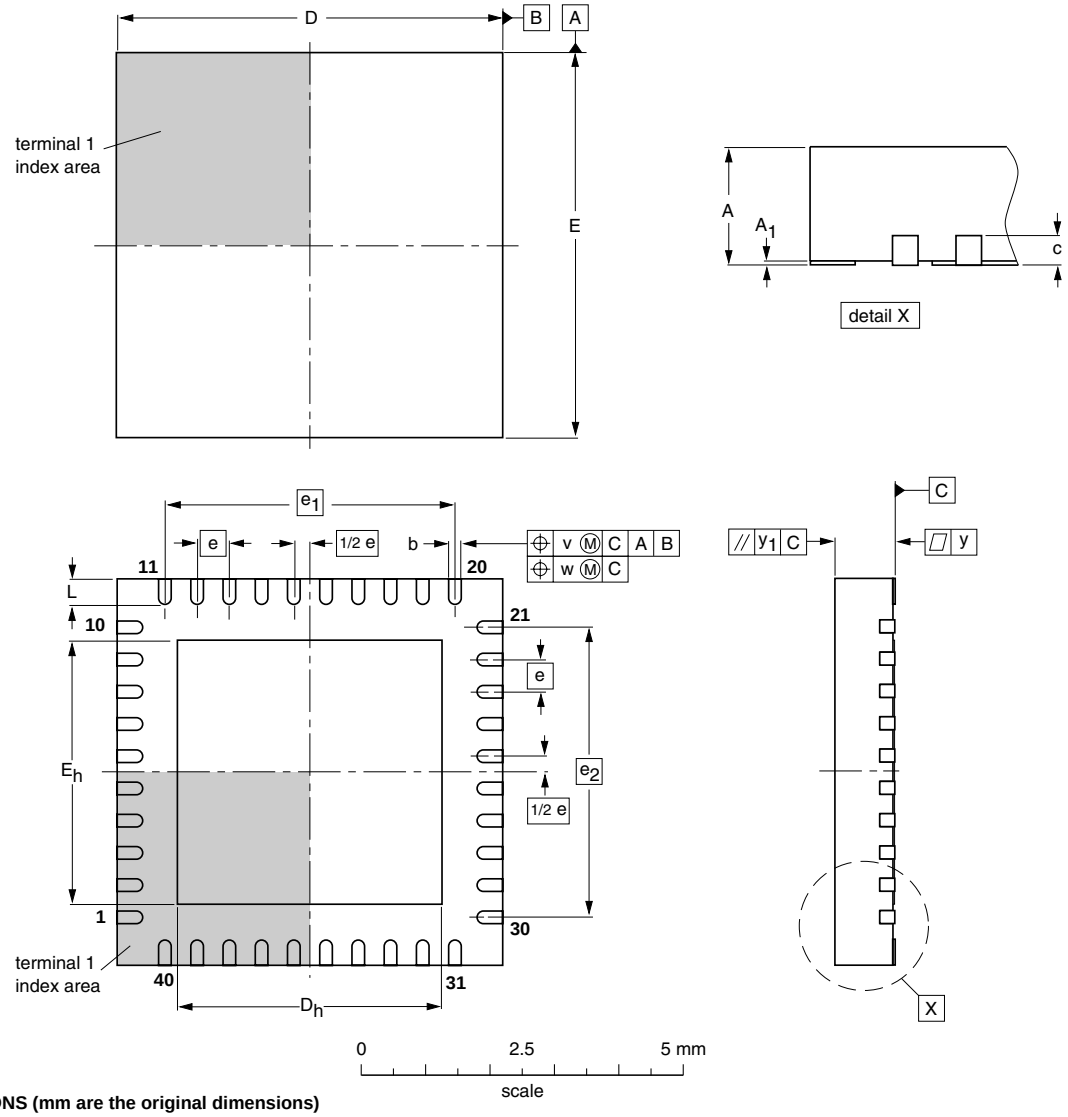


Refer to the application notes for PCB design recommendations.

Fig 7. Typical application diagram

13. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 8. Package outline SOT618-1 (HVQFN40)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
BOM	Bill Of Materials
CCO	Current Controlled Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
PLL	Phase Locked Loop
POR	Power-On-Reset
PWM	Pulse-Width Modulated or Pulse-Width Modulator

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UBA3077HN v.1	20110208	Objective data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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