



Custom Clock Generator for FAX System

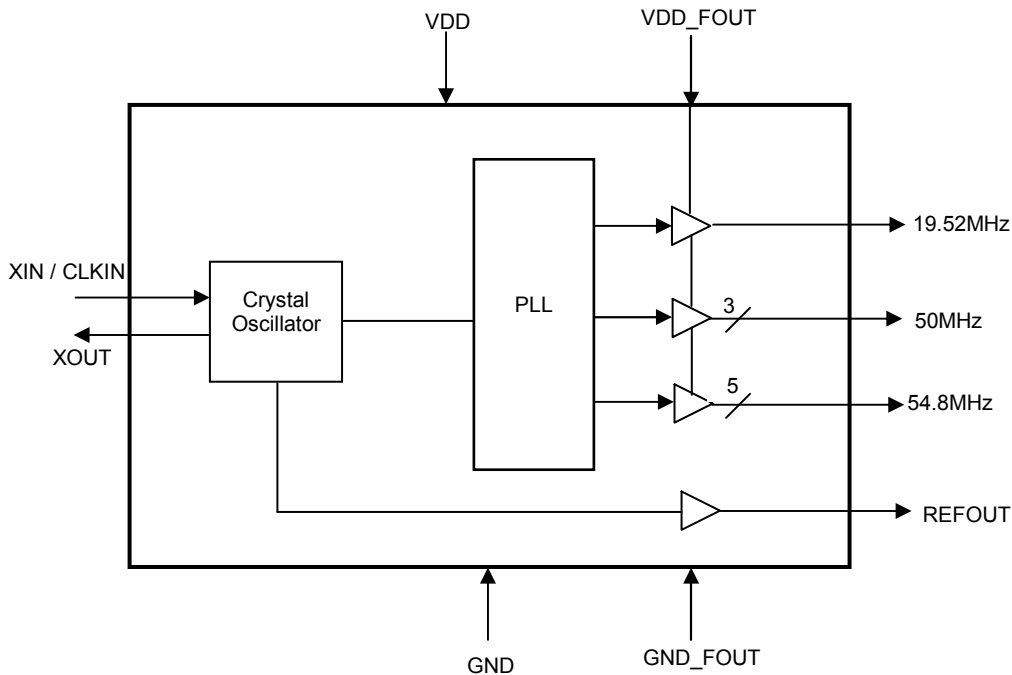
Features

- Generates Custom Clocks for FAX system from an inexpensive 24MHz Crystal
- 3 x 50MHz synchronized clocks
- 5 x 54.8MHz synchronized clocks
- 1 x 19.52MHz clock for Scanner
- REFOUT Clock
- Supply Voltage $3.3\text{ V} \pm 0.3\text{V}$
- Available in 16L TSSOP, Green package

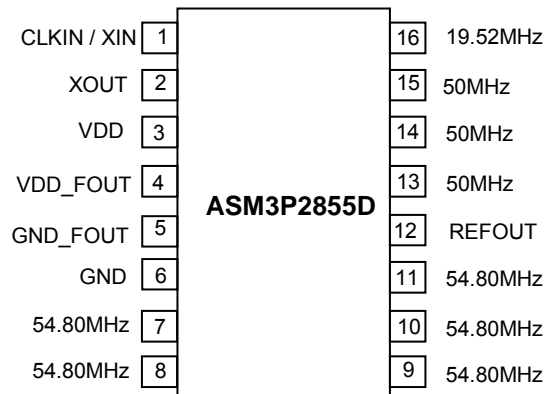
Product Description

ASM3P2855D is a custom clock generator for FAX system. ASM3P2855D realizes all the ten clocks required by the various components and subsystems of the FAX system. It uses an inexpensive 24MHz crystal as the input to generate five synchronized 54.8MHz clocks and three synchronized 50MHz PCI clocks that can be used by CPU, HDD, PCI Analyzer, ASIC2 and ASIC3, Ethernet, LAN PHY and for the CPU Timer, a 19.52MHz clock used by ASIC1 for Scanner. The custom clock generator ASM3P2855D works with a Supply Voltage of $3.3\text{V} \pm 0.3\text{V}$. The device is available in a 16L TSSOP Green package.

Block Diagram



Pin Diagram



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	Crystal connection or external reference Clock input.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	VDD	P	Power supply for the core
4	VDD_FOUT	P	Power supply for the output buffers.
5	GND_FOUT	P	Ground connection for the output buffers
6	GND	P	Ground connection
7	54.80MHz	O	Synchronous 54.80MHz Clock Output
8	54.80MHz	O	Synchronous 54.80MHz Clock Output
9	54.80MHz	O	Synchronous 54.80MHz Clock Output
10	54.80MHz	O	Synchronous 54.80MHz Clock Output
11	54.80MHz	O	Synchronous 54.80MHz Clock Output
12	REFOUT	O	24MHz Reference Clock Output
13	50MHz	O	Synchronous 50MHz Clock Output
14	50MHz	O	Synchronous 50MHz Clock Output
15	50MHz	O	Synchronous 50MHz Clock Output
16	19.52MHz	O	19.52MHz Clock Output

ASM3P2855D

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, VDD_FOUT	Power Supply Voltage relative to GND	-0.5 to +4.6	V
V _{IN}	Input Voltage relative to GND (Input Pins)	-0.5 to VDD+0.5	
T _{STG}	Storage temperature	-65 to +125	°C
T _s	Max. Soldering Temperature (10 sec)	260	°C
T _J	Junction Temperature	150	°C
T _{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
T _A	Operating Temperature	0		+70	°C
VDD	Output Core Voltage	+3.0	+3.3	+3.6	V
VDD_FOUT	Output Buffer Voltage	+3.0	+3.3	+3.6	V

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V _{IL}	Input low voltage	GND-0.3		0.8	V
V _{IH}	Input high voltage	2.0		VDD+0.3	V
I _{IL}	Input low current			-35	µA
I _{IH}	Input high current			35	µA
I _{XOL}	XOUT output low current (V _{XOL} @ 0.4V, VDD = 3.3V)		3		mA
I _{XOH}	XOUT output high current (V _{XOH} @ 2.5V, VDD = 3.3V)		3		mA
V _{OL}	Output low voltage (VDD = 3.3V, I _{OL} = 10mA)			0.4	V
V _{OH}	Output high voltage (VDD = 3.3V, I _{OH} = -10mA)	2.5			V
I _{DD}	Static supply current ¹			12	mA
I _{CC}	Dynamic supply current (VDD = 3.3V, Unloaded Outputs)		32		mA
VDD	Operating Core Voltage	3.0	3.3	3.6	V
VDD_FOUT	Operating Buffer Voltage	3.0	3.3	3.6	V
t _{ON}	Power-up time (first locked cycle after power-up) ²			5	mS
Z _O	Output impedance		30		Ω

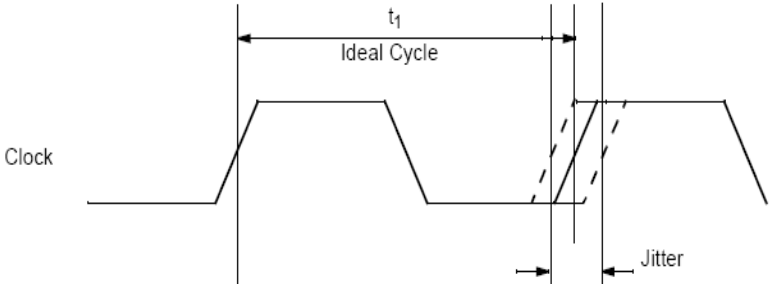
Notes: 1. CLKIN / XIN is pulled to GND.
2. VDD and CLKIN inputs are stable.

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
XIN / CLKIN	Input frequency		24		MHz
F _{OUT}	Output frequency	At Pin 12	24		MHz
		At Pins 7,8,9,10,11	54.80		
		At Pins 13,14,15	50		
		At Pin 16	19.52		
t _{LH} ¹	Output rise time (measured from 20% to 80%)		1.0		nS
t _{HL} ¹	Output fall time (measured from 80% to 20%)		1.0		nS
t _D	Output duty cycle	45	50	55	%
t _{JP}	Period Jitter (Unloaded Outputs)			±275	pS

Note: 1. t_{LH} and t_{HL} are measured into a capacitive load of 15pF.

Period Jitter

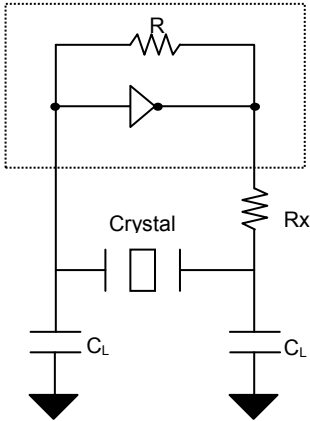


Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	24MHz
Frequency tolerance	± 50 ppm or better at 25°C
Operating temperature range	-25°C to +85°C
Storage temperature	-40°C to +85°C
Load capacitance(C _P)	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

Note: Note: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

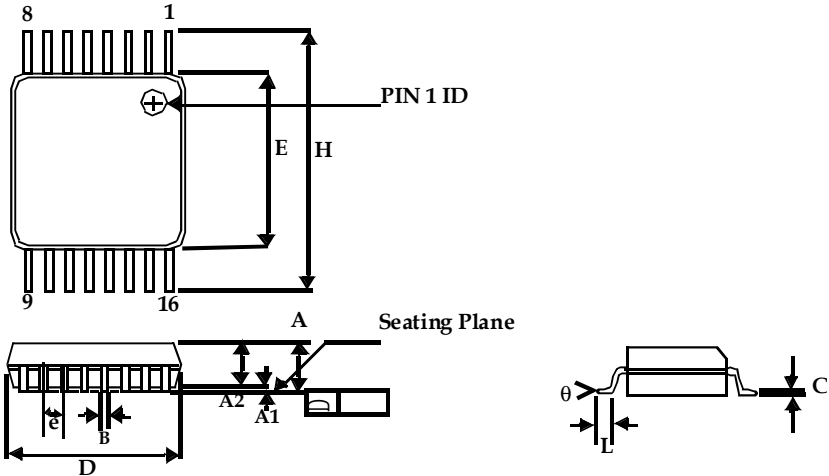
Typical Crystal Interface Circuit



$C_L = 2 * (C_P - C_S)$,
 Where C_P = Load capacitance of crystal
 C_S = Stray capacitance due to C_{IN}, PCB, Trace etc.

Package Information

16-lead Thin Shrunken Small Outline Package (4.40-MM Body)




Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
theta	0°	8°	0°	8°

ASM3P2855D

Ordering Code

Ordering Code	Marking	Package Type	Operating Range
ASM3P2855DG-16TR	3P28 55D	16-pin 4.4-mm TSSOP - TAPE & REEL, Green	0°C to +7 0°C

A "microdot" placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. U.S Patent Pending; Timing-Safe and Active Bead are trademarks of PulseCore Semiconductor, a wholly owned subsidiary of ON Semiconductor. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855
Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website:
www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative