

**ON Semiconductor®**<http://onsemi.com>

# LC87F7932B

## CMOS IC

**32K-byte FROM and 2048-byte RAM integrated**

## 8-bit 1-chip Microcontroller

### Overview

The LC87F7932B is an 8-bit microcontroller that, centered around a CPU running at a minimum bus cycle time of 250ns, integrates on a single chip a number of hardware features such as 32K-byte flash ROM (onboard programmable), 2048-byte RAM, an on-chip debugger, an LCD controller/driver, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), two 16-bit timers/counters (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a real time clock function (RTC), a base timer serving as a time-of-day clock, a synchronous SIO interface with automatic transfer function, an asynchronous/synchronous SIO interface, a UART interface (full duplex), a 7-channel AD converter with a 12-/8-bit resolution selector, a high-speed clock counter, a system clock frequency divider, an internal reset circuit, and a 21-source 10-vector interrupt function.

### Features

#### ■Flash ROM

- Capable of on-board programming with a wide supply voltage range of 3.0V to 5.5V
- 128-byte block erase
- $32768 \times 8$  bits

#### ■RAM

- $2048 \times 9$  bits

#### ■Minimum Bus Cycle Time

- 250ns (4MHz)  $V_{DD}=2.4V$  to 3.6V

Note: The bus cycle time here refers to the ROM read speed.

#### ■Minimum Instruction Cycle Time (tCYC)

- 750ns (4MHz)  $V_{DD}=2.4V$  to 3.6V

\* This product is licensed from Silicon Storage Technology, Inc. (USA).

**■Operating Temperature Range**

- -40°C to +85°C

**■Ports**

- Normal withstand voltage I/O ports

Ports whose input/output can be programmed in 1-bit units: 21 (P0n, P1n, P30, P70 to P73)

Multiplexed functions

Input ports (for debugger): 3 (DBGP0 (P05) to DBGP2 (P07))

LCD ports (segment output): 8 (P1n)

- LCD ports/general purpose I/O ports

Segment output: 32 (S00 to S31)

Common output: 4 (COM0 to COM3)

Bias power supply for LCD driving 5 (V1 to V3, CUP1, CUP2)

Multiplexed functions

Input/output ports: 36 (LPAn, LPBn, LPCn, LPL0 to LPL3, P1n)

- Oscillator pins:

4 (CF1, CF2, XT1, XT2)

- Reset pin:

1 ( $\overline{\text{RES}}$ )

- Power supply:

5 (VSS1, VSS2, VDD1, VDD2, V2)

**■LCD Controller**

(1) Seven display modes are available

(2) Duty: 1/3 duty, 1/4 duty

(3) Bias: 1/2 bias, 1/3 bias

(4) Segment/common output can be switched to general purpose I/O ports.

(5) LCD power range

1) 1/3 bias V1: 1.2V to 1.8V

V2: 2.4V to 3.6V

V3: 3.6V to 5.4V

An LCD panel that supports the  $V2 (=V_{DD}) \times 1.5[V]$  must be used when 1/3 bias is selected.

If the supply voltage  $V_{DD}$  is 3.0V, for example, use an LCD panel that supports 4.5V.

2) 1/2 bias V1: 1.2V to 1.8V

V2: 2.4V to 3.6V

V3: 2.4V to 3.6V

(Connect V2 and V3 externally.)

An LCD panel that supports the  $V2 (=V_{DD})[V]$  must be used when 1/2 bias is selected.

If the supply voltage  $V_{DD}$  is 3.0V, for example, use an LCD panel that supports 3.0V.

**■Timers**

- Timer 0: 16 bit timer/counter with a capture register

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers)  $\times$  2 channels

Mode 1: 8 bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)

Mode 2: 16 bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16 bit counter (with a 16 bit capture register)

- Timer 1: 16 bit timer/counter that supports PWM/toggle output

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle output) + 8-bit timer/counter (with toggle output)

Mode 1: 8-bit PWM with an 8-bit prescaler  $\times$  2 channels

Mode 2: 16 bit timer/counter with an 8-bit prescaler (with toggle output)

(Toggle outputs also from the low-order 8 bits)

Mode 3: 16 bit timer with an 8-bit prescaler (with toggle output)

(The low-order 8 bits can be used as a PWM.)

- Timer 4: 8-bit timer with a 6-bit prescaler

- Timer 5: 8-bit timer with a 6-bit prescaler

- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)

- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)

- Base Timer

(1) The clock can be selected from any of the following:

Subclock (32.768kHz crystal oscillator/low-speed RC oscillator), system clock, and timer 0 prescaler output.

(2) Interrupts can be generated at five specified time intervals.

**■High-speed Clock Counter**

- (1) Capable of counting a clock with a maximum clock rate of 8MHz (at a main clock of 4MHz).
- (2) Real-time output

**■Serial Interface**

- SIO0: 8-bit synchronous serial interface
  - (1) Synchronous 8-bit serial I/O (2- or 3-wire configuration, 4/3 to 512/3 tCYC transfer clock rate)
  - (2) Continuous data transfer (variable length data transfer in bit units from 1 to 256 bits, 4/3 to 512/3 tCYC transfer clock rate)
  - (3) Bi-phase modulation
    - Manchester/Bi-phase-Space data transfer
  - (4) LSB first/MSB first selectable
  - (5) SPI function: HOLD/X'tal HOLD mode release function upon receipt of a 1-byte (8-bit clock).
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clock rate)
  - Mode 1: Asynchronous serial I/O (half duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrate)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clock rate)
  - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

**■UART**

- Full duplex
- Data length: 7/8/9 bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator
- Operating mode: Programmable transfer mode, fixed-rate transfer mode
- Transfer data conversion: Normal (NRZ), Manchester encoding

**■AD Converter: 12 bits/8 bits × 7 channels**

- 12-/8-bit AD converter resolution selectable

**■Remote Control Receiver Circuit (multiplexed with the P73/INT3/T0IN pin)**

- Noise rejection function (Noise filter time constant selectable from 1/32/128 tCYC)

**■Watchdog Timer**

- Generation of interrupt or system reset selectable
- Two types of watchdog timer
  - (1) Watchdog timer using an external RC circuit
  - (2) Watchdog timer using the microcontroller's base timer
- Detection intervals (1/2/4/8 seconds) can be selected for the watchdog timer that uses the base timer by configuring options.

**■Buzzer Output**

- Generates buzzer output from P17 using the base timer.

**■Real Time Clock (RTC)**

- (1) Uses the base timer to count the calendar years, months, days, hours, minutes, and seconds.
- (2) Calendar counts up to December 31, 2799 and calculates leap years automatically
- (3) The RTC uses the Gregorian calendar, which maintains GMT (Greenwich Mean Time).

**■Internal Reset Function**

- Power-on-reset (POR) function
  - (1) The POR causes a system reset only when power is turned on.

**■Interrupts:**

- 21 sources, 10 vectors
- (1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
- (2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the lowest vector address takes precedence.

| No. | Vector Address | Level  | Interrupt Source    |
|-----|----------------|--------|---------------------|
| 1   | 00003H         | X or L | INT0                |
| 2   | 0000BH         | X or L | INT1                |
| 3   | 00013H         | H or L | INT2/T0L            |
| 4   | 0001BH         | H or L | INT3/base timer/RTC |
| 5   | 00023H         | H or L | T0H                 |
| 6   | 0002BH         | H or L | T1L/T1H             |
| 7   | 00033H         | H or L | SIO0/UART1-receive  |
| 8   | 0003BH         | H or L | SIO1/UART-send      |
| 9   | 00043H         | H or L | ADC/T6/T7/SPI       |
| 10  | 0004BH         | H or L | Port 0/T4/T5        |

- Priority level:  $X > H > L$
- For equal priority levels, the interrupt with the lowest vector address is given priority.

**■Subroutine Stack Levels:**

- Up to 1024 levels max. (Stack is allocated in RAM.)

**■High-speed Multiplication/Division Instructions**

- 16 bits  $\times$  8 bits (5 tCYC execution time)
- 24 bits  $\times$  16 bits (12 tCYC execution time)
- 16 bits  $\div$  8 bits (8 tCYC execution time)
- 24 bits  $\div$  16 bits (12 tCYC execution time)

**■Oscillator Circuits**

- On-chip high-speed RC oscillator: For system clock (500kHz typ)
- On-chip low-speed RC oscillator: For system clock (50kHz typ)
- CF oscillator: For system clock, Rf built in, Rd external
- Crystal oscillator: For low-speed system clock, Rf built in
- On-chip variable modulation frequency RC oscillator (VMRC): For system clock
  - (1) Adjustable in  $\pm 4\%$  (typ) step from a selected center frequency
  - (2) Can measure the frequency of the source oscillator clock using an input signal from the XT1 pin as a reference.

**■System Clock Divider**

- Low consumption current operation possible
- The minimum instruction cycle can be selected from among 750ns, 1.5 $\mu$ s, 3.0 $\mu$ s, 6.0 $\mu$ s, 12 $\mu$ s, 24 $\mu$ s, 48 $\mu$ s, 96 $\mu$ s, and 192 $\mu$ s (at a main clock rate of 4MHz).

**■System Clock Output**

- The system clock can be output from the P04 pin.

**■Standby Function**

- **HALT mode:** HALT mode is used to reduce power consumption.  
Halts instruction execution while allowing the peripheral circuits to continue operation.  
(Some serial transfer functions are suspended.)
  - (1) Oscillators do not stop automatically.
  - (2) Released by a system reset or occurrence of an interrupt
- **HOLD mode:** HOLD mode is used to reduce power consumption.  
Suspends instruction execution and operation of the peripheral circuits.
  - (1) CF oscillator, RC oscillators, crystal oscillator, and VMRC oscillator stop automatically.
  - (2) There are five ways of releasing HOLD mode.
    - 1) Low level input to the reset pin
    - 2) Watchdog timer interrupt
    - 3) Specified level input to at least one of INT0, INT1, and INT2 pins
    - 4) Port 0 interrupt
    - 5) SPI interrupt by receiving 1-byte (8-bit clock)
- **X'tal HOLD mode:** X'tal HOLD mode is used to reduce power consumption.  
Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - (1) CF oscillator, RC oscillators, and VMRC oscillator stop automatically.
  - (2) The state of the crystal oscillator when X'tal HOLD mode is entered is retained.
  - (3) There are seven ways of releasing X'tal HOLD mode.
    - 1) Low level input to the reset pin
    - 2) Watchdog timer interrupt
    - 3) Specified level input to at least one of INT0, INT1, and INT2 pins
    - 4) Port 0 interrupt
    - 5) Base-timer interrupt
    - 6) RTC interrupt
    - 7) SPI interrupt by receiving 1-byte (8-bit clock)

**■On-chip Debugger**

- Supports software debugging with the IC mounted on the target board.

**■Package Form**

- QIP64E (14×14) (Lead-and-halogen-free product)
- TQFP64J (7×7) (Lead-and-halogen-free product)
- SQFP64 (10×10) (Lead-and-halogen-free product)

**■Development Tools**

- On-chip debugger: TCB87 TypeB+LC87F7932B

**■Flash ROM Programming Boards**

| Package        | Programming Boards |
|----------------|--------------------|
| QIP64E (14×14) | W87F70256Q         |
| TQFP64J (7×7)  | W87F70256TQ7       |
| SQFP64 (10×10) | W87F79256SQ        |

## LC87F7932B

### ■Flash ROM Programmer

| Maker   | Model         |                               | Supported Version                     | Device     |
|---|---------------|-------------------------------|---------------------------------------|------------|
| Flash Support Group, Inc.<br>(Formerly Ando Electric Co., Ltd.) | Single        | AF9708/AF9709/AF9709B         | Rev 03.04 or later                    | LC87F2832A |
|   | Ganged        | AF9723 (Main unit)            | Rev 0x.xx or later                    |            |
|   |               | AF9833 (Unit)                 | Rev 0x.xx or later                    |            |
| Our company   | Single/ganged | SKK/SKK Type B<br>(SANYO FWS) | Application Version<br>1.05A or later | LC87F7932B |
|   | Onboard       | SKK/SKK Type B                | Chip Data Version                     |            |
|   | Single/ganged | (SANYO FWS)                   | 2.25 or later                         |            |

For information about AF-Series:

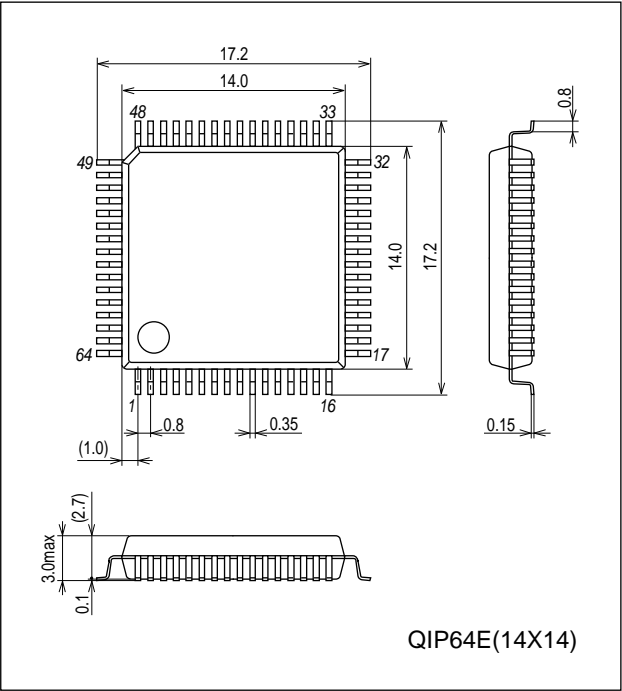
Flash Support Group, Inc.

TEL: +81-53-459-1050

E-mail: sales@j-fsg.co.jp

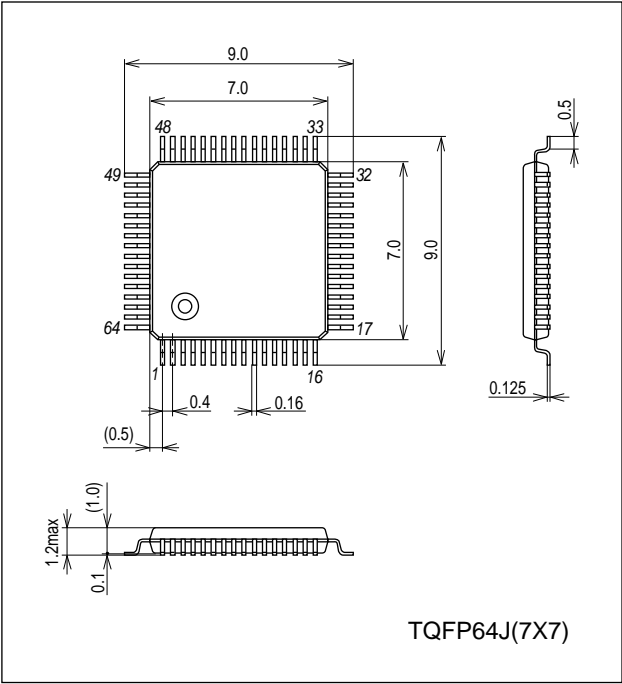
Package Dimensions

unit : mm (typ)  
3159A



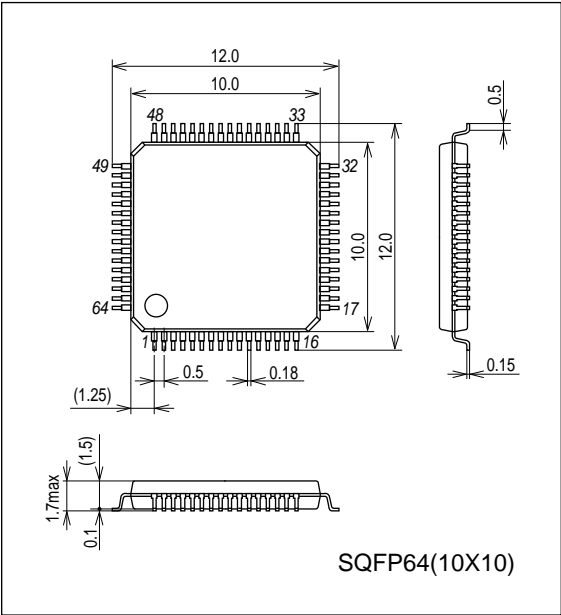
Package Dimensions

unit : mm (typ)  
3289



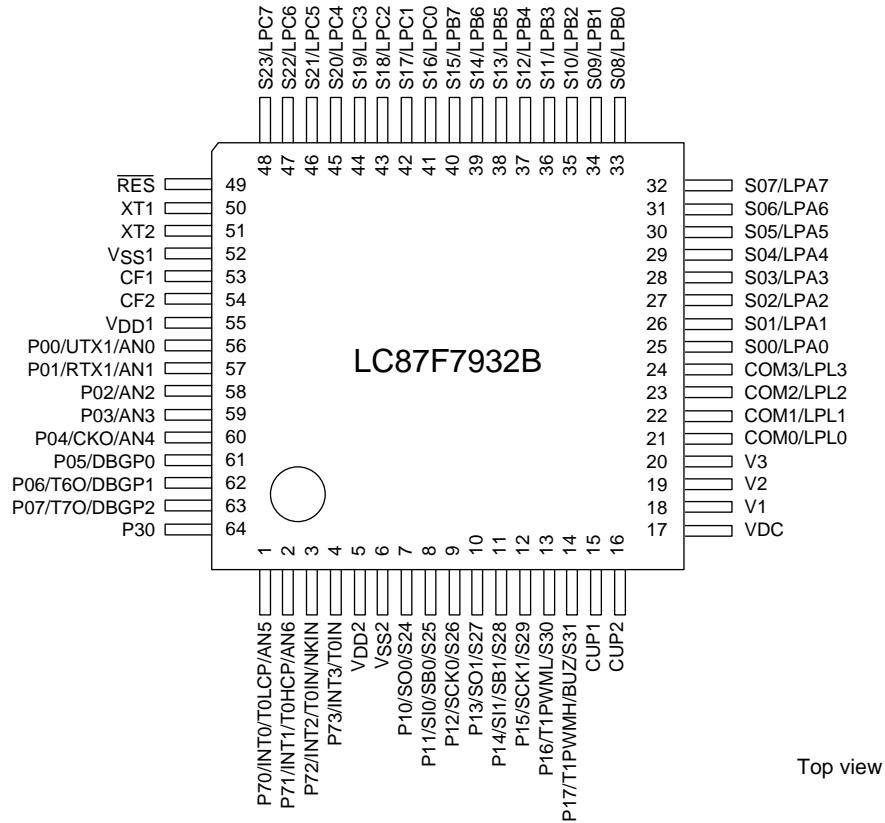
Package Dimensions

unit : mm (typ)  
3190A



# LC87F7932B

## Pin Assignment



QIP64E (14×14) “Lead-and-halogen-free product”  
 TQFP64J (7×7) “Lead-and-halogen-free product”  
 SQFP64 (10×10) “Lead-and-halogen-free product”

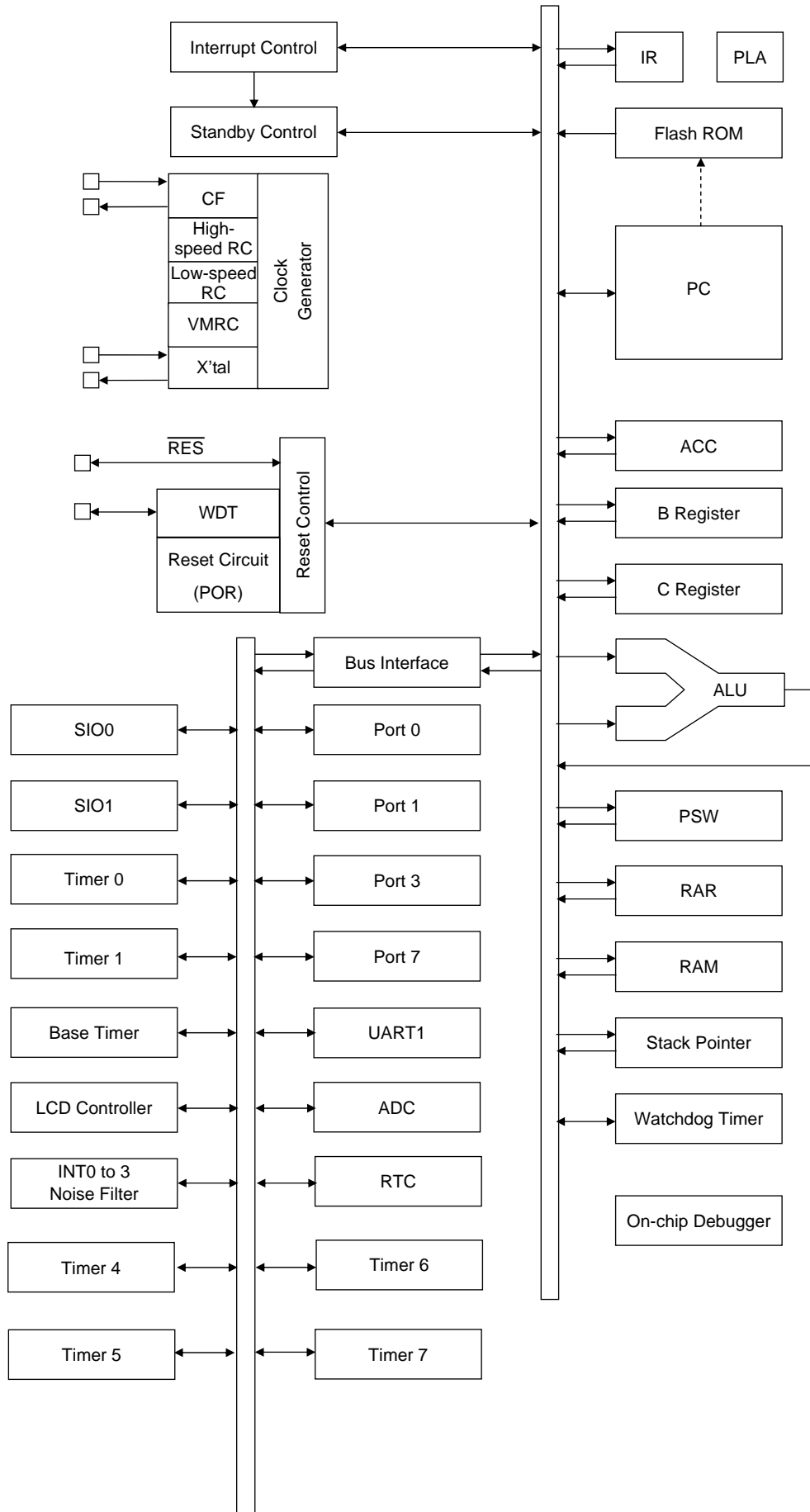


## LC87F7932B

| PIN No. | NAME               |
|---------|--------------------|
| 1       | P70/INT0/T0LCP/AN5 |
| 2       | P71/INT1/T0HCP/AN6 |
| 3       | P72/INT2/T0IN/NKIN |
| 4       | P73/INT3/T0IN      |
| 5       | V <sub>DD2</sub>   |
| 6       | V <sub>SS2</sub>   |
| 7       | P10/SO0/S24        |
| 8       | P11/SI0/SB0/S25    |
| 9       | P12/SCK0/S26       |
| 10      | P13/SO1/S27        |
| 11      | P14/SI1/SB1/S28    |
| 12      | P15/SCK1/S29       |
| 13      | P16/T1PWML/S30     |
| 14      | P17/T1PWMH/BUZ/S31 |
| 15      | CUP1               |
| 16      | CUP2               |
| 17      | VDC                |
| 18      | V1                 |
| 19      | V2                 |
| 20      | V3                 |
| 21      | COM0/LPL0          |
| 22      | COM1/LPL1          |
| 23      | COM2/LPL2          |
| 24      | COM3/LPL3          |
| 25      | S00/LPA0           |
| 26      | S01/LPA1           |
| 27      | S02/LPA2           |
| 28      | S03/LPA3           |
| 29      | S04/LPA4           |
| 30      | S05/LPA5           |
| 31      | S06/LPA6           |
| 32      | S07/LPA7           |

| PIN NO. | NAME                    |
|---------|-------------------------|
| 33      | S08/LPB0                |
| 34      | S09/LPB1                |
| 35      | S10/LPB2                |
| 36      | S11/LPB3                |
| 37      | S12/LPB4                |
| 38      | S13/LPB5                |
| 39      | S14/LPB6                |
| 40      | S15/LPB7                |
| 41      | S16/LPC0                |
| 42      | S17/LPC1                |
| 43      | S18/LPC2                |
| 44      | S19/LPC3                |
| 45      | S20/LPC4                |
| 46      | S21/LPC5                |
| 47      | S22/LPC6                |
| 48      | S23/LPC7                |
| 49      | $\overline{\text{RES}}$ |
| 50      | XT1                     |
| 51      | XT2                     |
| 52      | V <sub>SS1</sub>        |
| 53      | CF1                     |
| 54      | CF2                     |
| 55      | V <sub>DD1</sub>        |
| 56      | P00/UTX1/AN0            |
| 57      | P01/RTX1/AN1            |
| 58      | P02/AN2                 |
| 59      | P03/AN3                 |
| 60      | P04/CKO/AN4             |
| 61      | P05/DBGP0               |
| 62      | P06/T6O/DBGP1           |
| 63      | P07/T7O/DBGP2           |
| 64      | P30                     |

# System Block Diagram



# LC87F7932B

## Pin Description

| Pin Name                                 | I/O    | Description  | Option             |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
|--|--------|--|--------------------|---------|---------|--------------------|---------|---------|------|--------|--------|---------|--------|--------|------|--------|--------|---------|--------|--------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|----|
| V <sub>SS</sub> 1, V <sub>SS</sub> 2     | -      | • Power supply (-)   | No                 |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| V <sub>DD</sub> 1, V <sub>DD</sub> 2, V2 | -      | • Power supply (+)   | No                 |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| VDC                                      | -      | • Internal power supply  | No                 |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| CUP1, CUP2                               | -      | • Capacitor connecting pins for step-up/step-down circuits   | No                 |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| Port 0<br>P00 to P07                     | I/O    | <ul style="list-style-type: none"><li>• 8-bit I/O port</li><li>• I/O can be specified in 1-bit units.</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• HOLD release input</li><li>• Port 0 interrupt input</li><li>• Multiplexed functions<ul style="list-style-type: none"><li>P00: UART1 transmit data output</li><li>P01: UART1 receive data input</li><li>P04: System clock output</li><li>P05: DBGPO (LC87F7932B)</li><li>P06: Timer 6 toggle output/DBGP1 (LC87F7932B)</li><li>P07: Timer 7 toggle output/DBGP2 (LC87F7932B)</li></ul></li><li>AD converter input ports: AN0 (P00) to AN4 (P04)</li></ul>  | Yes                |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| Port 1<br>P10/S24 to<br>P17/S31          | I/O    | <ul style="list-style-type: none"><li>• 8-bit I/O port</li><li>• I/O can be specified in 1-bit units.</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Multiplexed functions<ul style="list-style-type: none"><li>P10: SIO0 data output</li><li>P11: SIO0 data input or bus I/O</li><li>P12: SIO0 clock I/O</li><li>P13: SIO1 data output</li><li>P14: SIO1 data input or bus I/O</li><li>P15: SIO1 clock I/O</li><li>P16: Timer 1 PWML output</li><li>P17: Timer 1 PWMH output/buzzer output</li></ul></li><li>Segment output for LCD: S24 (P10) to S31 (S17)</li></ul>   | Yes                |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| Port 3<br>P30                            | I/O    | <ul style="list-style-type: none"><li>• 1-bit I/O port</li><li>• I/O can be specified in 1-bit units.</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li></ul>   | Yes                |         |         |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| Port 7<br>P70 to P73                     | I/O    | <ul style="list-style-type: none"><li>• 4-bit I/O port</li><li>• I/O can be specified in 1-bit units.</li><li>• Pull-up resistors can be turned on and off in 1-bit units.</li><li>• Multiplexed functions<ul style="list-style-type: none"><li>P70: INT0 input/HOLD release input/timer 0L capture input/output for watchdog timer</li><li>P71: INT1 input/HOLD release input/timer 0H capture input</li><li>P72: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/high-speed clock counter input</li><li>P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input</li></ul></li><li>AD converter input ports: AN5 (P70), AN6 (P71)</li><li>Interrupt acknowledge type<table><tr><th></th><th>Rising</th><th>Falling</th><th>Rising and falling</th><th>H level</th><th>L level</th></tr><tr><td>INT0</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr><tr><td>INT1</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td></tr><tr><td>INT2</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr><tr><td>INT3</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td></tr></table></li></ul> |                    | Rising  | Falling | Rising and falling | H level | L level | INT0 | Enable | Enable | Disable | Enable | Enable | INT1 | Enable | Enable | Disable | Enable | Enable | INT2 | Enable | Enable | Enable | Disable | Disable | INT3 | Enable | Enable | Enable | Disable | Disable | No |
|  | Rising | Falling  | Rising and falling | H level | L level |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT0                                     | Enable | Enable   | Disable            | Enable  | Enable  |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT1                                     | Enable | Enable   | Disable            | Enable  | Enable  |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT2                                     | Enable | Enable   | Enable             | Disable | Disable |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |
| INT3                                     | Enable | Enable   | Enable             | Disable | Disable |                    |         |         |      |        |        |         |        |        |      |        |        |         |        |        |      |        |        |        |         |         |      |        |        |        |         |         |    |

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| Pin name                | I/O | Description   | Option |
|-------------------------|-----|---|--------|
| S00/LPA0 to S07/LPA7    | I/O | <ul style="list-style-type: none"> <li>Segment output for LCD</li> <li>Can be used as general purpose I/O ports (LPA)</li> </ul>  | No     |
| S08/LPB0 to S15/LPB7    | I/O | <ul style="list-style-type: none"> <li>Segment output for LCD</li> <li>Can be used as general purpose I/O ports (LPB)</li> </ul>  | No     |
| S16/LPC0 to S23/LPC7    | I/O | <ul style="list-style-type: none"> <li>Segment output for LCD</li> <li>Can be used as general purpose I/O ports (LPC)</li> </ul>  | No     |
| COM0/LPL0 to COM3/LPL3  | I/O | <ul style="list-style-type: none"> <li>Common output for LCD</li> <li>Can be used as general purpose I/O ports (LPL)</li> </ul>   | No     |
| V1 to V3                | I/O | LCD drive bias power supply   | No     |
| $\overline{\text{RES}}$ | I   | Reset pin   | No     |
| XT1                     | I/O | <ul style="list-style-type: none"> <li>32.768kHz crystal resonator input pin</li> <li>General purpose input port</li> <li>Must be connected to <math>V_{DD1}</math> if not to be used.</li> </ul> | No     |
| XT2                     | I/O | <ul style="list-style-type: none"> <li>32.768kHz crystal resonator output pin</li> <li>General purpose I/O port</li> <li>Must be set for oscillation and kept open if not to be used.</li> </ul>  | No     |
| CF1                     | I   | <ul style="list-style-type: none"> <li>Ceramic resonator input pin</li> <li>Must be connected to <math>V_{DD1}</math> if not to be used.</li> </ul>   | No     |
| CF2                     | O   | <ul style="list-style-type: none"> <li>Ceramic resonator output pin</li> <li>Must be kept open if not to be used.</li> </ul>  | No     |

## Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in output mode.

| Port                   | Options Selected in Units of | Option Type | Output Type   | Pull-up Resistor |
|------------------------|------------------------------|-------------|---|------------------|
| P00 to P07             | 1 bit                        | 1           | CMOS  | Programmable     |
|                        |                              | 2           | N-channel open drain  | Programmable     |
| P10 to P17             | 1 bit                        | 1           | CMOS  | Programmable     |
|                        |                              | 2           | N-channel open drain  | Programmable     |
| P30                    | 1 bit                        | 1           | CMOS  | Programmable     |
|                        |                              | 2           | N-channel open drain  | Programmable     |
| P70                    | -                            | No          | N-channel open drain  | Programmable     |
| P71 to P73             | -                            | No          | CMOS  | Programmable     |
| S00/LPA0 to S23/LPC7   | -                            | No          | CMOS  | No               |
|                        |                              |             | P-channel open drain  |                  |
|                        |                              |             | N-channel open drain  |                  |
| COM0/LPL0 to COM3/LPL3 | -                            | No          | CMOS  | No               |
|                        |                              |             | P-channel open drain  |                  |
|                        |                              |             | N-channel open drain  |                  |
| XT1                    | -                            | No          | Input only  | No               |
| XT2                    | -                            | No          | 32.768kHz crystal resonator output                                  | No               |
|                        |                              |             | N-channel open drain when selected as a general-purpose output port |                  |

## User Option Table

| Option Name                  | Option to be Applied on            | Mask Version<br>*1 | Flash-ROM<br>Version | Option Selected<br>in Units of | Option Selection     |
|------------------------------|------------------------------------|--------------------|----------------------|--------------------------------|----------------------|
| Port output type             | P00 to P07                         |                    | ○                    | 1 bit                          | CMOS                 |
|                              |                                    |                    |                      |                                | N-channel open drain |
|                              | P10 to P17                         |                    | ○                    | 1 bit                          | CMOS                 |
|                              |                                    |                    |                      |                                | N-channel open drain |
|                              | P30                                |                    | ○                    | 1 bit                          | CMOS                 |
|                              |                                    |                    |                      |                                | N-channel open drain |
| Base timer<br>watchdog timer | Watchdog timer<br>detection period |                    | ○                    | -                              | 1 second             |
|                              |                                    |                    |                      |                                | 2 seconds            |
|                              |                                    |                    |                      |                                | 4 seconds            |
|                              |                                    |                    |                      |                                | 8 seconds            |
| Program start<br>address     | -                                  | *2                 | ○                    | -                              | 00000h               |
|                              |                                    |                    |                      |                                | 07E00h               |

\*1: Mask option selection. No change possible after mask is completed.

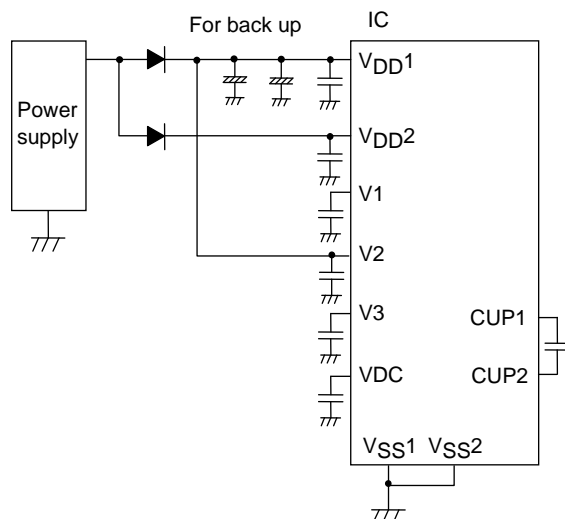
\*2: Program start address of the mask version is 00000h.

\*Note 1: Connect the IC as shown below to minimize noise on the V<sub>DD1</sub>.

Be sure to electrically short the V<sub>SS1</sub> and V<sub>SS2</sub>.

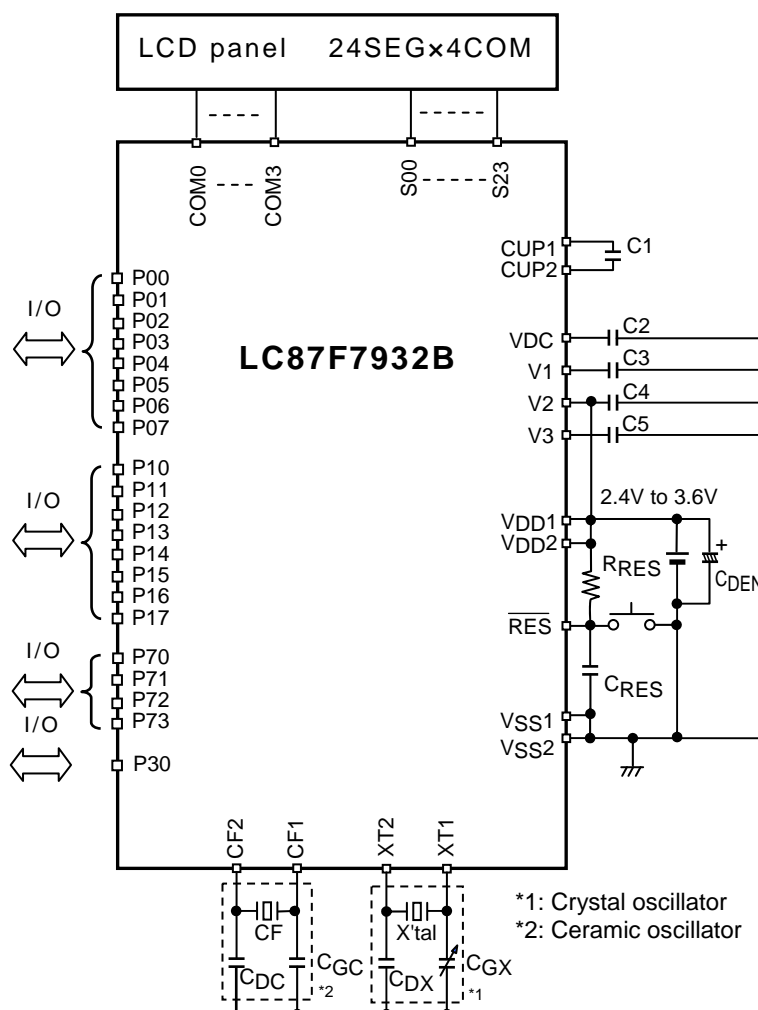
\*Note 2: The power to retain the internal memory is supplied via the V2 pin. V<sub>DD1</sub>, V<sub>DD2</sub> and V2 are used as power supply for ports. If V<sub>DD1</sub> and V<sub>DD2</sub> are not backed up, the output does not go high even if a high level is applied to the port latch. Therefore, if V<sub>DD1</sub> and V<sub>DD2</sub> are not backed up, the high level output becomes unstable in HOLD mode, and the backup time becomes shorter because a through-current flows from V<sub>DD</sub> to GND in the input buffer.

If V<sub>DD1</sub> and V<sub>DD2</sub> are not backed up, configure the program or set up the external circuit so that the output is held at a low level in HOLD mode to prevent an unnecessary through-current from flowing.



# Circuit Example

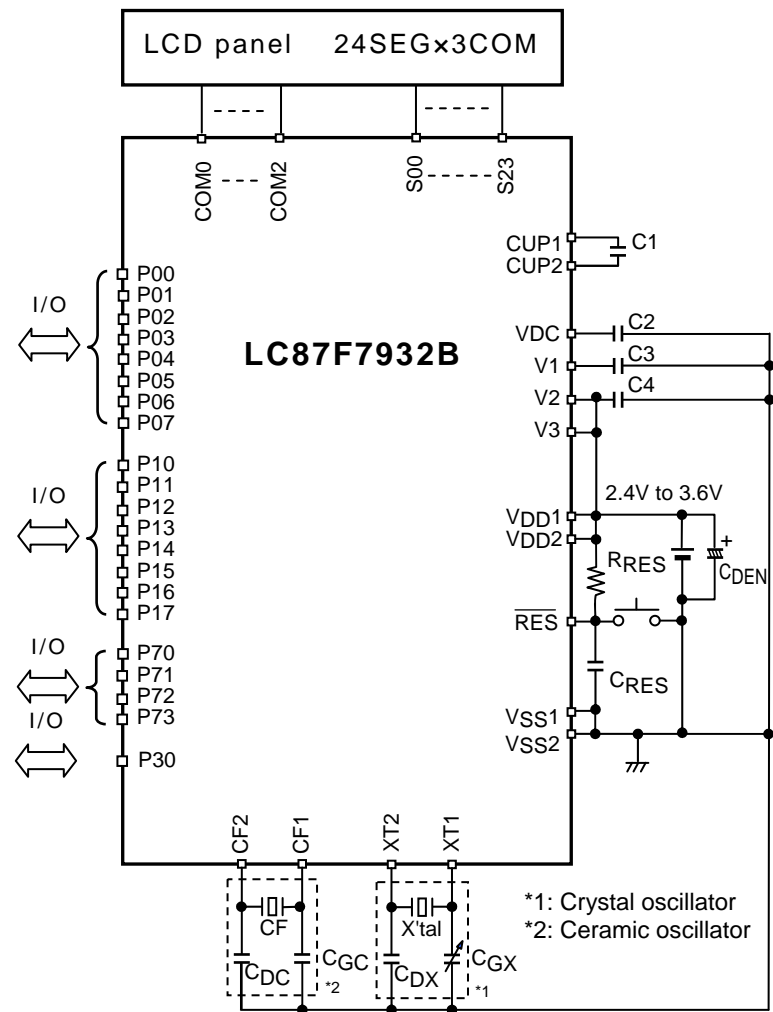
(1)1/3 bias, 1/4 duty



|          |                                       |  |
|----------|---------------------------------------|--|
| X'tal    | Crystal resonator                     | Refer to Page 26<br>(Characteristics of a sample clock oscillator circuit) |
| CGX      | Trimmer capacitor                     |  |
| CDX      | Capacitor for crystal oscillator      |  |
| CF       | Ceramic resonator                     | Refer to Page 26<br>(Characteristics of a sample clock oscillator circuit) |
| CGC      | Capacitor for ceramic oscillator      |  |
| CDC      | Capacitor for ceramic oscillator      |  |
| C1 to C5 | Capacitors                            | 0.1μF (recommended)  |
| CDEN     | Electrolytic capacitor                | For back up  |
| CRES     | Capacitor for $\overline{\text{RES}}$ | Refer to User's manual "Reset Function"                                    |
| RRES     | Resistor for $\overline{\text{RES}}$  |  |

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(2)1/2 bias, 1/3 duty



|          |                                       |  |
|----------|---------------------------------------|--|
| X'tal    | Crystal resonator                     | Refer to Page 26                                       |
| C'GX     | Trimmer capacitor                     | (Characteristics of a sample clock oscillator circuit) |
| C'DX     | Capacitor for crystal oscillator      |  |
| CF       | Ceramic resonator                     | Refer to Page 26                                       |
| C'GC     | Capacitor for ceramic oscillator      | (Characteristics of a sample clock oscillator circuit) |
| C'DC     | Capacitor for ceramic oscillator      |  |
| C1 to C4 | Capacitors                            | 0.1μF (recommended)                                    |
| C'DEN    | Electrolytic capacitor                | For back up  |
| C'RES    | Capacitor for $\overline{\text{RES}}$ | Refer to User's manual "Reset Function"                |
| RRES     | Resistor for $\overline{\text{RES}}$  |  |

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## Absolute Maximum Ratings at Ta=25°C and V<sub>SS</sub>1=V<sub>SS</sub>2=0V

| Parameter                   | Symbol                   | Pin/Remarks                                   | Conditions                             | Specification                                   |      |     |                      |      |
|-----------------------------|--------------------------|---|--|---|------|-----|----------------------|------|
|                             |                          |   |  | V <sub>DD</sub> [V]                             | min  | typ | max                  | unit |
| Maximum supply voltage      | V <sub>DD</sub> max      | V <sub>DD</sub> 1, V <sub>DD</sub> 2, V2      | V <sub>DD</sub> 1=V <sub>DD</sub> 2=V2 |   | -0.3 |     | +4.3                 | V    |
| Supply voltage for LCD      | VLCD                     | V1  |  |   | -0.3 |     | 1/2V <sub>DD</sub>   |      |
|                             |                          | V2  |  |   | -0.3 |     | V <sub>DD</sub>      |      |
|                             |                          | V3  |  |   | -0.3 |     | 2/3V <sub>DD</sub>   |      |
| Input voltage               | V <sub>I</sub>           | XT1, CF1, $\overline{\text{RES}}$             |  |   | -0.3 |     | V <sub>DD</sub> +0.3 |      |
| Input/output voltage        | V <sub>IO</sub> (1)      | Ports 0, 1, 3, 7<br>LPA, LPB, LPC<br>LPL, XT2 |  |   | -0.3 |     | V <sub>DD</sub> +0.3 |      |
| High level output current   | Peak output current      | IOPH(1)                                       | Ports 0, 1                             | • CMOS output selected<br>• Current at each pin |      | -10 |                      | mA   |
|                             |                          | IOPH(2)                                       | Port 3                                 | • CMOS output selected                          |      | -20 |                      |      |
|                             |                          | IOPH(3)                                       | LPA, LPB, LPC<br>LPL                   | • CMOS output selected<br>• Current at each pin |      | -4  |                      |      |
|                             |                          | IOPH(4)                                       | P71 to P73                             | • Current at each pin                           |      | -5  |                      |      |
|                             | Total output current     | ΣIOAH(1)                                      | Port 0                                 | Total of all pins                               |      | -20 |                      |      |
|                             |                          | ΣIOAH(2)                                      | Ports 3, 7                             | Total of all pins                               |      | -30 |                      |      |
|                             |                          | ΣIOAH(3)                                      | Port 1                                 | Total of all pins                               |      | -20 |                      |      |
|                             |                          | ΣIOAH(4)                                      | Ports 1, 3, 7                          | Total of all pins                               |      | -45 |                      |      |
|                             |                          | ΣIOAH(5)                                      | LPA, LPB, LPC,<br>LPL                  | Total of all pins                               |      | -30 |                      |      |
|                             | Low level output current | IOPL(1)                                       | Ports 0, 1                             | Current at each pin                             |      |     | 20                   |      |
|                             |                          | IOPL(2)                                       | Port 3                                 | Current at each pin                             |      |     | 30                   |      |
|                             |                          | IOPL(3)                                       | Port 7                                 | Current at each pin                             |      |     | 10                   |      |
|                             |                          | IOPL(4)                                       | LPA, LPB, LPC,<br>LPL                  | Current at each pin                             |      |     | 6                    |      |
|                             |                          | ΣIOAL(1)                                      | Port 0                                 | Total of all pins                               |      |     | 40                   |      |
|                             |                          | ΣIOAL(2)                                      | Ports 3, 7                             | Total of all pins                               |      |     | 50                   |      |
|                             |                          | ΣIOAL(3)                                      | Port 1                                 | Total of all pins                               |      |     | 40                   |      |
|                             |                          | ΣIOAL(4)                                      | Ports 1, 3, 7                          | Total of all pins                               |      |     | 65                   |      |
|                             |                          | ΣIOAL(5)                                      | LPA, LPB, LPC,<br>LPL                  | Total of all pins                               |      |     | 60                   |      |
| Allowable power dissipation | Pd max                   | QIP64E (14×14)                                | Ta = -40°C to +85°C                    |   |      |     | 267                  | mW   |
|                             |                          | TQFP64J (7×7)                                 |  |   |      |     | 152                  |      |
|                             |                          | SQFP64 (10×10)                                |  |   |      |     | 192                  |      |
| Operating temperature range | T <sub>opr</sub>         |   |  |   | -40  |     | 85                   | °C   |
| Storage temperature range   | T <sub>stg</sub>         |   |  |   | -55  |     | 125                  |      |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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## Allowable Operating Conditions at Ta=-40°C to +85°C, V<sub>SS</sub>1=V<sub>SS</sub>2=0V

| Parameter                                 | Symbol              | Pin/Remarks  | Conditions  | Specification       |                            |        |                            |      |
|---|---------------------|--|---|---------------------|----------------------------|--------|----------------------------|------|
|   |                     |  |   | V <sub>DD</sub> [V] | min                        | typ    | max                        | unit |
| Operating supply voltage<br>(Note 2-1)    | V <sub>DD</sub> (1) | V <sub>DD</sub> 1=V <sub>DD</sub> 2=V2                 | 0.75μs≤tCYC≤200μs<br>Normal mode  |                     | 2.4                        |        | 3.6                        | V    |
| Memory sustaining supply voltage          | V <sub>HD</sub>     | V <sub>DD</sub> 1=V <sub>DD</sub> 2=V2                 | RAM and register contents sustained in HOLD mode.   |                     | 2.2                        |        | 3.6                        |      |
| High level input voltage                  | V <sub>IH</sub> (1) | Ports 0, 3<br>LPA, LPB, LPC, LPL                       | Output disabled   | 2.4 to 3.6          | 0.3V <sub>DD</sub><br>+0.7 |        | V <sub>DD</sub>            |      |
|   | V <sub>IH</sub> (2) | Port 1<br>P71 to 73<br>P70 port input / interrupt side | • Output disabled<br>• When INT1VTS=0 (P71 only)  | 2.4 to 3.6          | 0.3V <sub>DD</sub><br>+0.7 |        | V <sub>DD</sub>            |      |
|   | V <sub>IH</sub> (3) | P71 interrupt side                                     | • Output disabled<br>• When INT1VTS=1   | 2.4 to 3.6          | 0.85V <sub>DD</sub>        |        | V <sub>DD</sub>            |      |
|   | V <sub>IH</sub> (4) | P70 watchdog timer side                                | Output disabled   | 2.4 to 3.6          | 0.9V <sub>DD</sub>         |        | V <sub>DD</sub>            |      |
|   | V <sub>IH</sub> (5) | XT1, XT2, CF1, $\overline{\text{RES}}$                 |   | 2.4 to 3.6          | 0.75V <sub>DD</sub>        |        | V <sub>DD</sub>            |      |
| Low level input voltage                   | V <sub>IL</sub> (1) | Ports 0, 3<br>LPA, LPB, LPC, LPL                       | Output disabled   | 2.4 to 3.6          | V <sub>SS</sub>            |        | 0.2V <sub>DD</sub>         |      |
|   | V <sub>IL</sub> (2) | Port 1<br>P71 to 73<br>P70 port input / interrupt side | • Output disabled<br>• When INT1VTS=0 (P71 only)  | 2.4 to 3.6          | V <sub>SS</sub>            |        | 0.2V <sub>DD</sub>         |      |
|   | V <sub>IL</sub> (3) | P71 interrupt side                                     | • Output disabled<br>• When INT1VTS=1   | 2.4 to 3.6          | V <sub>SS</sub>            |        | 0.45V <sub>DD</sub>        |      |
|   | V <sub>IL</sub> (4) | P70 watchdog timer side                                | Output disabled   | 2.4 to 3.6          | V <sub>SS</sub>            |        | 0.8V <sub>DD</sub><br>-1.0 |      |
|   | V <sub>IL</sub> (5) | XT1, XT2, CF1, $\overline{\text{RES}}$                 |   | 2.4 to 3.6          | V <sub>SS</sub>            |        | 0.25V <sub>DD</sub>        |      |
| Instruction cycle time<br>(Note 2-2)      | tCYC                |  |   | 2.4 to 3.6          |                            |        | 200                        | μs   |
| External system clock frequency           | FEXCF(1)            | CF1  | • CF2 pin open<br>• System clock frequency division ratio = 1/1<br>• External system clock duty = 50±5% | 2.4 to 3.6          | 0.1                        |        | 4                          | MHz  |
|   |                     |  | • CF2 pin open<br>• System clock frequency division ratio = 1/2   | 2.4 to 3.6          | 0.2                        |        | 8                          |      |
| Oscillation frequency range<br>(Note 2-3) | FmCF(1)             | CF1, CF2   | • 4MHz ceramic oscillation<br>• See Fig. 1.   | 2.4 to 3.6          |                            | 4      |                            | MHz  |
|   | FmRC(1)             |  | Internal high-speed RC oscillation  | 2.4 to 3.6          | 250                        | 500    | 750                        | kHz  |
|   | FsRC(1)             |  | Internal low-speed RC oscillation   | 2.4 to 3.6          | 25                         | 50     | 75                         |      |
|   | FsX'tal             | XT1, XT2   | • 32.768kHz crystal oscillation<br>• See Fig. 2.  | 2.4 to 3.6          |                            | 32.768 |                            |      |
| VMRC oscillation usable range             | OpVMRC(1)           |  | When VMSL4M=0   | 3.0 to 3.6          | 8                          | 10     | 12                         | MHz  |
|   | OpVMRC(2)           |  | When VMSL4M=1   | 2.4 to 3.6          | 3.5                        | 4      | 4.5                        |      |
| VMRC oscillation adjustment range         | VmADJ(1)            |  | Each step of VMRAJn (Wide range)  | 2.4 to 3.6          | 8                          | 24     | 64                         | %    |
|   | VmADJ(2)            |  | Each step of VMFAJn (Small range)   | 2.4 to 3.6          | 1                          | 4      | 8                          |      |

Note 2-1: V<sub>DD</sub> must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

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## Electrical Characteristics at Ta=-40°C to +85°C, V<sub>SS1</sub>=V<sub>SS2</sub>=0V

| Parameter                    | Symbol               | Pin/Remarks                              | Conditions   | V <sub>DD</sub> [V] | Specification        |                    |      |      |
|------------------------------|----------------------|--|--|---------------------|----------------------|--------------------|------|------|
|                              |                      |  |  |                     | min                  | typ                | max  | unit |
| High level input current     | I <sub>IH</sub> (1)  | Ports 0, 1, 3, 7<br>LPA, LPB, LPC<br>LPL | • Output disabled<br>• Pull-up resistor off<br>• V <sub>IN</sub> =V <sub>DD</sub><br>(Including output Tr's off leakage current) | 2.4 to 3.6          |                      |                    | 1    | μA   |
|                              | I <sub>IH</sub> (2)  | $\overline{\text{RES}}$                  | V <sub>IN</sub> =V <sub>DD</sub>   | 2.4 to 3.6          |                      |                    | 1    |      |
|                              | I <sub>IH</sub> (3)  | XT1, XT2                                 | • Input port specification<br>• V <sub>IN</sub> =V <sub>DD</sub>   | 2.4 to 3.6          |                      |                    | 1    |      |
|                              | I <sub>IH</sub> (4)  | CF1                                      | V <sub>IN</sub> =V <sub>DD</sub>   | 2.4 to 3.6          |                      |                    | 15   |      |
| Low level input current      | I <sub>IL</sub> (1)  | Ports 0, 1, 3, 7<br>LPA, LPB, LPC<br>LPL | • Output disabled<br>• Pull-up resistor off<br>• V <sub>IN</sub> =V <sub>SS</sub><br>(Including output Tr's off leakage current) | 2.4 to 3.6          | -1                   |                    |      | μA   |
|                              | I <sub>IL</sub> (2)  | $\overline{\text{RES}}$                  | V <sub>IN</sub> =V <sub>SS</sub>   | 2.4 to 3.6          | -1                   |                    |      |      |
|                              | I <sub>IL</sub> (3)  | XT1, XT2                                 | • Input port specification<br>• V <sub>IN</sub> =V <sub>SS</sub>   | 2.4 to 3.6          | -1                   |                    |      |      |
|                              | I <sub>IL</sub> (4)  | CF1                                      | V <sub>IN</sub> =V <sub>SS</sub>   | 2.4 to 3.6          | -15                  |                    |      |      |
| High level output voltage    | V <sub>OH</sub> (1)  | CMOS output ports<br>0, 1                | I <sub>OH</sub> =-0.4mA  | 3.0 to 3.6          | V <sub>DD</sub> -0.4 |                    |      | V    |
|                              | V <sub>OH</sub> (2)  |  | I <sub>OH</sub> =-0.2mA  | 2.4 to 3.6          | V <sub>DD</sub> -0.4 |                    |      |      |
|                              | V <sub>OH</sub> (3)  | CMOS output port 3                       | I <sub>OH</sub> =-1.6mA  | 3.0 to 3.6          | V <sub>DD</sub> -0.4 |                    |      |      |
|                              | V <sub>OH</sub> (4)  |  | I <sub>OH</sub> =-1mA  | 2.4 to 3.6          | V <sub>DD</sub> -0.4 |                    |      |      |
|                              | V <sub>OH</sub> (5)  | P71 to 73                                | I <sub>OH</sub> =-0.4mA  | 3.0 to 3.6          | V <sub>DD</sub> -0.4 |                    |      |      |
|                              | V <sub>OH</sub> (6)  |  | I <sub>OH</sub> =-0.2mA  | 2.4 to 3.6          | V <sub>DD</sub> -0.4 |                    |      |      |
|                              | V <sub>OH</sub> (7)  | LPA, LPB, LPC<br>LPL                     | I <sub>OH</sub> =-0.1mA  | 2.4 to 3.6          | V <sub>DD</sub> -0.4 |                    |      |      |
| Low level output voltage     | V <sub>OL</sub> (1)  | Ports 0, 1                               | I <sub>OL</sub> =1.6mA   | 3.0 to 3.6          |                      |                    | 0.4  | V    |
|                              | V <sub>OL</sub> (2)  |  | I <sub>OL</sub> =1mA   | 2.4 to 3.6          |                      |                    | 0.4  |      |
|                              | V <sub>OL</sub> (3)  | Port 3                                   | I <sub>OL</sub> =5mA   | 3.0 to 3.6          |                      |                    | 0.4  |      |
|                              | V <sub>OL</sub> (4)  |  | I <sub>OL</sub> =2.5mA   | 2.4 to 3.6          |                      |                    | 0.4  |      |
|                              | V <sub>OL</sub> (5)  | Port 7<br>XT2                            | I <sub>OL</sub> =1.6mA   | 3.0 to 3.6          |                      |                    | 0.4  |      |
|                              | V <sub>OL</sub> (6)  |  | I <sub>OL</sub> =1mA   | 2.4 to 3.6          |                      |                    | 0.4  |      |
|                              | V <sub>OL</sub> (7)  | LPA, LPB, LPC<br>LPL                     | I <sub>OL</sub> =0.1mA   | 2.4 to 3.6          |                      |                    | 0.4  |      |
| LCD output voltage deviation | VODLS                | S00 to S31                               | • I <sub>O</sub> =0mA<br>• V1, V2, V3<br>LCD level output<br>• See Fig. 8.   | 2.4 to 3.6          | 0                    |                    | ±0.2 | V    |
|                              | VODLC                | COM0 to COM3                             | • I <sub>O</sub> =0mA<br>• V1, V2, V3<br>LCD level output<br>• See Fig. 8.   | 2.4 to 3.6          | 0                    |                    | ±0.2 |      |
| Pull-up resistance           | R <sub>pu</sub> (1)  | Ports 0, 1, 3, 7                         | V <sub>OH</sub> =0.9V <sub>DD</sub>  | 2.4 to 3.6          | 18                   | 50                 | 150  | kΩ   |
| Hysteresis voltage           | V <sub>HYS</sub> (1) | Ports 1, 7<br>$\overline{\text{RES}}$    |  | 2.4 to 3.6          |                      | 0.1V <sub>DD</sub> |      | V    |
| Pin capacitance              | CP                   | All pins                                 | • For pins other than that under test: V <sub>IN</sub> =V <sub>SS</sub><br>• f=1MHz<br>• Ta=25°C                                 | 2.4 to 3.6          |                      | 10                 |      | pF   |

**Serial I/O Characteristics** at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0V

**1. SIO0 Serial I/O Characteristics (Note 4-1-1)**

| Parameter     |                 |                        | Symbol   | Pin/Remarks  | Conditions   | V <sub>DD</sub> [V] | Specification      |                             |     |                    |
|---------------|-----------------|------------------------|--|--|--|---------------------|--------------------|-----------------------------|-----|--------------------|
|               |                 |                        |  |  |  |                     | min                | typ                         | max | unit               |
| Serial clock  | Input clock     | Frequency              | tSCK(1)  | SCK0(P12)  | See Fig. 6.  | 2.4 to 3.6          | 2                  |                             |     | tCYC               |
|               |                 | Low level pulse width  | tSCKL(1)   |  | 1  |                     |                    |                             |     |                    |
|               |                 | High level pulse width | tSCKH(1)   | 1  |  |                     |                    |                             |     |                    |
|               |                 | tSCKHA(1)              | <ul style="list-style-type: none"><li>Continuous data transmission/reception mode</li><li>See Fig. 6.</li><li>(Note 4-1-2)</li></ul>         | 4  |  |                     |                    |                             |     |                    |
|               | Output clock    | Frequency              | tSCK(2)  | SCK0(P12)  | <ul style="list-style-type: none"><li>CMOS output selected</li><li>See Fig. 6.</li></ul>                         | 2.4 to 3.6          | 4/3                |                             |     | tSCK               |
|               |                 | Low level pulse width  | tSCKL(2)   |  | 1/2  |                     |                    |                             |     |                    |
|               |                 | High level pulse width | tSCKH(2)   | 1/2  |  |                     | tCYC               |                             |     |                    |
|               |                 | tSCKHA(2)              | <ul style="list-style-type: none"><li>Continuous data transmission/reception mode</li><li>CMOS output selected</li><li>See Fig. 6.</li></ul> | tSCKH(2)<br>+2tCYC   |  |                     |                    | tSCKH(2)<br>+(10/3)<br>tCYC |     |                    |
| Serial input  | Data setup time | tsDI(1)                | SB0(P11),<br>SIO(P11)  | <ul style="list-style-type: none"><li>Must be specified with respect to the rising edge of SIOCLK.</li><li>See Fig. 6.</li></ul> | 2.4 to 3.6   | 0.03                |                    |                             | μs  |                    |
|               | Data hold time  | thDI(1)                |  | 0.03   |  |                     |                    |                             |     |                    |
| Serial output | Input clock     | Output delay time      | tdDO(1)  | SO0(P10),<br>SB0(P11)  | <ul style="list-style-type: none"><li>Continuous data transmission/reception mode</li><li>(Note 4-1-3)</li></ul> | 2.4 to 3.6          |                    |                             |     | (1/3)tCYC<br>+0.05 |
|               |                 | tdDO(2)                | <ul style="list-style-type: none"><li>Synchronous 8-bit mode</li><li>(Note 4-1-3)</li></ul>  |  |  |                     |                    | 1tCYC<br>+0.05              |     |                    |
|               | Output clock    | tdDO(3)                | (Note 4-1-3)   |  |  |                     | (1/3)tCYC<br>+0.05 |                             |     |                    |

Note 4-1-1: These specifications are theoretical values. Be sure to add margin depending on its use.

Note 4-1-2: In an application where the serial clock input is to be used in continuous data transmission/reception mode, the time from SIORUN being set when serial clock is high to the falling edge of the first serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to the falling edge of SIOCLK. Must be specified as the time up to the beginning of output state change in open drain output mode. See Fig. 6.

## 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

| Parameter     |                   | Symbol                 | Pin/Remarks        | Conditions  | V <sub>DD</sub> [V] | Specification |     |                  |      |
|---------------|-------------------|------------------------|--------------------|---|---------------------|---------------|-----|------------------|------|
|               |                   |                        |                    |   |                     | min           | typ | max              | unit |
| Serial clock  | Input clock       | Frequency              | SCK1(P15)          | See Fig. 6.   | 2.4 to 3.6          | 2             |     |                  | tCYC |
|               |                   | Low level pulse width  |                    |   |                     | 1             |     |                  |      |
|               |                   | High level pulse width |                    |   |                     | 1             |     |                  |      |
|               | Output clock      | Frequency              | SCK1(P15)          | <ul style="list-style-type: none"> <li>CMOS output selected</li> <li>See Fig. 6.</li> </ul>   | 2.4 to 3.6          | 2             |     |                  | tSCK |
|               |                   | Low level pulse width  |                    |   |                     | 1/2           |     |                  |      |
|               |                   | High level pulse width |                    |   |                     | 1/2           |     |                  |      |
| Serial input  | Data setup time   | tsDI(2)                | SB1(P14), SI1(P14) | <ul style="list-style-type: none"> <li>Must be specified with respect to the rising edge of SIOCLK.</li> <li>See Fig. 6.</li> </ul>   | 2.4 to 3.6          | 0.03          |     |                  | μs   |
|               | Data hold time    | thDI(2)                |                    |   |                     | 0.03          |     |                  |      |
| Serial output | Output delay time | tdDO(4)                | SO1(P13), SB1(P14) | <ul style="list-style-type: none"> <li>Must be specified with respect to the falling edge of SIOCLK.</li> <li>Must be specified as the time up to the beginning of output state change in open drain output mode.</li> <li>See Fig. 6.</li> </ul> | 2.4 to 3.6          |               |     | (1/3)tCYC + 0.05 |      |

Note 4-2-1: These specifications are theoretical values. Be sure to add margin depending on its use.

### Pulse Input Conditions at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0V

| Parameter                  | Symbol             | Pin/Remarks  | Conditions   | V <sub>DD</sub> [V] | Specification |     |     |      |
|----------------------------|--------------------|--|--|---------------------|---------------|-----|-----|------|
|                            |                    |  |  |                     | min           | typ | max | unit |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P70), INT1(P71), INT2(P72)                    | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul> | 2.4 to 3.6          | 1             |     |     | tCYC |
|                            | tPIH(2)<br>tPIL(2) | INT3(P73) when noise filter time constant is 1/1   | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul> | 2.4 to 3.6          | 2             |     |     |      |
|                            | tPIH(3)<br>tPIL(3) | INT3(P73) when noise filter time constant is 1/32  | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul> | 2.4 to 3.6          | 64            |     |     |      |
|                            | tPIH(4)<br>tPIL(4) | INT3(P73) when noise filter time constant is 1/128 | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timer 0 are enabled.</li> </ul> | 2.4 to 3.6          | 256           |     |     |      |
|                            | tPIL(5)            | RES  | Resetting is enabled.  | 2.4 to 3.6          | 200           |     |     | μs   |

**AD Converter Characteristics** at  $V_{SS1} = V_{SS2} = 0V$

<12-bit AD Conversion Mode at  $T_a = -40^{\circ}C$  to  $+85^{\circ}C$ >

| Parameter                  | Symbol | Pin/Remarks   | Conditions  | Specification |          |     |          |         |
|----------------------------|--------|---|---|---------------|----------|-----|----------|---------|
|                            |        |   |   | $V_{DD}[V]$   | min      | typ | max      | unit    |
| Resolution                 | N      | AN0 (P00) to<br>AN4 (P04),<br>AN5 (P70) to<br>AN6 (P71) |   | 3.0 to 3.6    |          | 12  |          | bit     |
| Absolute accuracy          | ET     |   | (Note 6-1)  | 3.0 to 3.6    |          |     | $\pm 16$ | LSB     |
| Conversion time            | TCAD   |   | • See conversion time calculation formulas.<br>(Note 6-2) | 3.0 to 3.6    | 64       |     | 115      | $\mu s$ |
| Analog input voltage range | VAIN   |   |   | 3.0 to 3.6    | $V_{SS}$ |     | $V_{DD}$ | V       |
| Analog port input current  | IAINH  |   | $VAIN = V_{DD}$   | 3.0 to 3.6    |          |     | 1        | $\mu A$ |
|                            | IAINL  |   | $VAIN = V_{SS}$   | 3.0 to 3.6    | -1       |     |          |         |

<8-bit AD Conversion Mode at  $T_a = -40^{\circ}C$  to  $+85^{\circ}C$ >

| Parameter                  | Symbol | Pin/Remarks   | Conditions  | Specification |          |     |           |         |
|----------------------------|--------|---|---|---------------|----------|-----|-----------|---------|
|                            |        |   |   | $V_{DD}[V]$   | min      | typ | max       | Unit    |
| Resolution                 | N      | AN0(P00) to<br>AN4(P04),<br>AN5(P70) to<br>AN6(P71) |   | 3.0 to 3.6    |          | 8   |           | bit     |
| Absolute accuracy          | ET     |   | (Note 6-1)  | 3.0 to 3.6    |          |     | $\pm 1.5$ | LSB     |
| Conversion time            | TCAD   |   | • See conversion time calculation formulas.<br>(Note 6-2) | 3.0 to 3.6    | 40       |     | 90        | $\mu s$ |
| Analog input voltage range | VAIN   |   |   | 3.0 to 3.6    | $V_{SS}$ |     | $V_{DD}$  | V       |
| Analog port input current  | IAINH  |   | $VAIN = V_{DD}$   | 3.0 to 3.6    |          |     | 1         | $\mu A$ |
|                            | IAINL  |   | $VAIN = V_{SS}$   | 3.0 to 3.6    | -1       |     |           |         |

**Conversion Time Calculation Formulas:**

12-bit AD conversion mode:  $TCAD$  (conversion time) =  $((52 / (\text{AD division ratio})) + 2) \times (1/3) \times t_{CYC}$

8-bit AD conversion mode:  $TCAD$  (conversion time) =  $((32 / (\text{AD division ratio})) + 2) \times (1/3) \times t_{CYC}$

<Recommended Operating Conditions>

| External Oscillator (FmCF) | Supply Voltage Range ( $V_{DD}$ ) | System Clock Division Ratio (SYSDIV) | Cycle Time ( $t_{CYC}$ ) | AD Frequency Division Ratio (ADDIV) | Conversion Time (TCAD) |              |
|----------------------------|-----------------------------------|--------------------------------------|--------------------------|-------------------------------------|------------------------|--------------|
|                            |                                   |                                      |                          |                                     | 12-bit AD              | 8-bit AD     |
| CF-4MHz                    | 3.0V to 3.6V                      | 1/1                                  | 750ns                    | 1/8                                 | 104.5 $\mu s$          | 64.5 $\mu s$ |

Note 6-1: The quantization error ( $\pm 1/2LSB$ ) is excluded from the absolute accuracy. The absolute accuracy is measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process is executed until the time the conversion result register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is doubled in the following cases:

- The first AD conversion is performed in the 12 bits AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8 bits to 12 bits conversion mode.

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## Consumption Current Characteristics at Ta = -40°C to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0V

| Parameter   | Symbol   | Pin/Remarks  | Conditions  | Specification       |     |     |     |      |
|---|----------|--|---|---------------------|-----|-----|-----|------|
|   |          |  |   | V <sub>DD</sub> [V] | min | typ | max | unit |
| Current consumption in normal operating mode (Note 7-1) | IDDOP(1) | V <sub>DD1</sub> =V <sub>DD2</sub> =V <sub>2</sub> | <ul style="list-style-type: none"> <li>FmCF=4MHz ceramic oscillation</li> <li>FsX'tal=32.768kHz crystal oscillation</li> <li>System clock set to 4MHz side</li> <li>Internal RC oscillation stopped</li> <li>VMRC oscillation stopped</li> <li>1/1 frequency division ratio</li> </ul>  | 2.4 to 3.6          |     | 2.0 | 4.2 | mA   |
|   | IDDOP(2) |  | <ul style="list-style-type: none"> <li>FmCF=0Hz (Oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation</li> <li>System clock set to high-speed internal RC oscillation</li> <li>VMRC oscillation stopped</li> <li>1/1 frequency division ratio</li> </ul>   | 2.4 to 3.6          |     | 250 | 900 | μA   |
|   | IDDOP(3) |  | <ul style="list-style-type: none"> <li>FmCF=0Hz (Oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation</li> <li>System clock set to low-speed internal RC oscillation</li> <li>VMRC oscillation stopped</li> <li>1/1 frequency division ratio</li> </ul>  | 2.4 to 3.6          |     | 30  | 120 |      |
|   | IDDOP(4) |  | <ul style="list-style-type: none"> <li>FmCF=0Hz (Oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation</li> <li>Internal RC oscillation stopped</li> <li>System clock set to 4MHz VMRC oscillation</li> <li>1/1 frequency division ratio</li> </ul>   | 2.4 to 3.6          |     | 2.0 | 5.4 | mA   |
|   | IDDOP(5) |  | <ul style="list-style-type: none"> <li>FmCF=0Hz (Oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation</li> <li>Internal RC oscillation stopped</li> <li>System clock set to 500kHz VMRC oscillation</li> <li>1/1 frequency division ratio</li> </ul>   | 2.4 to 3.6          |     | 250 | 900 | μA   |
|   | IDDOP(6) |  | <ul style="list-style-type: none"> <li>FmCF=0Hz (Oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation</li> <li>System clock set to 32.768kHz side</li> <li>Internal RC oscillation stopped</li> <li>VMRC oscillation stopped</li> <li>1/1 frequency division ratio</li> <li>Normal XT amp mode</li> </ul>          | 2.4 to 3.6          |     | 20  | 86  |      |
|   | IDDOP(7) |  | <ul style="list-style-type: none"> <li>FmCF=0Hz (Oscillation stopped)</li> <li>FsX'tal=32.768kHz crystal oscillation</li> <li>System clock set to 32.768kHz side</li> <li>Internal RC oscillation stopped</li> <li>VMRC oscillation stopped</li> <li>1/1 frequency division ratio</li> <li>Low consumption XT amp mode</li> </ul> | 2.4 to 3.6          |     | 15  | 72  |      |

Note 7-1: The consumption current value does not include current that flows into the output transistors and internal pull-up resistors.

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| Parameter                                   | Symbol     | Pin/Remarks  | Conditions  | Specification       |     |      |      |      |
|---|------------|--|---|---------------------|-----|------|------|------|
|   |            |  |   | V <sub>DD</sub> [V] | min | typ  | max  | unit |
| Current consumption in HALT mode (Note 7-1) | IDDHALT(1) | V <sub>DD1</sub> =V <sub>DD2</sub> =V <sub>2</sub> | HALT mode<br>• FmCF=4MHz ceramic oscillation<br>• FsX'tal=32.768kHz crystal oscillation<br>• System clock set to 4MHz side<br>• Internal RC oscillation stopped<br>• VMRC oscillation stopped<br>• 1/1 frequency division ratio   | 2.4 to 3.6          |     | 0.55 | 1.55 | mA   |
|   | IDDHALT(2) |  | HALT mode<br>• FmCF=0Hz (Oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation<br>• System clock set to high-speed internal RC oscillation<br>• VMRC oscillation stopped<br>• 1/1 frequency division ratio  | 2.4 to 3.6          |     | 68   | 280  | μA   |
|   | IDDHALT(3) |  | HALT mode<br>• FmCF=0Hz (Oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation<br>• System clock set to low-speed internal RC oscillation<br>• VMRC oscillation stopped<br>• 1/1 frequency division ratio   | 2.4 to 3.6          |     | 7    | 85   |      |
|   | IDDHALT(4) |  | HALT mode<br>• FmCF=0Hz (Oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation<br>• Internal RC oscillation stopped<br>• System clock set to 4MHz VMRC oscillation<br>• 1/1 frequency division ratio  | 2.4 to 3.6          |     | 650  | 1460 |      |
|   | IDDHALT(5) |  | HALT mode<br>• FmCF=0Hz (Oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation<br>• Internal RC oscillation stopped<br>• System clock set to VMRC oscillation (500kHz)<br>• 1/1 frequency division ratio  | 2.4 to 3.6          |     | 68   | 280  |      |
|   | IDDHALT(6) |  | HALT mode<br>• FmCF=0Hz (Oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation<br>• System clock set to 32.768kHz side<br>• Internal RC oscillation stopped.<br>• VMRC oscillation stopped<br>• 1/1 frequency division ratio<br>• Normal XT amp mode          | 2.4 to 3.6          |     | 8    | 70   |      |
|   | IDDHALT(7) |  | HALT mode<br>• FmCF=0Hz (Oscillation stopped)<br>• FsX'tal=32.768kHz crystal oscillation<br>• System clock set to 32.768kHz side<br>• Internal RC oscillation stopped.<br>• VMRC oscillation stopped<br>• 1/1 frequency division ratio<br>• Low consumption XT amp mode | 2.4 to 3.6          |     | 4    | 50   |      |

Note 7-1: The consumption current value does not include current that flows into the output transistors and internal pull-up resistors.

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| Parameter  | Symbol     | Pin/Remarks  | Conditions   | Specification       |     |      |     |      |
|--|------------|--|--|---------------------|-----|------|-----|------|
|  |            |  |  | V <sub>DD</sub> [V] | min | typ  | max | unit |
| Current consumption in HOLD mode                   | IDDHOLD(1) | V <sub>DD1</sub> =V <sub>DD2</sub> =V <sub>2</sub> | HOLD mode<br>• CF1=V <sub>DD</sub> or open<br>(When using external clock)  | 2.4 to 3.6          |     | 0.05 | 30  | μA   |
| Current consumption in time-of-day clock HOLD mode | IDDHOLD(2) | V <sub>DD1</sub> =V <sub>DD2</sub> =V <sub>2</sub> | Time-of-day clock HOLD mode<br>• CF1=V <sub>DD</sub> or open<br>(When using external clock)<br>• FsX'tal=32.768kHz crystal oscillation<br>• 1/1 frequency division ratio<br>• LCD display off<br>• Normal XT amp mode          | 2.4 to 3.6          |     | 6.5  | 67  |      |
|  | IDDHOLD(3) |  | Time-of-day clock HOLD mode<br>• CF1=V <sub>DD</sub> or open<br>(When using external clock)<br>• FsX'tal=32.768kHz crystal oscillation<br>• 1/1 frequency division ratio<br>• LCD display off<br>• Low consumption XT amp mode | 2.4 to 3.6          |     | 0.45 | 46  |      |
|  | IDDHOLD(4) |  | Time-of-day clock HOLD mode<br>• CF1=V <sub>DD</sub> or open<br>(When using external clock)<br>• FsX'tal=low-speed RC oscillation<br>• 1/1 frequency division ratio<br>• LCD display off                                       | 2.4 to 3.6          |     | 1.5  | 70  |      |



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## F-ROM Programming Characteristics at $T_a = +10^{\circ}\text{C}$ to $+55^{\circ}\text{C}$ , $V_{SS1} = V_{SS2} = 0\text{V}$

| Parameter                   | Symbol                | Pin/Remarks | Conditions   | $V_{DD}[\text{V}]$ | Specification |     |     |      |
|-----------------------------|-----------------------|-------------|--|--------------------|---------------|-----|-----|------|
|                             |                       |             |  |                    | min           | typ | max | unit |
| Onboard programming current | I <sub>DDFW</sub> (1) | $V_{DD1}$   | • Excluding power dissipation in the microcontroller block | 3.0 to 5.5         |               | 5   | 10  | mA   |
| Programming time            | t <sub>FW</sub> (1)   |             | • Erasing operation  | 3.0 to 5.5         |               | 20  | 30  | ms   |
|                             | t <sub>FW</sub> (2)   |             | • Programming operation                                    |                    |               | 45  | 60  | μs   |

## UART (Full Duplex) Operating Conditions at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{SS1} = V_{SS2} = 0\text{V}$

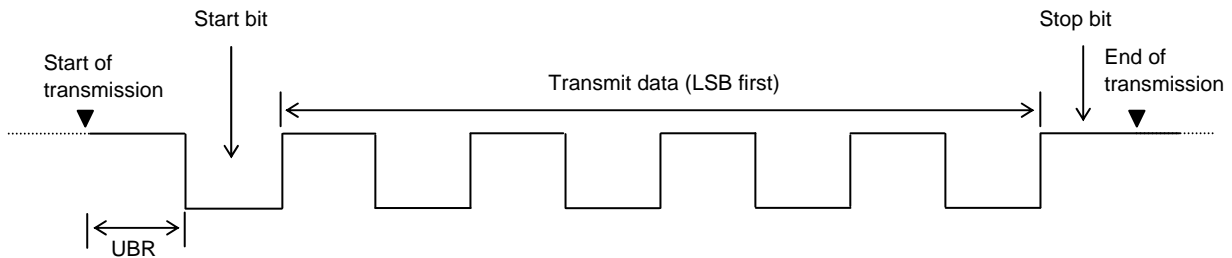
| Parameter     | Symbol | Pin/Remarks             | Conditions | $V_{DD}[\text{V}]$ | Specification |     |        |      |
|---------------|--------|-------------------------|------------|--------------------|---------------|-----|--------|------|
|               |        |                         |            |                    | min           | typ | max    | unit |
| Transfer rate | UBR    | UTX (P00),<br>URX (P01) |            | 2.4 to 3.6         | 16/3          |     | 8192/3 | tCYC |

Data length: 7/8/9 bits (LSB first)

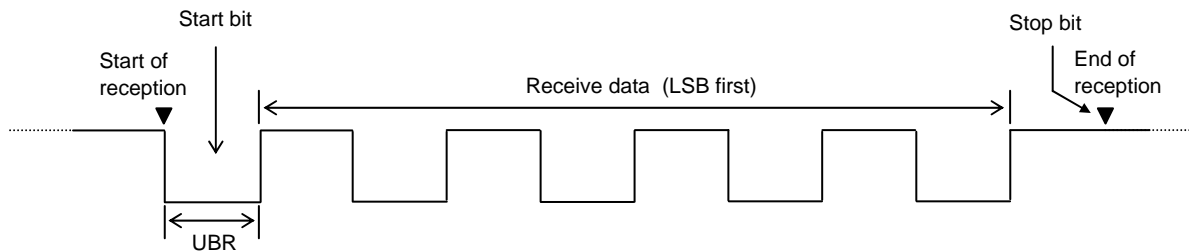
Stop bits: 1 bit (2 bits in continuous data transmission)

Parity bits: None

### Example of 8-bit Data Transmission Mode Processing (Transmit Data=55H)



### Example of 8-bit Data Reception Mode Processing (Receive Data=55H)



## Characteristics of a Sample Main System Clock Oscillator Circuit

Given below are the characteristics of a sample main system clock oscillator circuit, which are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with normal and stable oscillation confirmed by the resonator vendor.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

| Nominal Frequency | Vendor Name | Resonator Name  | Circuit Constant |         |         |         | Operating Voltage Range [V] | Oscillation Stabilization Time |          | Remarks         |
|-------------------|-------------|-----------------|------------------|---------|---------|---------|-----------------------------|--------------------------------|----------|-----------------|
|                   |             |                 | C1 [pF]          | C2 [pF] | Rf1 [Ω] | Rd1 [Ω] |                             | typ [ms]                       | max [ms] |                 |
| 4.00MHz           | Murata      | CSTCR4M00G53-R0 | (15)             | (15)    | Open    | 1k      | 2.4 to 3.6                  | 0.03                           | 0.15     | Internal C1, C2 |
|                   |             | CSTLS4M00G53-B0 | (15)             | (15)    | Open    | 1k      | 2.4 to 3.6                  | 0.02                           | 0.15     |                 |

The oscillation stabilization time is the period required for the resonator to stabilize in the following situations.

(See Figure 4)

- After  $V_{DD}$  goes above the operating voltage lower limit until the oscillation is stabilized.
- After the instruction for starting the main clock oscillation circuit is executed until the oscillation is stabilized.
- After HOLD mode is released until the oscillation is stabilized.
- After HOLD mode is released and oscillation is started with CFSTOP (OCR register, bit0) set to 0 until the oscillation is stabilized.

## Characteristics of a Sample Sub-system Clock Oscillator Circuit

Given below are the characteristics of a sample sub-system clock oscillator circuit, which are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with normal and stable oscillation confirmed by the resonator vendor. (Different evaluation boards are used for Tables 2 and 3.)

Table 2 Characteristics of a Sample Sub-system Clock Oscillator Circuit with a Crystal Resonator 1

| Nominal Frequency | Vendor Name   | Resonator Name | Circuit Constant |         |         |         | Operating Voltage Range [V] | Oscillation Stabilization Time |         | Remarks                      |
|-------------------|---------------|----------------|------------------|---------|---------|---------|-----------------------------|--------------------------------|---------|------------------------------|
|                   |               |                | C3 [pF]          | C4 [pF] | Rf2 [Ω] | Rd2 [Ω] |                             | typ [s]                        | max [s] |                              |
| 32.768KHz         | Epson Toyocom | MC-306         | 9                | 9       | Open    | 330k    | 2.4 to 3.6                  | 1                              | 3       | CL=7.0pF Normal amp          |
|                   |               |                | 3                | 3       | Open    | 0       | 2.4 to 3.6                  | 2                              | 6       | CL=7.0pF Low consumption amp |

Table 3 Characteristics of a Sample Sub-system Clock Oscillator Circuit with a Crystal Resonator 2 (\*5)

| Nominal Frequency | Vendor Name            | Resonator Name | Circuit Constant |         |         |         | Operating Voltage Range [V] | Oscillation Stabilization Time |         | Remarks                           |
|-------------------|------------------------|----------------|------------------|---------|---------|---------|-----------------------------|--------------------------------|---------|-----------------------------------|
|                   |                        |                | C3 [pF]          | C4 [pF] | Rf2 [Ω] | Rd2 [Ω] |                             | typ [s]                        | max [s] |                                   |
| 32.768kHz (*1)    | Seiko Instruments (*2) | SSP-T7-F       | 22               | 22      | Open    | 820k    | 2.4 to 3.6                  | 1.8                            | 3       | CL=12.5pF (*3) Normal amp         |
|                   |                        | VT-200-F       |                  |         |         |         |                             |                                |         |                                   |
|                   |                        | SSP-T7-FL      | 7                | 6       | Open    | 0       | 2.4 to 3.6                  | 0.9                            | 3       | CL=6.0pF (*4) Low consumption amp |
|                   |                        | VT-200-FL      |                  |         |         |         |                             |                                |         |                                   |

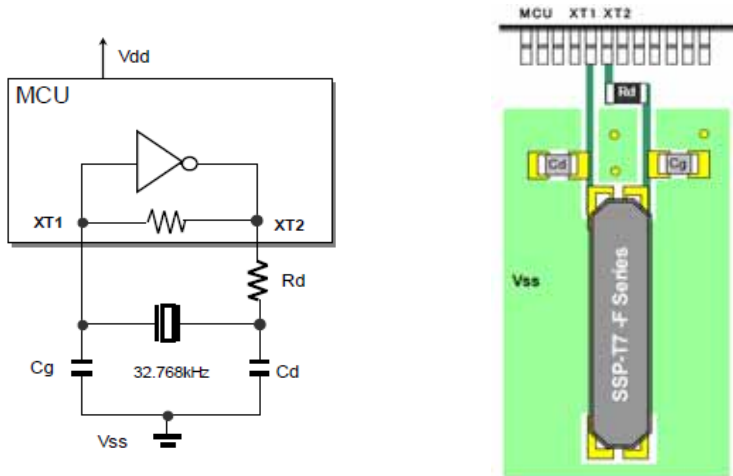
(\*1) Normal XT amplifier mode (\*3) or low consumption amplifier mode (\*4) should be selected for the sub-system clock oscillator circuit.

(\*2) Contact Seiko Instruments, Inc., (<http://www.sii-crystal.com>) for further information about the use of the resonator.

(\*3) When considering the use of normal XT amplifier mode, use a resonator that has a large load capacitance.

(\*4) When considering the use of low consumption XT amplifier mode, use a resonator that has a small load capacitance. The applicable CL value of 6.0pF makes it possible to achieve a high time accuracy for the subclock oscillator as well as high-speed oscillation startup and low power dissipation. In addition to this value, 7.0pF and 9.0pF also fall within the applicable CL value range.

(\*5) A sample PCB trace pattern for a Seiko Instrument resonator is shown below.



(Note 1) The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations (see Figure 4):

- After the instruction for starting the subclock oscillator circuit is executed until the oscillation is stabilized.
- After HOLD mode is released and oscillation is started with EXTOSC (OCR register, bit 6) set to 1 until the oscillation is stabilized.

(Note 2) The circuit constants shown are the reference values that are provided by the resonator vendor for evaluation. To make final verification of the oscillation characteristics on production boards, call the resonator vendor for evaluation on printed circuit boards.

(Note 3) When using an oscillator circuit, observe the following wiring precautions to avoid the possible adverse influence of wiring capacitance, especially in low consumption XT amplifier mode:

- Place the components that are involved in oscillation as close to the resonator as possible with the shortest possible traces as the oscillation characteristics are subject to the variation of trace patterns.
- Do not take a signal directly from the oscillator circuit.
- Do not place the oscillator circuit in the vicinity of any lines that carry large current.
- Exercise extreme care in the wiring method when using low consumption XT amplifier mode.

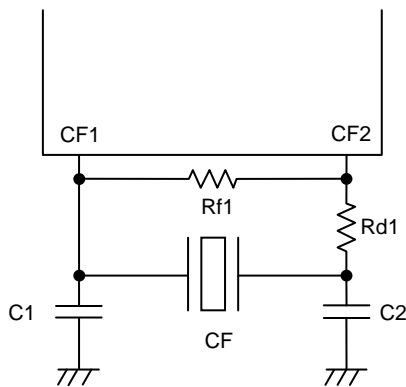


Figure 1 CF Oscillator Circuit

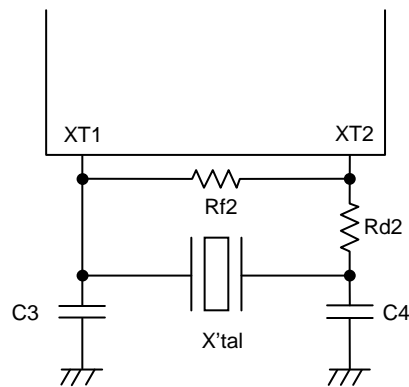


Figure 2 XT Oscillator Circuit

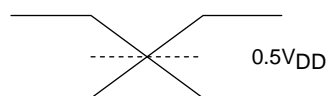
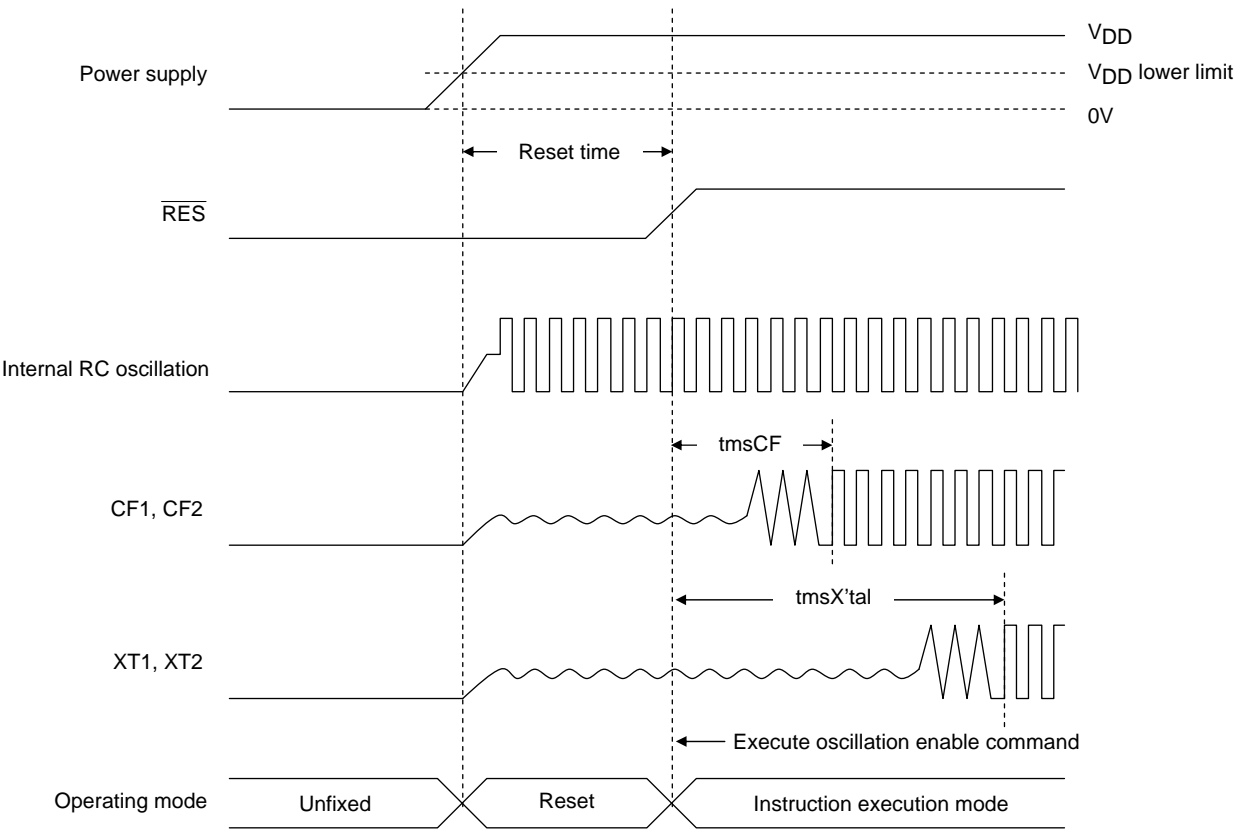
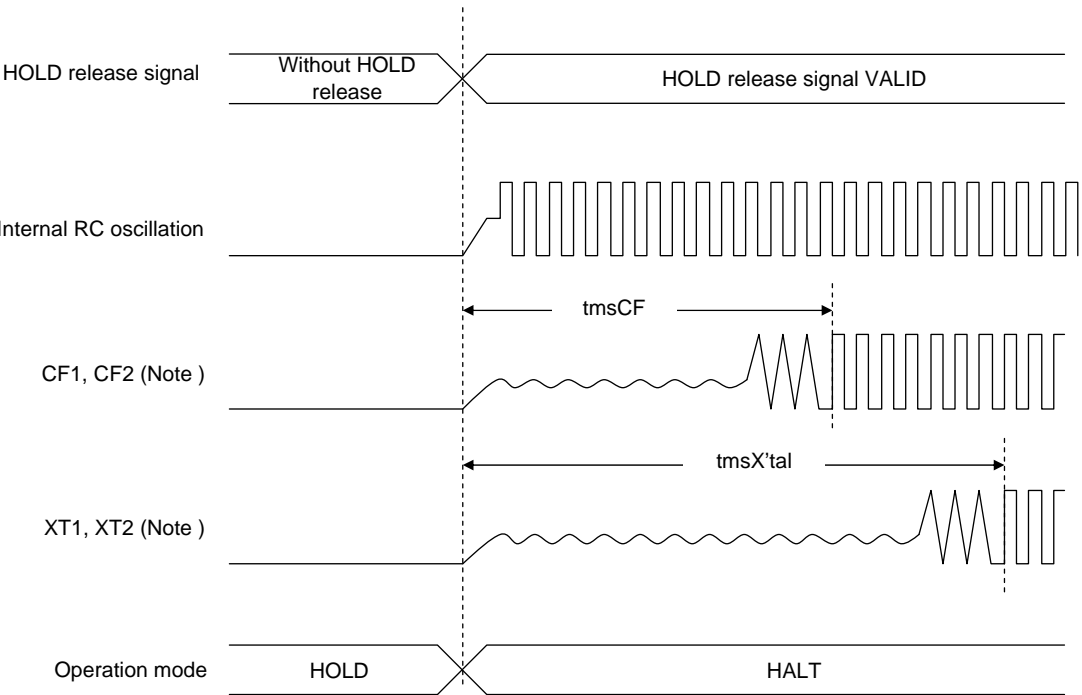


Figure 3 AC Timing Measurement Point



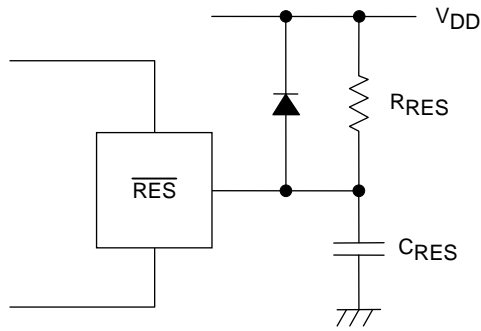
Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Note: Oscillation is enabled before HOLD mode is entered.

Figure 4 Oscillation Stabilization Time



Note:  
External circuits for reset may vary depending on the usage of POR. Please refer to the user's manual on reset function.

Figure 5 Reset Circuit

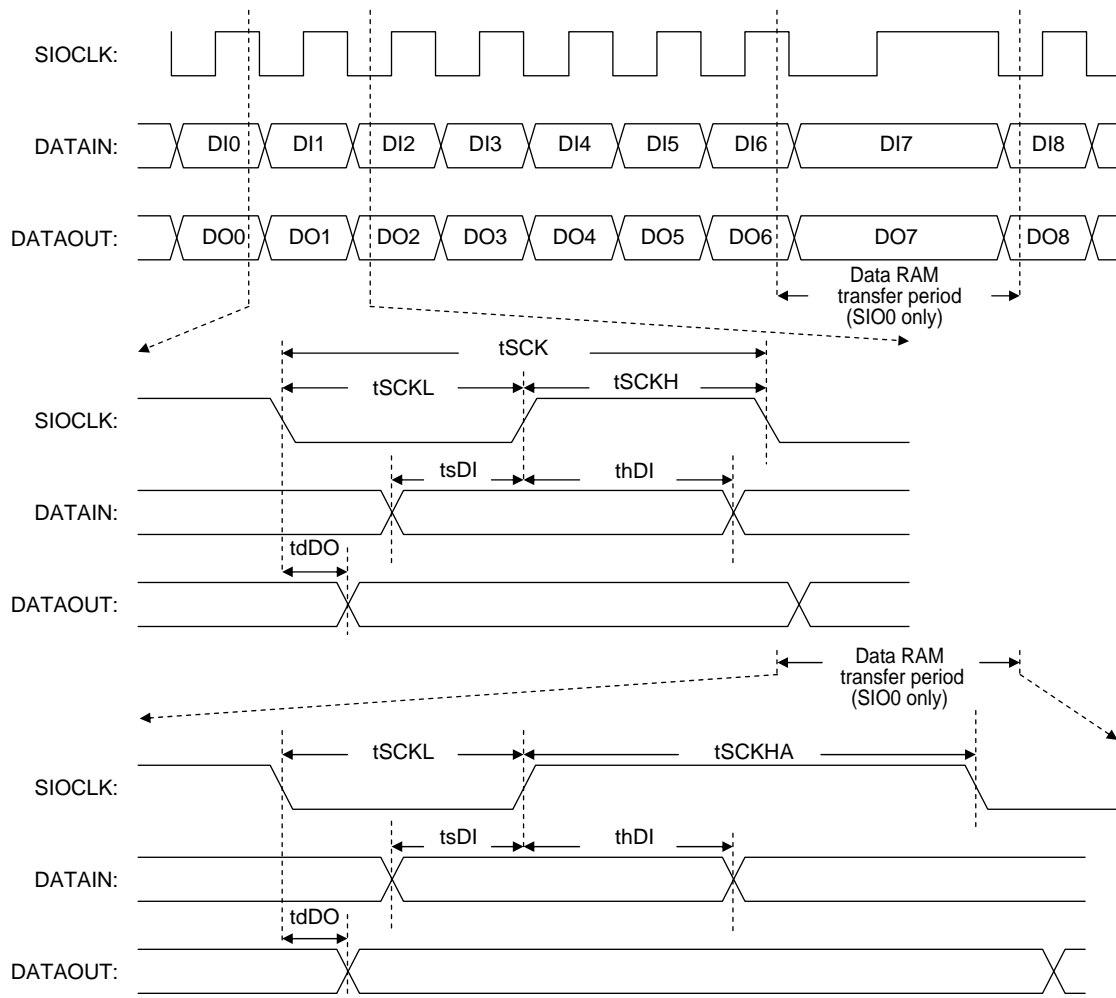


Figure 6 Serial Input/Output Waveform

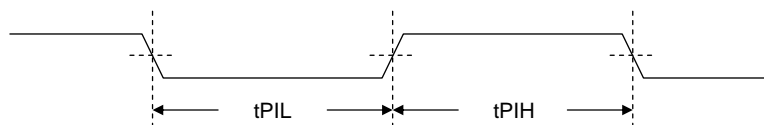


Figure 7 Pulse Input Timing Waveform

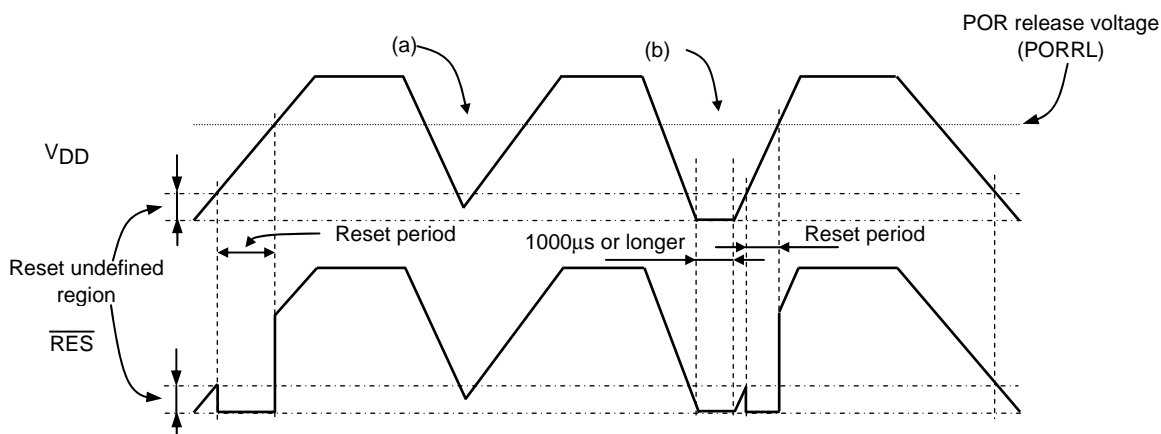


Figure 8 Sample Operating Waveforms when POR is Used  
(Reset pin: Pull-up resistor  $R_{RES}$  only)

- The POR function generates a reset only when power is turned on starting at the  $V_{SS}$  level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the  $V_{SS}$  level as shown in (a).
- A reset is generated only when the power level goes down to the  $V_{SS}$  level as shown in (b) and power is turned on again after this condition continues for 1000µs or longer.

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