

## SANYO Semiconductors **DATA SHEET**

An ON Semiconductor Company

# LC87F2708A — Short Short

#### Overview

The LC87F2708A is an 8-bit microcotroller that, centered around a CPU running at a minimum bus cycle time of 100ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM (onboard programmable), 512-byte RAM, an on-chip debugger, a sophisticated 16-bit timer/counter (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers or PWMs), a synchronous SIO interface, a high-speed 12-bit PWM, two high-speed pulse width/period counters, a 7-channel AD converter with 12-/8-bit resolution selector, an analog comparator, a watchdog timer, an internal reset circuit, a system clock frequency divider, and a 16-source 10-vector interrupt feature.

#### **Features**

- ■Flash ROM
  - Capable of on-board programming of voltage source (3.0 to 5.5V)
  - Block-erasable in 128 byte units
  - $8192 \times 8$  bits

#### ■RAM

•  $512 \times 9$  bits

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#### **SANYO Semiconductor Co., Ltd.**

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■Minimum Bus Cycle Time Note1

• 100ns (10MHz) V<sub>DD</sub>=2.7 to 5.5V Note2

■Minimum Instruction Cycle Time

• 300ns (10MHz) V<sub>DD</sub>=2.7 to 5.5V Note2

Note1: The bus cycle time here refers to the ROM read speed.

Note2: Use this product in a voltage range of 3.0 to 5.5V because the minimum release voltage (PORRL) of the power-on reset (POR) circuit is 2.87V±0.12V.

#### **■**Ports

• I/O ports

Ports whose I/O direction can be designated in 1-bit units 11 (P10 to P16, P30 to P33)

• Reset pins 1 (RES)

• Power pins 2 (V<sub>SS</sub>1, V<sub>DD</sub>1)

#### **■**Timers

• Timer 0: 16-bit timer/counter with a capture register.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)  $\times$  2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register)

+ 8-bit counter (with an 8-bit capture register)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16-bit counter (with a 16-bit capture register)

• Timer 1: 16-bit timer/counter that can provide with PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/

counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler  $\times$  2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs)

(toggle output also possible from the lower-order 8 bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs)

(Lower-order 8 bits may be used as PWM)

#### ■Serial Interface

- SIO7: 8-bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3 tCYC)

#### ■High-Speed 12-bit PWM

- System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
- Duty/period programmable
- Continuous PWM output/specific count PWM output (automatic stop) selectable

#### ■ High-speed Pulse/Period Counter

- HCT1: High-speed pulse width/period counter 1
  - 1) System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
  - 2) H-level width/L-level width/period measurement modes selectable
  - 3) Input triggering noise filter
- HCT2: High-speed pulse width/period counter 2
  - 1) System clock/high-speed RC oscillation clock (20MHz or 40MHz) operation selectable
  - 2) Can measure both L-level width and period simultaneously.
  - 3) Input triggering noise filter
  - 4) Input trigger selectable (from 3 signals, i.e., P11/HCT2IN, P31/HCT2IN, and analog comparator output)

#### ■ AD Converter: 12 bits $\times$ 7 channels

• 12-/8-bits AD converter resolution selectable

#### ■Analog Comparator

- Sends output to the P32/CMPO port (polarity selectable).
- Edge detection function (shared with INTC and also allows the selection of the noise filter function)

#### ■Watchdog Timer

- Can generate the internal reset signal on a timer overflow monitored by the WDT-dedicated low-speed RC oscillation clock (30kHz).
- Allows selection of continue, stop, or hold mode operation of the counter on entry into the HALT/ HOLD mode.

#### ■Interrupts Source Flags

- 16 sources, 10 vector addresses
  - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INTA
2	0000BH	X or L	INTB
3	00013H	H or L	INTC/T0L/INTE
4	0001BH	H or L	INTD/INTF
5	00023H	H or L	T0H/SIO7
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	HCT1
8	0003BH	H or L	HCT2
9	00043H	H or L	ADC/HPWM automatic stop/HPWM cycle
10	0004BH	H or L	None

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- ■Subroutine Stack Levels: 256levels maximum (The stack is allocated in RAM.)
- ■High-speed Multiplication/Division Instructions

16 bits × 8 bits
24 bits × 16 bits
16 bits ÷ 8 bits
24 bits ÷ 16 bits
16 bits ÷ 16 bits
17 tCYC execution time
18 tCYC execution time
19 tCYC execution time
10 tCYC execution time
11 tCYC execution time
12 tCYC execution time
13 tCYC execution time
14 tCYC execution time
15 tCYC execution time
16 tCYC execution time
17 tCYC execution time
18 tCYC execution time
19 tCYC execution time
10 tCYC execution time

#### ■Oscillation Circuits

Medium speed RC oscillation circuit (internal):
 Low speed RC oscillation circuit (internal):
 For system clock (1MHz)
 For watchdog timer (30kHz)

• High speed RC oscillation circuit (internal): For system clock (20MHz or 40MHz)

1) 2 source oscillation frequencies (20MHz or 40MHz) selectable for the high-speed RC oscillation circuit by optional configuration.

#### ■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (when high speed RC oscillation is selected for system clock.).

#### ■Internal reset circuit

- Power-on reset (POR) function
  - 1) POR reset is generated only at power-on time.
  - 2) The POR release level can be selected from 3 levels (2.87V, 3.86V, and 4.35V) by optional configuration.
- Low-voltage detection reset (LVD) function
  - LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  - 2) The use or disuse of the LVD function and the low voltage threshold level (3 levels: 2.81V, 3.79V and 4.28V). can be selected by optional configuration.

#### ■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) There are the following three ways of resetting the HALT mode.
    - (1) Setting the reset pin to the low level
    - (2) Generating a reset signal via the watchdog timer or brown-out detector
    - (3) Having an interrupt generated
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The medium- and high-speed RC oscillation circuits automatically stop operation.
  - 2) There are the following four ways of resetting the HOLD mode.
    - (1) Setting the reset pin to the lower level.
    - (2) Generating a reset signal via the watchdog timer or brown-out detector
    - (3) Setting at least one of the INTA, INTB, INTC, INTD, INTE, and INTF pins to the specified level (INTA and INTB HOLD mode reset is available only when level detection is set.)
    - (4) Applying input signals to the IN+ and IN- pins so that the analog comparator output is set to the specified level (when the analog comparator output is assigned to the INTC input)

#### ■On-chip Debugger Function

- Supports software debugging with the IC mounted on the target board (LC87D2708A). LC87F2708A has an On-chip debugger but its function is limited.
- 3 channels of on-chip debugger pins are available.

## ■Data Security Function Note3

Protects the program data stored in flash memory from unauthorized read or copy.
 Note3: This data security function does not necessarily provide absolute data security.

#### ■Package Form

• MFP14S(225mil): Lead-free Type

#### **■**Development Tools

On-chip debugger: 1) TCB87-Type B + LC87D2708A

2) TCB87-Type B + LC87F2708A

3) TCB87-Type C (3 wire version) + LC87D2708A

4) TCB87-Type C (3 wire version) + LC87F2708A

#### **■**Programming Board

Package	Programming Board
MFP14S(225mil)	W87F27M-DBG

#### ■Flash ROM Programming Board

Maker		Model	Version	Device	
Flash Support Group, Inc. (FSG)	In circuit	AF9101/AF9103 (Main body) (FSG models)		LC87F2708A	
+ SANYO (Note 4)	In-circuit Programmer	SIB87 (Inter Face Driver) (SANYO model)	(Note 5)		
SANYO	Single/Gang Programmer In-circuit/ Gang Programmer	SKK-DBG Type B (SANYO FWS)	Application Version 1.04 or later Chip Data Version 2.10 or later	LC87F2708A	

For information about AF-series:

Flash Support Group, Inc. TEL: +81-53-459-1050 E-mail: sales@j-fsg.co.jp

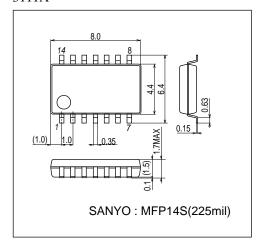
Note4: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from SANYO (SIB87) together can give a PC-less, standalone on-board-programming capabilities.

Note5: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or SANYO for the information.

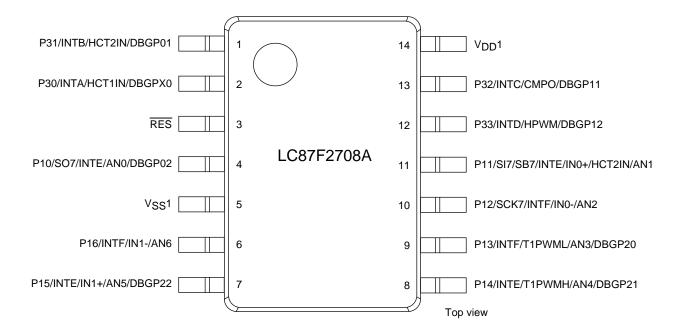
#### **Package Dimensions**

unit : mm (typ)

3111A



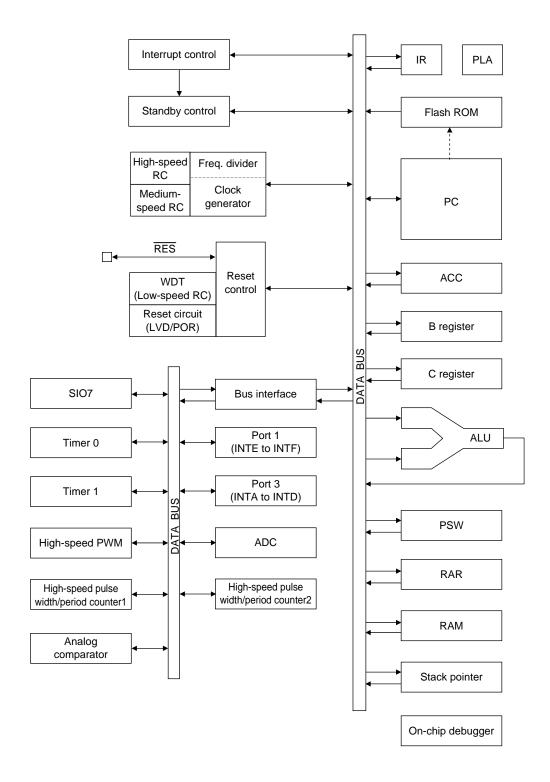
## **Pin Assignment**



SANYO: MFP14S(225mil) "Lead-free Type"

MFP14S	NAME	MFP14S	NAME
1	P31/INTB/HCT2IN/DBGP01	8	P14/INTE/T1PWMH/AN4/DBGP21
2	P30/INTA/HCT1IN/DBGPX0	9	P13/INTF/T1PWML/AN3/DBGP20
3	RES	10	P12/SCK7/INTF/IN0-/AN2
4	P10/SO7/INTE/AN0/DBGP02	11	P11/SI7/SB7/INTE/IN0+/HCT2IN/AN1
5	V <sub>SS</sub> 1	12	P33/INTD/HPWM/DBGP12
6	P16/INTF/IN1-/AN6	13	P32/INTC/CMPO/DBGP11
7	P15/INTE/IN1+/AN5/DBGP22	14	V <sub>DD</sub> 1

## **System Block Diagram**



## **Pin Description**

Pin Name	I/O			Desc	ription			Option		
V <sub>SS</sub> 1	-	- power supply p	in					No		
V <sub>DD</sub> 1	-	+ power supply p	+ power supply pin							
PORT1	I/O	• 7-bit I/O port								
P10 to P16		I/O specifiable	• I/O specifiable in 1-bit units							
		Pull-up resistor	Pull-up resistors can be turned on and off in 1-bit units							
		Multiplexed pin	Multiplexed pins							
		P10: SIO7 data	P10: SIO7 data output							
		P11: SIO7 data	input/bus I/O/hig	gh-speed pulse v	width/period cour	nter 2 input				
		P12: SIO7 cloc	k I/O							
		P13: Timer 1 P	WML output							
		P14: Timer 1 P	WMH output							
		P10, P11, P14,	P15:							
		INTE inpu	t/HOLD release	input/timer 1 eve	ent input/timer 0L	. capture input/				
		timer 0H o	capture input							
		P12, P13, P16:								
		INTF inpu	t/HOLD release	input/timer 1 eve	ent input/timer 0L	. capture input/				
		timer 0H o	capture input							
		AD converter in	put port: AN0 to	AN6(P10 to P16	5)					
		Analog compar	ator input port 0:	IN0+, IN0-(P11,	P12)					
		Analog compar	ator input port 1:	IN1+, IN1-(P15,	P16)					
		On-chip debugg	ger pin 1: DBGP	02 (P10)						
		On-chip debug	ger pin 3: DBGP2	20 to DBGP22 (F	P13 to P15)					
		<ul> <li>Interrupt ackno</li> </ul>	wledge type				1			
			Rising	Falling	Rising &	H level	L level			
			g	9	Falling		2.010.			
		INTE	enable	enable	enable	disable	disable			
		INTF	enable	enable	enable	disable	disable			
PORT3	I/O	• 4-bit I/O port						Yes		
P30 to P33		I/O specifiable	in 1-bit units							
		Pull-up resistor	s can be turned	on and off in 1-b	it units					
		Multiplexed pin	s							
		P30: INTA inpu	t/HOLD release	input/timer 0L ca	pture input/high-	speed pulse wid	lth/			
		period cou	unter 1 input							
		P31: INTB inpu	t/HOLD release	input/timer 0H ca	apture input/high	-speed pulse wi	dth/			
		period cou	unter 2 input							
		P32: INTC input/HOLD release input/timer 0 event input/timer 0L capture input/ analog comparator output								
		1		inpublimer o eve	ant input timer of	. captaro input				
		analog co			·					
		analog co P33: INTD inpu	mparator output		·					
		analog co P33: INTD inpu high-spee	mparator output t/HOLD release	input/timer 0 eve	ent input/timer 0H					
		analog co P33: INTD inpu high-spee On-chip debug	mparator output t/HOLD release d PWM output	input/timer 0 eve	ent input/timer 0H	I capture input/				
		analog co P33: INTD inpu high-spee On-chip debug	mparator output nt/HOLD release d PWM output ger pin 1: DBGP ger pin 2: DBGP	input/timer 0 eve	ent input/timer 0H	I capture input/				
		analog co P33: INTD inpu high-spee On-chip debug On-chip debug	mparator output tt/HOLD release d PWM output ger pin 1: DBGP; ger pin 2: DBGP; wledge type	input/timer 0 eve K0 to DBGP01 (I K0 to DBGP12 (I	ent input/timer 0H	I capture input/	Llow			
		analog co P33: INTD inpu high-spee On-chip debug On-chip debug	mparator output nt/HOLD release d PWM output ger pin 1: DBGP ger pin 2: DBGP	input/timer 0 eve	P30 to P31) P30, P32 to P33	I capture input/	L level			
		analog co P33: INTD inpu high-spee On-chip debugg On-chip debugg • Interrupt ackno	mparator output t/HOLD release d PWM output ger pin 1: DBGP; ger pin 2: DBGP; wledge type Rising	K0 to DBGP01 (I K0 to DBGP12 (I Falling	P30 to P31) P30, P32 to P33 Rising & Falling	H capture input/				
		analog co P33: INTD inpu high-spee On-chip debugg On-chip debugg • Interrupt ackno	mparator output tt/HOLD release d PWM output ger pin 1: DBGP2 ger pin 2: DBGP2 wledge type Rising enable	K0 to DBGP01 (IK0 to DBGP12 (IK0 to DBGP12)  Falling  enable	P30 to P31) P30, P32 to P33 Rising & Falling disable	H capture input/  H level  enable	enable			
		analog co P33: INTD inpu high-spee On-chip debugg On-chip debugg • Interrupt ackno  INTA INTB	mparator output tt/HOLD release d PWM output ger pin 1: DBGP2 ger pin 2: DBGP2 wledge type Rising enable enable	K0 to DBGP01 (IK0 to DBGP12 (IF) Falling enable enable	P30 to P31) P30, P32 to P33  Rising & Falling disable disable	H level enable enable	enable enable			
		analog co P33: INTD inpu high-spee On-chip debugg On-chip debugg • Interrupt ackno	mparator output tt/HOLD release d PWM output ger pin 1: DBGP2 ger pin 2: DBGP2 wledge type Rising enable	K0 to DBGP01 (IK0 to DBGP12 (IK0 to DBGP12)  Falling  enable	P30 to P31) P30, P32 to P33 Rising & Falling disable	H capture input/  H level  enable	enable			

#### **Port Output Types**

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option Sselected in Units of	Option Type	Output Type	Pull-up Resistor
P10 to P16	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P33	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable

#### **On-chip Debugger Pin Processing**

For the processing of the on-chip debugger pins, refer to the separately available documents entitled "RD87 On-chip Debugger Installation" and "LC872000 Series On-chip Debugger Pin Processing."

#### **Recommended Unused Pin Connections**

Din Name	Recommended Unu	sed Pin Connections
Pin Name	Board	Software
P10 to P16	OPEN	Set output low
P30 to P33	OPEN	Set output low

## **User Option Table**

Option Name	Option Type	Flash Version	Option Switched in Unit of	Description
Port output type	P10 to P16	0	1 bit	CMOS
				Nch-open drain
	P30 to P33	0	1 bit	CMOS
				Nch-open drain
Program start	-	0	-	00000h
address				01E00h
Brown-out detector	Brown-out detector	0	-	Enable: Used
reset function	function			Disable: Not Used
	Brown-out trip level	0	-	3 levels
Power-on-reset function	Power-on-reset level	0	-	3 levels
High-speed RC	Oscillation frequency	0	-	20 MHz
oscillator circuit				40 MHz

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = 0V$

Parameter   Symbol   Pin/Remarks   Conditions   Specification			т		, 55					
Maximum supply voltage   VoD max   VoD1   RES		Doromotor	Symbol	Din/Domorko	Conditions			Specif	ication	
Input voltage   V  RES			Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Peak output current			V <sub>DD</sub> max	V <sub>DD</sub> 1			-0.3		+6.5	
Peak output current	Inp	out voltage	VI	RES			-0.3		V <sub>DD</sub> +0.3	V
Peak output current   IOPH(1)   Port 1   CMOS output selected per applicable pin   Per appl	Inp	out/output	V <sub>IO</sub>	• Port 1			0.2		V 10 2	
Current   DPH(2)   Port 3   CMOS output selected per applicable pin   -7.5	vol	tage		• Port 3			-0.3		VDD+0.3	
Current   IOPH(2)   Port 3   CMOS output selected per applicable pin   -10		Peak output	IOPH(1)	Port 1	CMOS output selected		-7.5			
Mean output current   IOMH(1)   Port 1   CMOS output selected per applicable pin   -5		current					0			
Mean output current (Note 1-1)   IOMH(1)   Port 1   CMOS output selected per applicable pin   Port 3   Port 4   Port 4   Port 5   Port 3   Port 3   Port 3   Port 4   Port 5   Port 3   Port 3   Port 4   Port 5   Port 3   Port 4   Port 5   Port 5   Port 3   Port 4   Port 6   Port 6			IOPH(2)	Port 3	'		-10			
Ports 11 to 14   Ports 32, 33   applicable pins   Ports 32, 33   applicable pins	ent	Managarata	IOMIT(4)	Dort 4						
Ports 11 to 14   Ports 32, 33   applicable pins   Ports 32, 33   applicable pins	curr	· ·	IOMH(1)	Port 1	· .		-5			
Ports   11 to 14   Ports   23, 33   Section   Ports   12 to 14   Ports   32, 33   Section   Ports   34, 35   Section   Ports	put		IOMH(2)	Port 3						
Ports   11 to 14   Ports   23, 33   Section   Ports   12 to 14   Ports   32, 33   Section   Ports   34, 35   Section   Ports	ont	(14010-1-1)	IOWII I(Z)	1 011 5	· .		-7.5			
Ports   11 to 14   Ports   23, 33   Section   Ports   12 to 14   Ports   32, 33   Section   Ports   34, 35   Section   Ports	eve	Total output	ΣΙΟΑΗ(1)	• Ports 10, 15, 16						
Ports 11 to 14   Ports 32, 33   applicable pins   Ports 32, 33   applicable pins	igh I	-	- ( )				-20			
Ports 32, 33   applicable pins	I		ΣΙΟΑΗ(2)	• Ports 11 to 14	Total of currents at all					
Peak output current   IOPL(1)   Port 1   Per applicable pin   15				• Ports 32, 33	applicable pins		-20			
Peak output current         IOPL(1)         Port 1         Per applicable pin         15           Mean output current (Note 1-1)         IOML(1)         Port 3         Per applicable pin         10           Total output current         IOML(2)         Port 3         Per applicable pin         7.5           Total output current         ΣΙΟΑL(1)         • Port 10         Total of currents at all applicable pins         25           ΣΙΟΑL(2)         • Ports 30, 31         applicable pins         35           ΣΙΟΑL(3)         • Port 1         Total of currents at all applicable pins         35           Power dissipation         Pd max(1)         MFP14S(225mil)         • Ta=-40 to +85°C			ΣΙΟΑΗ(3)	• Port 1	Total of currents at all		25			mA
Current         IOPL(2)         Port 3         Per applicable pin         10           Mean output current (Note 1-1)         IOML(1)         Port 1         Per applicable pin         10           Total output current         ΣIOAL(1)         • Port 10         Total of currents at all applicable pins         25           ΣIOAL(2)         • Ports 30, 31         applicable pins         35           ΣIOAL(3)         • Port 1         Total of currents at all applicable pins         35           ΣIOAL(3)         • Port 1         Total of currents at all applicable pins         55           Power dissipation         Pd max(1)         MFP14S(225mil)         • Ta=-40 to +85°C				• Port 3	applicable pins		-33			
Mean output current (Note 1-1)   IOML(1)   Port 1   Per applicable pin   10		·	IOPL(1)	Port 1	Per applicable pin				15	
ΣΙΟΑL(3)         • Port 1         Total of currents at all applicable pins         55           Power dissipation         Pd max(1)         MFP14S(225mil)         • Ta=-40 to +85°C		current	IOPL(2)	Port 3	Per applicable pin				10	
ΣΙΟΑL(3)         • Port 1         Total of currents at all applicable pins         55           Power dissipation         Pd max(1)         MFP14S(225mil)         • Ta=-40 to +85°C	rent	Mean output	IOML(1)	Port 1	Per applicable pin				10	
ΣIOAL(3)         • Port 1         Total of currents at all         • Port 3         applicable pins         55           Power dissipation         Pd max(1)         MFP14S(225mil)         • Ta=-40 to +85°C	put cur		IOML(2)	Port 3	Per applicable pin				7.5	
ΣΙΟΑL(3)         • Port 1         Total of currents at all applicable pins         55           Power dissipation         Pd max(1)         MFP14S(225mil)         • Ta=-40 to +85°C	vel out	=	ΣIOAL(1)						25	
ΣΙΟΑL(3)         • Port 1         Total of currents at all applicable pins         55           Power dissipation         Pd max(1)         MFP14S(225mil)         • Ta=-40 to +85°C	w le		ΣIOAL(2)	·					0.5	
● Port 3 applicable pins 55  Power dissipation Pd max(1) MFP14S(225mil) ● Ta=-40 to +85°C	Lo			• Ports 32, 33	applicable pins				35	
● Port 3 applicable pins  Power dissipation Pd max(1) MFP14S(225mil) ● Ta=-40 to +85°C			ΣIOAL(3)	• Port 1	Total of currents at all				55	
Power dissipation Pd max(1) MFP14S(225mil) • Ta=-40 to +85°C				• Port 3					00	
• Independent package	Po	wer dissipation	Pd max(1)	MFP14S(225mil)					113	
Pd max(2) • Ta=-40 to +85°C			Pd max(2)		• Ta=-40 to +85°C					mW
Mounted on thermal test 260					Mounted on thermal test				260	11100
board									200	
• (Note 1-2)					• (Note 1-2)					
Operating ambient Topr -40 +85		•	Topr				-40		+85	
temperature		•	T. (							°C
Storage ambient Tstg +125 temperature		•	ıstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over  $100 \mathrm{ms}$ .

Note 1-2: Thermal test board used conforms to SEMI (size: 76.1×114.3×1.6tmm, glass epoxy board).

#### Allowable Operating Range at $Ta = -40 \text{ to } +85^{\circ}\text{C}, V_{SS}1 = 0\text{V}$

Parameter	Symbol	Pin/Remarks	Conditions			Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	V <sub>DD</sub>	V <sub>DD</sub> 1	0.272μs ≤ tCYC ≤ 100μs		2.7		5.5	
Memory sustaining supply voltage	V <sub>HD</sub>	V <sub>DD</sub> 1	RAM and register contents sustained in HOLD mode		2.0		5.5	
High level input voltage	V <sub>IH</sub> (1)	• Port 1 • Port 3	Output disabled	2.7 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	V
	V <sub>IH</sub> (2)	RES		2.7 to 5.5	0.75V <sub>DD</sub>		$V_{DD}$	
Low level input voltage	V <sub>IL</sub> (1)	• Port 1 • Port 3	Output disabled	4.0 to 5.5	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.4	
				2.7 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	RES		2.7 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
Instruction cycle time (Note 2-2)	tCYC			2.7 to 5.5	0.272		100	μs
Oscillation frequency range	FmHRC(1)		<ul> <li>High-speed RC oscillation</li> <li>40MHz selected as option</li> <li>Ta=-20 to +85°C</li> </ul>	4.5 to 5.5	38	40	42	
	FmHRC(2)		High-speed RC oscillation	4.5 to 5.5	37.6	40	42.4	
	FmHRC(3)		40MHz selected as option	3.5 to 5.5	36.8	40	43.2	
	FmHRC(4)		• Ta=-40 to +85°C	2.7 to 5.5	32	40	43.2	
	FmHRC(5)		<ul> <li>High-speed RC oscillation</li> <li>20MHz selected as option</li> <li>Ta=-20 to +85°C</li> </ul>	3.0 to 5.5	19	20	21	MHz
	FmHRC(6)		<ul> <li>High-speed RC oscillation</li> <li>20MHz selected as option</li> <li>Ta=-40 to +85°C</li> </ul>	2.7 to 5.5	18.7	20	21.3	
	FmRC		Medium-speed RC oscillation	2.7 to 5.5	0.5	1.0	2.0	
	FmSLRC		Low-speed RC oscillation	2.7 to 5.5	15	30	60	kHz
Oscillation stabilization time	tmsHRC		<ul> <li>When high-speed RC oscillation state is switched from stopped to enabled.</li> <li>See Fig. 2.</li> </ul>	2.7 to 5.5			100	μs

Note 2-1: Use this product in a voltage range of 3.0 to 5.5V because the minimum release voltage (PORRL) of the power-on reset (POR) circuit is 2.87V±0.12V.

Note 2-2: Relationship between tCYC and oscillation frequency is as follows:

- When system clock source is set to medium-speed RC oscillation 3/FmRC at a division ratio of 1/1, 6/FmRC at a division ratio of 1/2, 12/FmRC a division ratio of 1/4, and so forth
- When system clock source is set to high-speed RC oscillation (40MHz selected by optional configuration) 12/FmHRC at a division ratio of 1/1, 24/FmHRC at a division ratio of 1/2, 48/FmHRC a division ratio of 1/4, and so forth
- When system clock source is set to high-speed RC oscillation (20MHz selected by optional configuration) 6/FmHRC at a division ratio of 1/1, 12/FmHRC at a division ratio of 1/2, 24/FmHRC a division ratio of 1/4, and so forth

## Electrical Characteristics at $Ta = -40 \text{ to } +85^{\circ}\text{C}, \ V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			Specifica	ation	
Farameter	Symbol	Fill/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High level input current	I <sub>IH</sub> (1)	• Port 1 • Port 3	Output disabled Pull-up resistor off VIN=VDD (including output Tr. off leakage current)	2.7 to 5.5			1	
	I <sub>IH</sub> (2)	RES	V <sub>IN</sub> =V <sub>DD</sub>	2.7 to 5.5			1	μΑ
Low level input current	Ιμ	• Port 1 • Port 3	Output disabled     Pull-up resistor off     VIN=VSS     (including output Tr. off leakage current)	2.7 to 5.5	-1			
High level output	V <sub>OH</sub> (1)	CMOS output	I <sub>OH</sub> =-1mA	4.5 to 5.5	V <sub>DD</sub> -1			
voltage	V <sub>OH</sub> (2)	type port 1	I <sub>OH</sub> =-0.35mA	2.7 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)	CMOS output	I <sub>OH</sub> =-5mA	4.5 to 5.5	V <sub>DD</sub> -1.5			
	V <sub>OH</sub> (4)	type port 3	I <sub>OH</sub> =-0.7mA	2.7 to 5.5	V <sub>DD</sub> -0.4			V
Low level output	V <sub>OL</sub> (1)	Port 1	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5	
voltage	V <sub>OL</sub> (2)		I <sub>OL</sub> =1.4mA	2.7 to 5.5			0.4	
	V <sub>OL</sub> (3)	Port 3	I <sub>OL</sub> =5mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (4)		I <sub>OL</sub> =0.7mA	2.7 to 5.5			0.4	
Pull-up resistance	Rpu(1)	• Port 1	V <sub>OH</sub> =0.9V <sub>DD</sub>	4.5 to 5.5	15	35	80	
	Rpu(2)	• Port 3		2.7 to 4.5	18	50	150	kΩ
	Rpu(3)	RES		2.7 to 5.5	216	360	504	
Hysteresis voltage	VHYS	• Port 1 • Port 3 • RES		2.7 to 5.5		0.1V <sub>DD</sub>		V
Pin capacitance	СР	All pins	V <sub>IN</sub> =V <sub>SS</sub> for pins other than that under test     f=1MHz     Ta=25°C	2.7 to 5.5		10		pF

## Serial I/O Characteristics at $Ta = -40 \text{ to } +85^{\circ}\text{C}, \ V_{SS}1 = 0V$

## 1. SIO7 Serial I/O Characteristics (Note 4-1-1)

		Parameter	Symbol	Pin/	Conditions			Spec	ification	
		raiametei	Symbol	Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
	×	Frequency	tSCK(1)	SCK7(P12)	• See Fig. 4 (Note 4-1-2)		2			
	Input clock	Low level pulse width	tSCKL(1)			2.7 to 5.5	1			tCYC
Serial clock	4	High level pulse width	tSCKH(1)				1			icre
Serial	ıck	Frequency	tSCK(2)	SCK7(P12)	CMOS output selected     See Fig. 4.		4/3			
	Output clock	Low level pulse width	tSCKL(2)			2.7 to 5.5		1/2		tSCK
		High level pulse width	tSCKH(2)				1/2		ISON	
input	Data	Data setup time tsDI(1)		tsDI(1)  SB7(P11), SI7(P11)  • Must be specified with respect to rising edge of SIOCLK. • See Fig. 4.		2.7 to 5.5	0.03			
Serial		ta hold time	thDI(1)			2.7 10 3.3	0.03			
output	Input clock	Output delay time	tdDO(1)	SO7(P10), SB7(P11)	Must be specified with respect to rising edge of SIOCLK.     Must be specified as the time to the beginning of output state change in open drain output	2740 5 5			1tCYC +0.05	μs
Serial output	Output clock		tdDO(2)		mode • See Fig. 4.	2.7 to 5.5			(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in transmission/reception mode, the time from SI7RUN being set when serial clock is "H" to the first falling edge of the serial clock must be longer than 1tCYC.

## Pulse Input Conditions at $Ta = -40 \text{ to } +85^{\circ}\text{C}$ , $V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min.	typ.	max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	INTA(P30), INTB(P31), INTD(P33), INTE (P10, P11, P14, P15), INTF(P12, P13, P16)	Interrupt source flag can be set.     Event inputs for timers 0 and 1 are enabled.	2.7 to 5.5	1			
	tPIH(2) tPIL(2)	INTC(P32) when noise filter time constant is "none"	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.7 to 5.5	1			1010
	tPIH(3) tPIL(3)	INTC(P32) when noise filter time constant is "1/16"	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.7 to 5.5	64			tCYC
	tPIH(4) tPIL(4)	INTC(P32) when noise filter time constant is "1/32"	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.7 to 5.5	128			
	tPIH(5) tPIL(5)	INTC(P32) when noise filter time constant is "1/64"	<ul><li>Interrupt source flag can be set.</li><li>Event inputs for timer 0 are enabled.</li></ul>	2.7 to 5.5	256			
	tPIH(6) tPIL(6)	HCT1IN(P30)	Pulses can be recognized as signals by the high-speed pulse width/period counter 1.	2.7 to 5.5	3			H1CK (Note 5-1)
	tPIH(7) tPIL(7)	HCT2IN(P11, P31)	Pulses can be recognized as signals by the high-speed pulse width/period counter 2.	2.7 to 5.5	6			H2CK (Note 5-2)
	tPIL(8)	RES	Resetting is enabled.	2.7 to 5.5	200			μs

Note 5-1: H1CK denotes the period of the base clock (1 to  $8 \times \text{high-speed RC}$  oscillation clock or system clock) for the high-speed pulse width/period counter 1.

Note 5-2: H2CK denotes the period of the base clock (2 to  $16 \times \text{high-speed RC}$  oscillation clock or system clock) for the high-speed pulse width/period counter 2.

## Comparator Characteristics at $Ta = -40 \text{ to } +85^{\circ}\text{C}, V_{SS}1 = 0\text{V}$

			1					
Parameter	Symbol	Pin/Remarks	Conditions		Specification			
1 didinotoi Symbol	FIII/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Common mode input voltage range	VCMIN	IN0+(P11), IN0-(P12), IN1+(P15),		2.7 to 5.5	V <sub>SS</sub>		V <sub>DD</sub> -1.5	>
Offset voltage	VOFF	IN1-(P16)	Within common mode input voltage range	2.7 to 5.5		±10	±30	mV
Response time	tRT		Within common mode input voltage range     Input amplitude=100mV     Overdrive=50mV	2.7 to 5.5		200	600	ns
Operation stabilization time (Note 6-1)	tCMW			2.7 to 5.5			1.0	μs

Note 6-1: The interval after CMPON is set till the operation gets stabilized.

#### **AD Converter Characteristics** at $V_{SS}1 = 0V$

#### <12-bits AD Converter Mode/Ta = -40 to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions		Specification				
Parameter	Symbol	Pin/Remarks	Cortailloris	V <sub>DD</sub> [V]	min	typ	max	unit	
Resolution	N	AN0(P10) to		3.0 to 5.5		12		bit	
Absolute accuracy	ET	AN6(P16)	(Note 7-1)	3.0 to 5.5			±16	LSB	
Conversion time	time tCAD	See Conversion time calculation	4.0 to 5.5	38		104.3			
			method • (Note 7-2)	3.0 to 5.5	75.8		104.3	μs	
Analog input voltage range	VAIN			3.0 to 5.5	VSS		$V_{DD}$	٧	
Analog port	Analog port IAINH	VAIN=V <sub>DD</sub>	3.0 to 5.5			1	•		
input current IAINL	VAIN=V <sub>SS</sub>	3.0 to 5.5	-1			μΑ			

#### <8-bits AD Converter Mode/Ta = -40 to +85°C >

Parameter	Cumbal	Pin/Remarks	Conditions			Specifi		
Farameter Symbol	Symbol	Pin/Remarks		$V_{DD}[V]$	min	typ	max	unit
Resolution	N	AN0(P10) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN6(P16)	(Note 7-1)	3.0 to 5.5			±1.5	LSB
Conversion time	Conversion time tCAD	See Conversion time calculation	4.0 to 5.5	23.4		64.3		
			method. • (Note 7-2)	3.0 to 5.5	46.7		64.3	μs
Analog input voltage range	VAIN			3.0 to 5.5	$V_{SS}$		$V_{DD}$	٧
Analog port	Analog port IAINH input current IAINL	VAIN=V <sub>DD</sub>	3.0 to 5.5			1		
input current		VAIN=V <sub>SS</sub>	3.0 to 5.5	-1			μΑ	

#### Conversion time calculation formulas:

12-bits AD Converter Mode:  $tCAD(Conversion\ time) = ((52/(Division\ ratio))+2)\times(1/3)\times tCYC$ 8-bits AD Converter Mode:  $tCAD(Conversion\ time) = ((32/(Division\ ratio))+2)\times(1/3)\times tCYC$ 

#### <Recommended Operating Conditions>

High-speed RC oscillation	Supply voltage range	System clock division ratio	Cycle time	AD division ratio	Conversion time (tCAD)		
(FmHRC)	(V <sub>DD</sub> )	(SYSDIV)	(tCYC)	(ADDIV)	12-bits AD	8-bits AD	
400411=/200411=	4.0V to 5.5V	1/1	300ns	1/8	41.8µs	25.8µs	
40MHz/20MHz	3.0V to 5.5V	1/1	300ns	1/16	83.4µs	51.4μs	

- Note 7-1: The quantization error  $(\pm 1/2LSB)$  is excluded from the absolute accuracy. The absolute accuracy is measured when no change occurs in the I/O state of the pins that are adjacent to the analog input channel during AD conversion processing.
- Note 7-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital conversion value against the analog input value is loaded in the result register.
  - \* The conversion time is 2 times the normal-time conversion time when:
  - The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
  - The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

#### Power-on Reset (POR) Characteristics at $Ta = -40 \text{ to } +85^{\circ}\text{C}$ , $V_{SS}1 = 0\text{V}$

				Specification				
Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit
POR release	PORRL		Option selected	2.87V	2.75	2.87	2.99	
voltage			• See Fig. 6. (Note 8-1)	3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	V
Detection voltage unknown state	POUKS		• See Fig. 6 (Note 8-2)			0.7	0.95	
Power supply rise time	PORIS		Power startup time from V <sub>DD</sub> =0V to 2.8V.				100	ms

Note 8-1: The POR release voltage can be selected from three levels when the low-voltage detection feature is deselected.

Note 8-2: There is an unpredictable period before the power-on reset transistor starts to turn on.

#### Low Voltage Detection Reset (LVD) Characteristics at $Ta = -40 \text{ to } +85^{\circ}\text{C}$ , VSS1 = 0V

					Specification				
Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit	
LVD reset Voltage	LVDET		Option selected.	2.81V	2.71	2.81	2.91		
(Note 9-2)			• See Fig. 7.	3.79V	3.69	3.79	3.89	V	
		(Note 9-1)	4.28V	4.18	4.28	4.38			
LVD voltage	LVHYS		(Note 9-3)	2.81V		60			
hysteresis				3.79V		65		mV	
				4.28V		65			
Detection voltage unknown state	LVUKS		• See Fig. 7. (Note 9-4)			0.7	0.95	٧	
Minimum low voltage detection width (response sensitivity)	tLVDW		• LVDET-0.5V • See Fig. 8.		0.2			ms	

Note 9-1: The LVD reset voltage can be selected from three levels when the low-voltage detection feature is selected.

Note 9-2: The hysteresis voltage is not included in the LVD reset voltage value.

Note 9-3: There are cases when the LVD reset voltage value is exceeded when a greater change in the output level or large current is applied to the port.

Note 9-4: There is an unpredictable period before the low-voltage detection resetting transistor starts to run.

## Consumption Current Characteristics at $Ta = -40 \text{ to } +85^{\circ}\text{C}, \ V_{SS}1 = 0V$

Parameter	Symbol	Pin/	Conditions	c, , ss -		Specifi	ication	
Farameter	Symbol	Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Normal mode consumption current	IDDOP(1)	V <sub>DD</sub> 1	FmHRC=40MHz oscillation mode     System clock set to high-speed RC, 10MHz (1/4 of 40MHz)	4.5 to 5.5		7.8	14	
(Note 10-1)	IDDOP(2)		Medium-speed RC oscillation stopped     System clock frequency division ratio set to 1/1	2.7 to 3.6		4.9	9.4	
	IDDOP(4)		<ul> <li>FmHRC=20MHz oscillation mode</li> <li>System clock set to high-speed RC, 10MHz (1/2 of 20MHz)</li> </ul>	4.5 to 5.5		7.1	12.8	
			Medium-speed RC oscillation stopped     System clock frequency division ratio set to 1/1	2.7 to 3.6		4.5	8.6	
	IDDOP(5)		<ul><li> High-speed RC oscillation stopped</li><li> System clock set to medium-speed RC</li></ul>	4.5 to 5.5		0.60	1.9	
	IDDOP(6)  HALT mode consumption current (Note 10-1)  IDDHALT(1)  IDDHALT(2)		oscillation mode • System clock frequency division ratio set to 1/2	2.7 to 3.6		0.38	1.3	
consumption			HALT mode • FmHRC=40MHz oscillation mode • System clock set to high-speed RC,	4.5 to 5.5		3.2	5.0	mA
(Note 10-1)			10MHz (1/4 of 40MHz)     Medium-speed RC oscillation stopped     System clock frequency division ratio set to 1/1	2.7 to 3.6		2.0	3.1	
	IDDHALT(3)		HALT mode FmHRC=20MHz oscillation mode System clock set to high-speed RC,	4.5 to 5.5		2.5	3.9	
	IDDHALT(4)		10MHz (1/2 of 20MHz)  • Medium-speed RC oscillation stopped  • System clock frequency division ratio set to 1/1			1.6	2.5	
	IDDHALT(5)		HALT mode  • High-speed RC oscillation stopped  • System clock set to medium-speed RC	4.5 to 5.5		0.32	1.0	
	IDDHALT(6)		oscillation mode  • System clock frequency division ratio set to 1/2	2.7 to 3.6		0.16	0.55	
HOLD mode	IDDHOLD(1)		HOLD mode	4.5 to 5.5		0.04	3.0	
consumption	IDDHOLD(2)		• Ta=-10 to +50°C	2.7 to 3.6		0.02	1.8	
current (Note 10-1)	IDDHOLD(3)		HOLD mode	4.5 to 5.5		0.04	34	
(11010 10 1)	IDDHOLD(4)		• Ta=-40 to +85°C	2.7 to 3.6		0.02	22	
	IDDHOLD(5)		HOLD mode	4.5 to 5.5		3.1	6.8	
	IDDHOLD(6)		LVD option selected     Ta=-10 to +50°C	2.7 to 3.6		2.4	4.2	
	IDDHOLD(7)		HOLD mode	4.5 to 5.5		3.1	39	
	IDDHOLD(8)		<ul> <li>LVD option selected</li> <li>Ta=-40 to +85°C</li> </ul>	2.7 to 3.6		2.4	25	μΑ
	IDDHOLD(9)		HOLD mode  • Watchdog timer active	4.5 to 5.5		3.4	10	
	IDDHOLD(10)		• Ta=-10 to +50°C	2.7 to 3.6		1.7	6.0	
	IDDHOLD(11)		HOLD mode	4.5 to 5.5		3.4	42	
	IDDHOLD(12)	Watchdog timer active     Ta=-40 to +85°C		2.7 to 3.6		1.7	27	
		HOLD mode	4.5 to 5.5		110	160		
N 10 1 70	IDDHOLD(14)		Comparator active     (IN+=V <sub>DD</sub> , IN-=V <sub>SS</sub> )	2.7 to 3.6		65	100	

Note 10-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

## **F-ROM Programming Characteristics** at Ta = +10 to +55°C, $V_{SS}1 = 0V$

Parameter Symbol	Symbol Pin/Remarks		Conditions		Specification			
	FIII/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Onboard programming current	IDDFW	V <sub>DD</sub> 1	Microcontroller consumption current is excluded.	3.0 to 5.5		5	10	mA
Programming	tFW(1)		Erase operation	3.0 to 5.5		20	30	ms
time	tFW(2)		Programming operation	3.0 10 5.5		40	60	μs

## Power Pin Treatment Recommendations (VDD1, VSS1)

Connect bypass capacitors that meet the following conditions between the  $V_{DD}1$  and  $V_{SS}1$  pins:

- Connect among the V<sub>DD</sub>1 and V<sub>SS</sub>1 pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as equal as possible (L1=L1', L2=L2').
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1µF.

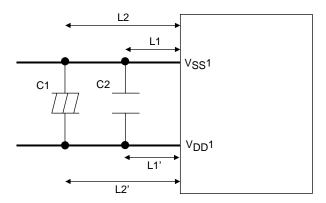
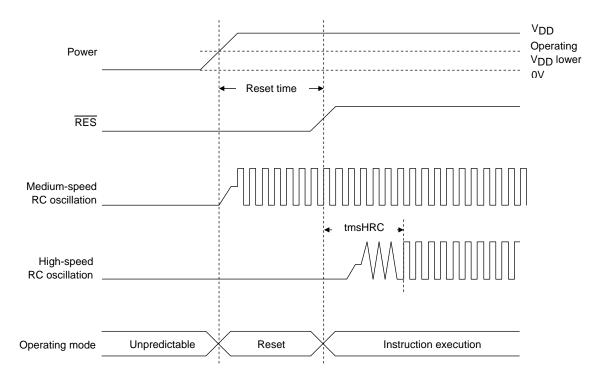
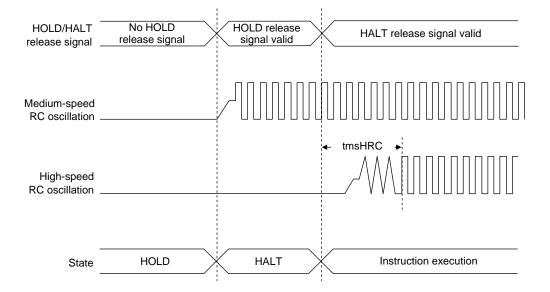




Figure 1 AC Timing Measurement Point

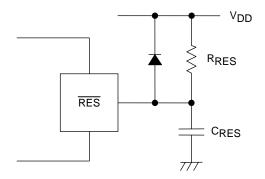


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 2 Oscillation Stabilization Times



#### Note:

The external peripheral circuit differs depending on the way in which the power-on reset and low-voltage detection reset functions are used. Refer to the Chapter, entitled "Reset Function", of the user's manual.

Figure 3 Sample Reset Circuit

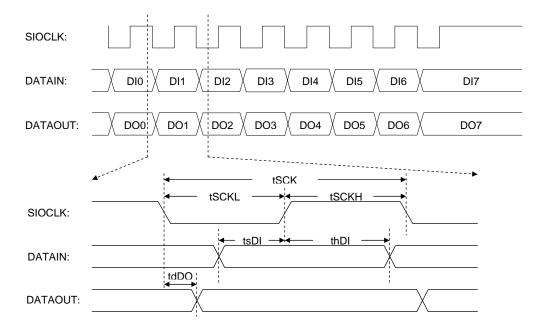


Figure 4 Serial I/O Waveforms

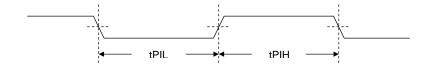


Figure 5 Pulse Input Timing Signal Waveform

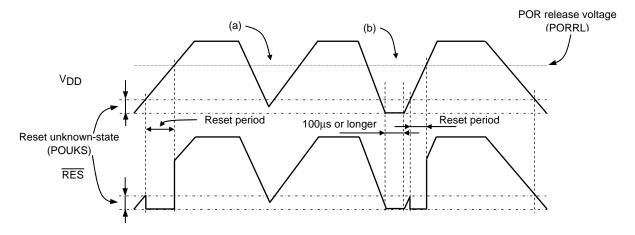


Figure 6 Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with RRES Pull-up Resistor Only)

- The POR circuit generates a reset signal only when the power voltage is raised from the VSS level.
- No stable reset signal is generated if power is turned on again when the power voltage does not go down to the VSS level as shown in (a). If this case is anticipated, use the LVD function as explained below or configure an external reset circuit.
- A reset is effected only when power is turned on again after the power voltage goes down to and remains at the VSS level for 100µs or longer as shown in (b).

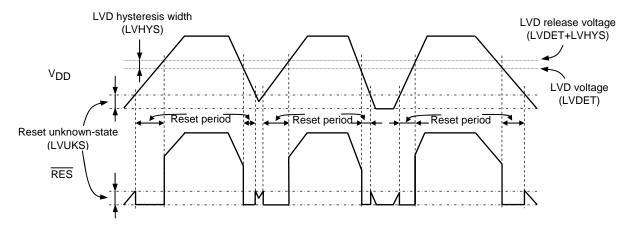


Figure 7 Example of POR + LVD Mode Waveforms (at Reset Pin with RRESS Pull-up Resistor Only)

- A reset is effected both when power is turned on and when it goes down.
- The hysteresis width (LVHYS) is introduced in the LVD circuit to prevent the iterations of the IC entering and exiting the reset state near the detection threshold level.

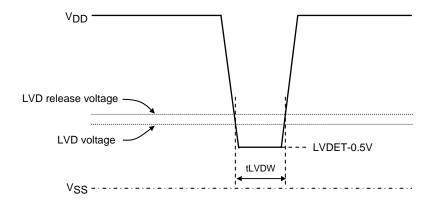


Figure 8 Minimum Low Voltage Detection Width (Example of Short Interruption of Power/Power Fluctuation Waveform)

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