# Single 2-Input NOR Gate/ CMOS Logic Level Shifter

# LSTTL-Compatible Inputs

The MC74VHC1GT02 is a single gate 2–input NOR fabricated with silicon gate CMOS technology.

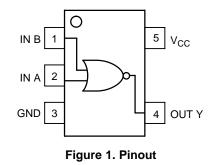
The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT02 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT02 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when  $V_{CC} = 0$  V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

#### Features

- High Speed:  $t_{PD} = 4.7$  ns (Typ) at  $V_{CC} = 5$  V
- Low Power Dissipation:  $I_{CC} = 1 \ \mu A$  (Max) at  $T_A = 25^{\circ}C$
- TTL–Compatible Inputs:  $V_{IL} = 0.8 V$ ;  $V_{IH} = 2 V$
- CMOS–Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC}$  @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 65
- Pb–Free Packages are Available



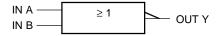
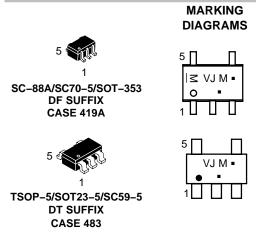


Figure 2. Logic Symbol



## **ON Semiconductor®**

http://onsemi.com



VJ = Device Code

M = Date Code\*

= Pb–Free Package

(Note: Microdot may be in either location) \*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT					
1	IN B				
2	IN A				
3	GND				
4	OUT Y				
5	V <sub>CC</sub>				

#### **FUNCTION TABLE**

Inp	uts	Output
Α	в	Y
L	L	Н
L	Н	L
н	L	L
Н	Н	L

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

#### MAXIMUM RATINGS

Symbol	Char	acteristics	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage		-0.5 to +7.0	V
V <sub>OUT</sub>	DC Output Voltage	V <sub>CC</sub> = 0 High or Low State	–0.5 to 7.0 –0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current		-20	mA
I <sub>OK</sub>	Output Diode Current	V <sub>OUT</sub> < GND; V <sub>OUT</sub> > V <sub>CC</sub>	+20	mA
I <sub>OUT</sub>	DC Output Current, per Pin		+25	mA
I <sub>CC</sub>	DC Supply Current, $V_{CC}$ and GND		+50	mA
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C
ΤL	Lead Temperature, 1 mm from Case for	or 10 Seconds	260	°C
ТJ	Junction Temperature Under Bias		+ 150	°C
$\theta_{JA}$	Thermal Resistance	SC70–5/SC–88A/SOT–353 (Note 1) SOT23–5/TSOP–5/SC59–5	350 230	°C/W
PD	Power Dissipation in Still Air at 85°C	SC70–5/SC–88A/SOT–353 SOT23–5/TSOP–5/SC59–5	150 200	mW
MSL	Moisture Sensitivity		Level 1	
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
I <sub>LATCHUP</sub>	Latchup Performance A	bove V <sub>CC</sub> and Below GND at 125°C (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.

2. Tested to EIA/JESD22-A114-A.

3. Tested to EIA/JESD22-A115-A.

4. Tested to JESD22-C101-A.

5. Tested to EIA/JESD78.

### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Characteristics	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	3.0	5.5	V
V <sub>IN</sub>	DC Input Voltage	0.0	5.5	V
V <sub>OUT</sub>	DC Output Voltage V <sub>CC</sub> = 0 High or Low State	0.0 0.0	5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time $\begin{array}{c} V_{CC} = 3.3 \ V \pm 0.3 \ V \\ V_{CC} = 5.0 \ V \pm 0.5 \ V \end{array}$	0 0	100 20	ns/V

#### DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

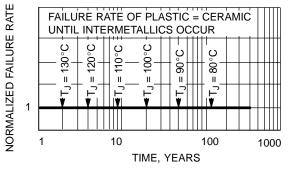


Figure 3. Failure Rate vs. Time Junction Temperature

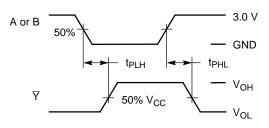
## DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> ≤	85°C	<b>−55</b> ≤ T <sub>A</sub>	≤ 125°C		
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High–Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0			1.4 2.0 2.0		1.4 2.0 2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \ \mu\text{A}$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V <sub>OL</sub>	Maximum Low–Level Output Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \ \mu\text{A}$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I <sub>IN</sub>	Maximum Input Leakage Current	$V_{IN} = 5.5 V \text{ or GND}$	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		20		40	μΑ
I <sub>CCT</sub>	Quiescent Supply Current	Per Input: $V_{IN} = 3.4 V$ Other Input: $V_{CC}$ or GND	5.5			1.35		1.50		1.65	mA
I <sub>OFF</sub>	Power Off Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		10	μΑ

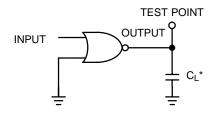
## AC ELECTRICAL CHARACTERISTICS Input $t_{f}$ = $t_{f}$ = 3.0 ns

				T <sub>A</sub> = 25	°C	T <sub>A</sub> ≤	85°C	–55 ≤ T <sub>A</sub>	≤ 125°C	
Symbol	Parameter	Test Conditions	Mir	Тур	Max	Min	Мах	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Y	$V_{CC} = 3.3 \pm 0.3 V$ $C_L = 15$ $C_L = 50$		4.5 5.8	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_{L} = 15$ $C_{L} = 50$	pF pF	3.0 3.8	6.7 7.7		7.5 8.5		8.5 9.5	
C <sub>IN</sub>	Maximum Input Capacitance			5.5	10		10		10	pF
					Typical	@ 25°C	;, V <sub>CC</sub> =	: 5.0 V		
C <sub>PD</sub>	D Power Dissipation Capacitance (Note 6)					11				pF

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$ . C<sub>PD</sub> is used to determine the no–load dynamic power consumption;  $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$ .







\*Includes all probe and jig capacitance

Figure 5. Test Circuit

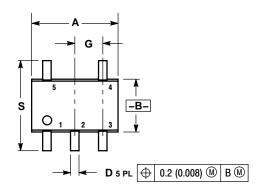
#### **ORDERING INFORMATION**

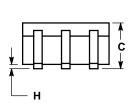
Device	Package	Shipping <sup>†</sup>
MC74VHC1GT02DFT1	SC70-5/SC-88A/SOT-353	
M74VHC1GT02DFT1G	SC70–5/SC–88A/SOT–353 (Pb–Free)	
MC74VHC1GT02DFT2	SC70-5/SC-88A/SOT-353	
M74VHC1GT02DFT2G	SC70-5/SC-88A/SOT-353 (Pb-Free)	3000/Tape & Reel
MC74VHC1GT02DTT1	SOT23-5/TSOP-5/SC59-5	
M74VHC1GT02DTT1G	SOT23–5/TSOP–5/SC59–5 (Pb–Free)	

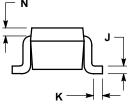
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### PACKAGE DIMENSIONS

SC-88A, SOT-353, SC-70 CASE 419A-02 ISSUE J



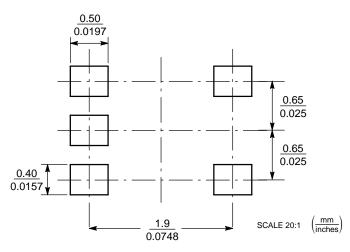




NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. 419A-01 OBSOLETE. NEW STANDARD 419A-02. 4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.071	0.087	1.80	2.20	
В	0.045	0.053	1.15	1.35	
C	0.031	0.043	0.80	1.10	
D	0.004	0.012	0.10	0.30	
G	0.026	BSC	0.65 BSC		
Н		0.004		0.10	
J	0.004	0.010	0.10	0.25	
K	0.004	0.012	0.10	0.30	
Ν	0.008 REF		0.20	REF	
S	0.079	0.087	2.00	2.20	

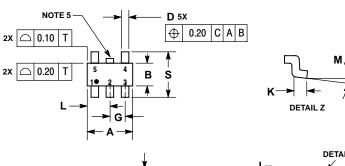
**SOLDERING FOOTPRINT\*** 

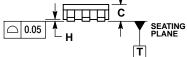


\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

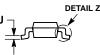
#### PACKAGE DIMENSIONS

TSOP-5 CASE 483-02 ISSUE F





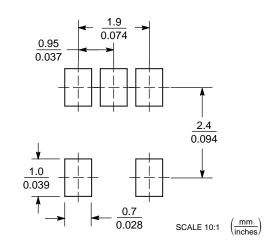




- NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- 2. 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS
- OF BASE MATERIAL. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION, TRIMMED LEAD NOT TO 5 EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS					
DIM	MIN MAX					
Α	3.00	BSC				
В	1.50	BSC				
С	0.90	1.10				
D	0.25	0.50				
G	0.95	0.95 BSC				
Н	0.01	0.10				
J	0.10	0.26				
к	0.20	0.60				
L	1.25	1.55				
М	0° 10°					
S	2.50	3.00				

#### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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