NL37WZ17

Triple Noninverting Schmitt-Trigger Buffer

The NL37WZ17 is a high performance buffer with Schmitt−Trigger inputs operating from a 1.65 to 5.5 V supply.

The NL37WZ17 can be used as a line receiver which will receive slow input signals. The NL37WZ17 is capable of transforming slowly changing input signals into sharply defined, jitter−free output signals. In addition, it has a greater noise margin than conventional inverters. The NL37WZ17 has hysteresis between the positive−going and the negative−going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- LVTTL Compatible − Interface Capability with 5 V TTL Logic with V_{CC} = 3 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Current Drive Capability is 24 mA at the Outputs
- Chip Complexity: FET = 94
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

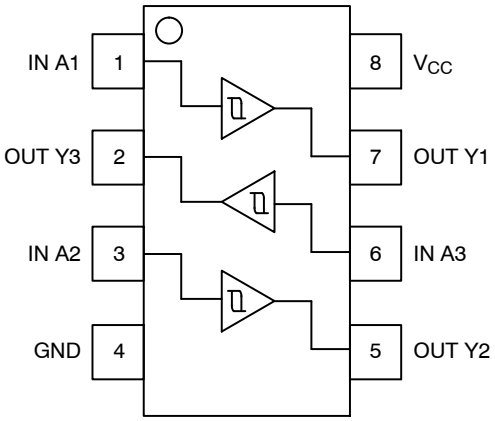

Figure 1. Pinout

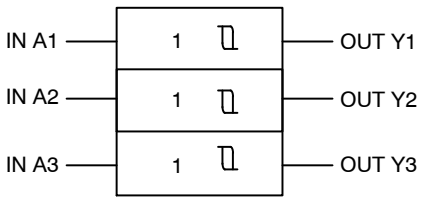

Figure 2. Logic Symbol

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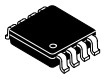
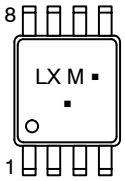
MARKING DIAGRAM



US8
US SUFFIX
CASE 493



LX = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

PIN ASSIGNMENT

Pin	Function
1	IN A1
2	OUT Y3
3	IN A2
4	GND
5	OUT Y2
6	IN A3
7	OUT Y1
8	V_{CC}

FUNCTION TABLE

A Input	$\overline{Y}$ Output
L	L
H	H

ORDERING INFORMATION

Device	Package	Shipping†
NL37WZ17USG	US8 (Pb−Free)	3000/Tape & Reel
NLV37WZ17USG*	US8 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_I	DC Input Voltage	$-0.5 \le V_I \le +7.0$	V
V_O	DC Output Voltage Output in Z or LOW State (Note 1)	$-0.5 \le V_O \le +7.0$	V
I_{IK}	DC Input Diode Current V_I < GND	−50	mA
I_{OK}	DC Output Diode Current V_O < GND	−50	mA
I_O	DC Output Sink Current	±50	mA
I_{CC}	DC Supply Current per Supply Pin	±100	mA
I_{GND}	DC Ground Current per Ground Pin	±100	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2)	333	°C/W
P_D	Power Dissipation in Still Air at 85°C	200	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	 > 2000 > 200 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	 2.3 1.5	 5.5 5.5	V
V_I	Input Voltage (Note 6)	0	5.5	V
V_O	Output Voltage (HIGH or LOW State)	0	5.5	V
T_A	Operating Free−Air Temperature	−40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	 0 0 0	 No Limit No Limit No Limit	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	−40°C ≤ T_A ≤ 85°C Min	−40°C ≤ T_A ≤ 85°C Max	Units
V_{T+}	Positive Input Threshold Voltage		2.3 2.7 3.0 4.5 5.5	1.0 1.2 1.3 1.9 2.2	1.5 1.7 1.9 2.7 3.3	1.8 2.0 2.2 3.1 3.6	1.0 1.2 1.3 1.9 2.2	1.8 2.0 2.2 3.1 3.6	V
V_{T-}	Negative Input Threshold Voltage		2.3 2.7 3.0 4.5 5.5	0.4 0.5 0.6 1.0 1.2	0.75 0.87 1.0 1.5 1.9	1.15 1.4 1.5 2.0 2.3	0.4 0.5 0.6 1.0 1.2	1.15 1.4 1.5 2.0 2.3	V
V_H	Input Hysteresis Voltage		2.3 2.7 3.0 4.5 5.5	0.25 0.3 0.4 0.6 0.7	0.75 0.83 0.93 1.2 1.4	1.1 1.15 1.2 1.5 1.7	0.25 0.3 0.4 0.6 0.7	1.1 1.15 1.2 1.5 1.7	V
V_{OH}	High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA I_{OH} = −3 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V_{CC} 1.52 2.1 2.4 2.7 2.5 4.0		V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.2 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0			1		10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = 5.5 V or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	−40°C ≤ T_A ≤ 85°C Min	−40°C ≤ T_A ≤ 85°C Max	Units
t_{PLH} t_{PHL}	Propagation Delay Input A to Y (Figures 3 and 4)	R_L = 1 MΩ, C_L = 15 pF	2.5 ± 0.2	1.8	4.3	7.4	1.8	8.1	ns
		R_L = 1 MΩ, C_L = 15 pF R_L = 500 Ω, C_L = 50 pF	3.3 ± 0.3	1.5 1.8	3.3 4.0	5.0 5.0	1.5 1.8	5.5 6.6	
		R_L = 1 MΩ, C_L = 15 pF R_L = 500 Ω, C_L = 50 pF	5.0 ± 0.5	1.0 1.2	2.7 3.2	4.1 4.9	1.0 1.2	4.5 5.4	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 7)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC} 10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	9 11	pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no−load dynamic power consumption; P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC}.

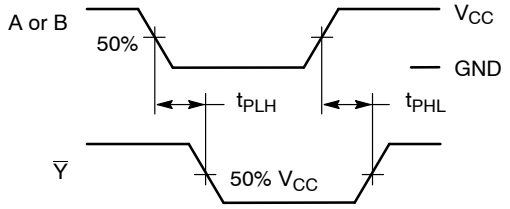
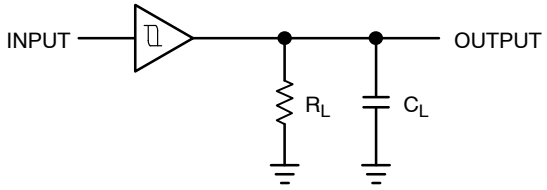


Figure 3. Switching Waveforms



A 1−MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

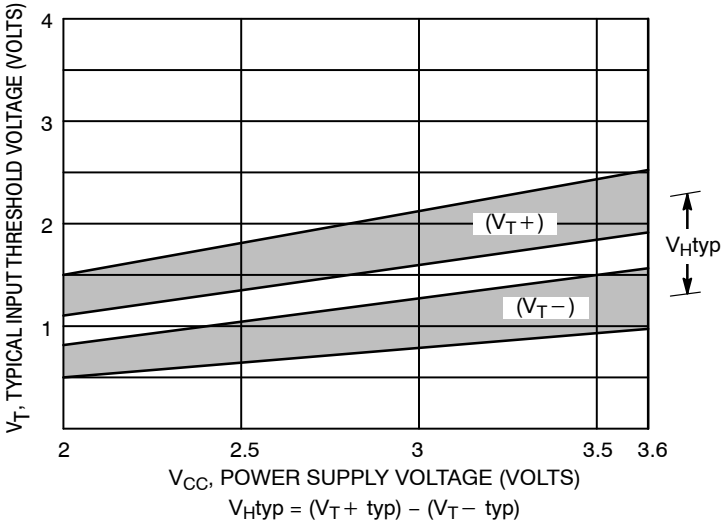
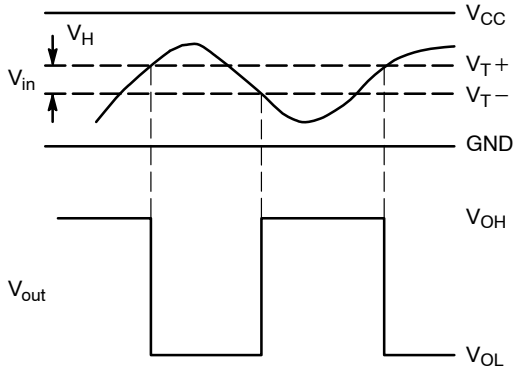
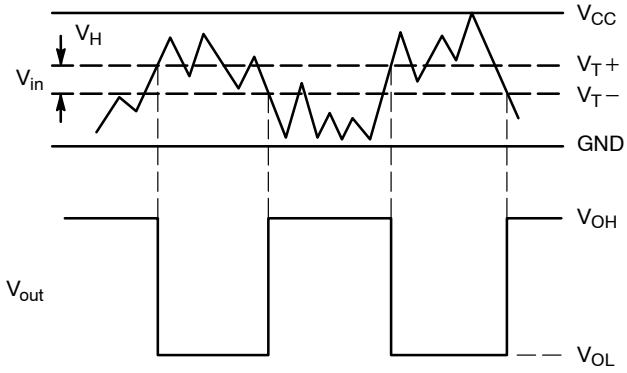


Figure 5. Typical Input Threshold, V_T+, V_T- versus Power Supply Voltage



(a) A Schmitt−Trigger Squares Up Inputs With Slow Rise and Fall Times

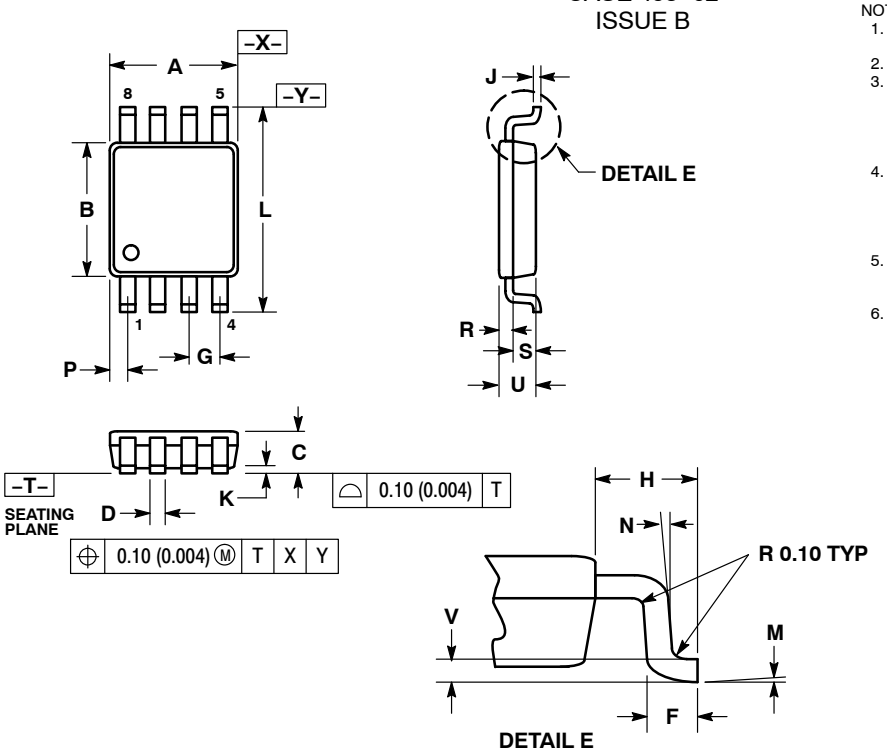


(b) A Schmitt−Trigger Offers Maximum Noise Immunity

Figure 6. Typical Schmitt−Trigger Applications

PACKAGE DIMENSIONS

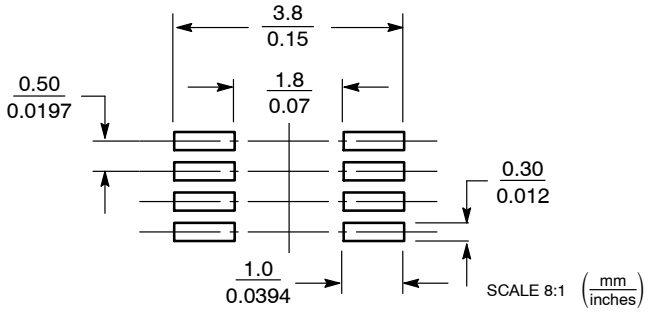
US8
CASE 493−02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055”) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSION. INTER−LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055”) PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076−0.0203 MM. (300−800 “).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 “).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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