Power MOSFET

–20 V, –8.2 A, Single P–Channel, 2.0x2.0x0.55 mm μCool [™] UDFN Package

Features

- UDFN Package with Exposed Drain Pads for Excellent Thermal Conduction
- Low Profile UDFN 2.0x2.0x0.55 mm for Board Space Saving
- Ultra Low R_{DS(on)}
- ESD Diode–Protected Gate
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Optimized for Power Management Applications for Portable Products, such as Cell Phones, Media Tablets, PMP, DSC, GPS, and Others
- Battery Switch
- High Side Load Switch

MAXIMUM RATINGS (T_J = 25° C unless otherwise stated)

Pa	Symbol	Value	Unit		
Drain-to-Source Voltage			V _{DSS}	-20	V
Gate-to-Source Vol	tage		V _{GS}	±8.0	V
Continuous Drain	Steady	$T_A = 25^{\circ}C$	I _D	-8.2	А
Current (Note 1) Continuous Drain	State	$T_A = 85^{\circ}C$		-5.9	
Current (Note 1)	t ≤ 5 s	T _A = 25°C		-12.2	
Power Dissipa- tion (Note 1)	Steady State	T _A = 25°C	PD	1.7	W
	t ≤ 5 s	T _A = 25°C		3.8	
Continuous Drain	,	T _A = 25°C	I _D	-5.1	А
Current (Note 2)	State	T _A = 85°C		-3.7	
Power Dissipation (Power Dissipation (Note 2)		PD	0.7	W
Pulsed Drain Curre	nt	tp = 10 μs	I _{DM}	-25	А
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to 150	°C
ESD (HBM, JESD22–A114)			V _{ESD}	2000	V
Source Current (Body Diode) (Note 2)			۱ _S	-1.7	А
Lead Temperature t (1/8" from case for		g Purposes	ΤL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions may affect device reliability.
Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

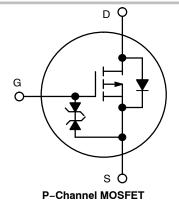
 Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.



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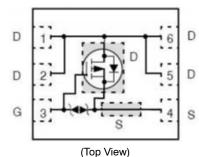
MOSFET						
V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX				
	18 mΩ @ –4.5 V					
–20 V	25 mΩ @ –2.5 V	-8.2 A				
	50 mΩ @ −1.8 V	0.271				
	90 mΩ @ −1.5 V					





S MARKING DIAGRAM UDFN6 $(\mu COOL^{TM})$ CASE 517BG AE = Specific Device Code M = Date Code • = Pb-Free Package (*Note: Microdot may be in either location)





ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	R_{\thetaJA}	72	
Junction-to-Ambient – t \leq 5 s (Note 3)	R_{\thetaJA}	33	°C/W
Junction-to-Ambient – Steady State min Pad (Note 4)	R_{\thetaJA}	189	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

4. Surface-mounted on FR4 board using the minimum recommended pad size of 30 mm², 2 oz. Cu.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Co	ndition	Min	Тур	Max	Units
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I	_D = –250 μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	I _D = -250 μA	∧, ref to 25°C		+10		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -20 V	$T_J = 25^{\circ}C$			-1.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V	/ _{GS} = ±5.0 V			±5	μΑ
ON CHARACTERISTICS (Note 5)							

-1.0 V Gate Threshold Voltage $V_{GS} = V_{DS}$, $I_D = -250 \ \mu A$ -0.4 V_{GS(TH)} Negative Threshold Temp. Coefficient V_{GS(TH)}/T_J 3.0 mV/°C Drain-to-Source On Resistance $V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -7.0 \text{ A}$ R_{DS(on)} 14.6 18 mΩ $V_{GS} = -2.5 \text{ V}, \text{ I}_{D} = -5.0 \text{ A}$ 19 25 $V_{GS} = -1.8 \text{ V}, I_D = -3.0 \text{ A}$ 25 50 $V_{GS} = -1.5 \text{ V}, \text{ I}_{D} = -1.0 \text{ A}$ 40 90 Forward Transconductance $V_{DS} = -5 \text{ V}, I_D = -3.0 \text{ A}$ 40 s **9**FS

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}		2240	pF
Output Capacitance	C _{OSS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = -15 V	240	
Reverse Transfer Capacitance	C _{RSS}		210	
Total Gate Charge	Q _{G(TOT)}		28	nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = -4.5 V, V _{DS} = -15 V; I _D = -4.0 A	1.0	
Gate-to-Source Charge	Q _{GS}	$I_{\rm D} = -4.0$ A	2.9	
Gate-to-Drain Charge	Q _{GD}		8.8	

SWITCHING CHARACTERISTICS, VGS = 4.5 V (Note 6)

Turn-On Delay Time	t _{d(ON)}		8.6	ns
Rise Time	t _r	V _{GS} = -4.5 V, V _{DD} = -15 V,	15	
Turn-Off Delay Time	t _{d(OFF)}	$I_D = -4.0 \text{ A}, R_G = 1 \Omega$	150	
Fall Time	t _f		88	

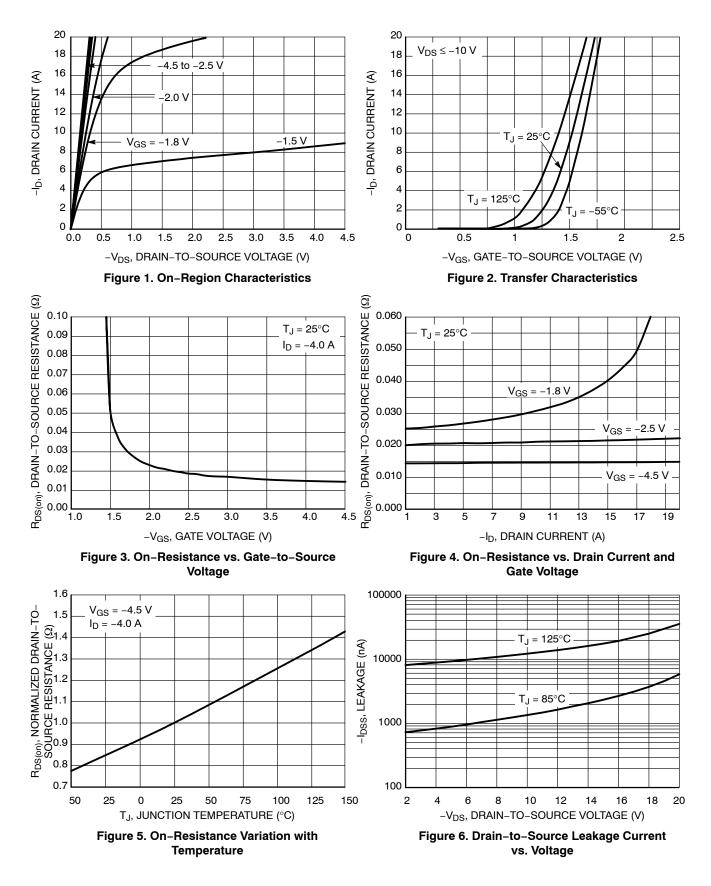
DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.0 A	$T_J = 25^{\circ}C$	0.63	1.0	V
		I _S = –1.0 A	$T_J = 125^{\circ}C$	0.50		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dls/dt = 100 A/μs, I _S = −1.0 A		26.1		ns
Charge Time	t _a			10.2		
Discharge Time	t _b			15.9		
Reverse Recovery Charge	Q _{RR}			12		nC

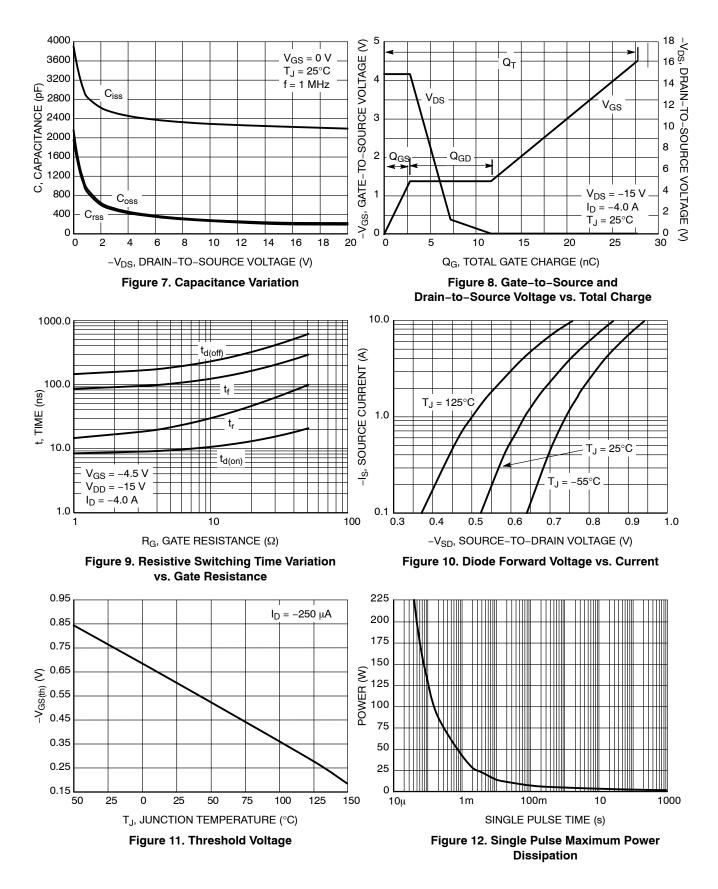
5. Pulse Test: pulse width \leq 300 μ s, duty cycle \leq 2%.

6. Switching characteristics are independent of operating junction temperatures.

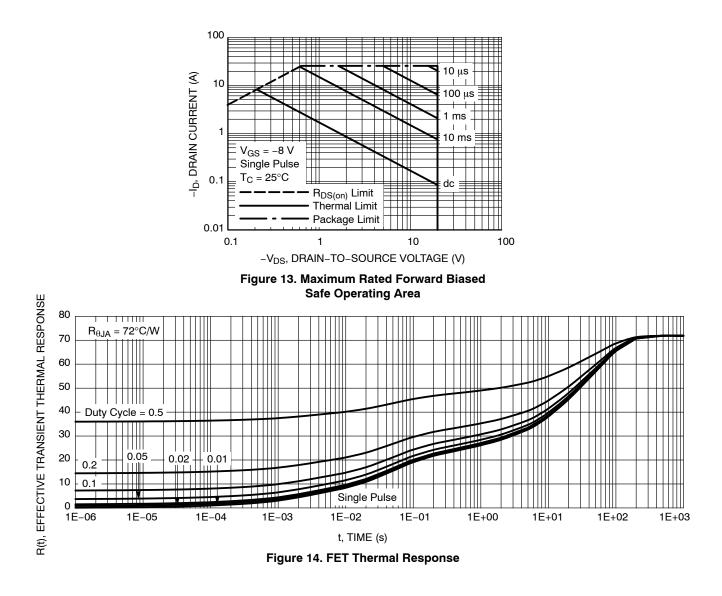
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



DEVICE ORDERING INFORMATION

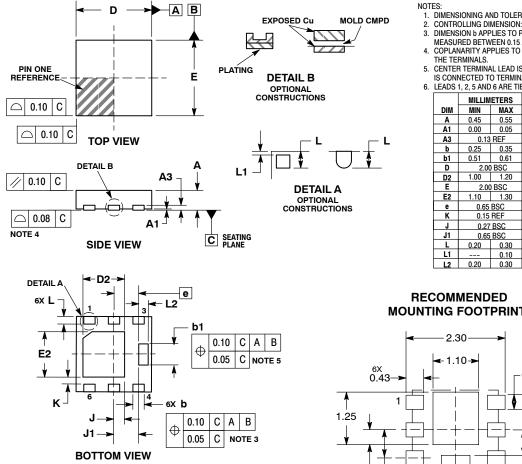
Device	Package	Shipping [†]
NTLUS3A18PZCTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUS3A18PZCTBG	UDFN6 (Pb-Free)	3000 / Tape & Reel
NTLUS3A18PZCTCG	UDFN6 (Pb-Free)	3000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

UDFN6 2x2, 0.65P CASE 517BG

ISSUE A



1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

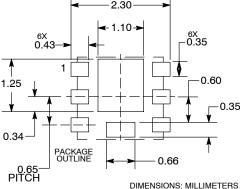
CONTROLLING DIMENSION: MILLIMETERS. DIMENSION b APPLIES TO PLATED TERMINAL AND IS

- MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS
- THE TERMINALS

CENTER TERMINAL LEAD IS OPTIONAL. CENTER TERMINAL IS CONNECTED TO TERMINAL LEAD # 4. LEADS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

. LEADS 1, 2, 5 AND 6 ARE TIED								
		MILLIM	MILLIMETERS					
	DIM	MIN	MAX					
	Α	0.45	0.55					
	A1	0.00	0.05					
	A3	0.13	REF					
	b	0.25	0.35					
	b1	0.51	0.61					
	D	2.00 BSC						
	D2	1.00	1.20					
	Е	2.00	2.00 BSC					
	E2	1.10	1.30					
	e	0.65	0.65 BSC					
	K	0.15	0.15 REF					
	J	0.27 BSC						
	J1	0.65 BSC						
	L	0.20	0.30					
	L1		0.10					
	1.2	0.20	0.30					

RECOMMENDED **MOUNTING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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