

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π-MOSIII)

2SK2611

DC-DC Converter, Relay Drive and Motor Drive Applications

Unit: mm

- Low drain-source ON-resistance : $R_{DS(ON)} = 1.2 \Omega$ (typ.)
- High forward transfer admittance : $|Y_{fs}| = 7.0 S$ (typ.)
- Low leakage current : $I_{DSS} = 100 \mu A$ (max) ($V_{DS} = 720 V$)
- Enhancement-mode : $V_{th} = 2.0$ to $4.0 V$ ($V_{DS} = 10 V$, $I_D = 1 mA$)

Absolute Maximum Ratings ($T_a = 25^\circ C$)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	900	V
Drain-gate voltage ($R_{GS} = 20 k\Omega$)		V_{DGR}	900	V
Gate-source voltage		V_{GSS}	± 30	V
Drain current	DC (Note 1)	I_D	9	A
	Pulse (Note 1)	I_{DP}	27	A
Drain power dissipation ($T_c = 25^\circ C$)		P_D	150	W
Single pulse avalanche energy (Note 2)		E_{AS}	663	mJ
Avalanche current		I_{AR}	9	A
Repetitive avalanche energy (Note 3)		E_{AR}	15	mJ
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature range		T_{stg}	-55 to 150	$^\circ C$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	0.833	$^\circ C / W$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	50	$^\circ C / W$

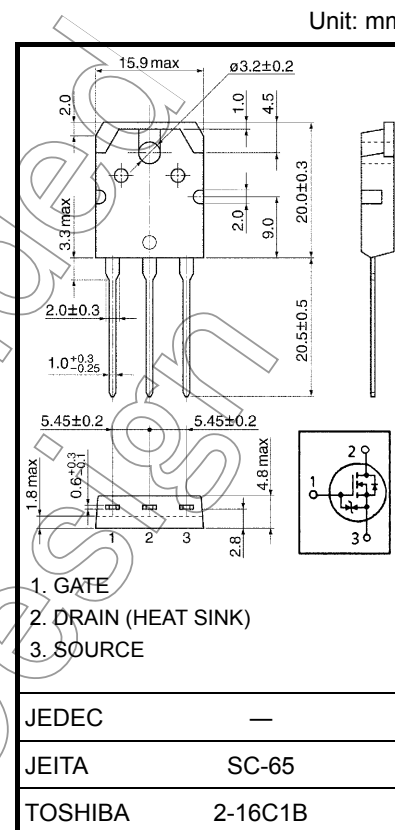
Note 1: Please use devices on condition that the channel temperature is below $150^\circ C$.

Note 2: $V_{DD} = 90 V$, $T_{ch} = 25^\circ C$ (initial), $L = 15 mH$, $R_G = 25 \Omega$, $I_{AR} = 9 A$

Note 3: Repetitive rating: Pulse width limited by maximum channel temperature

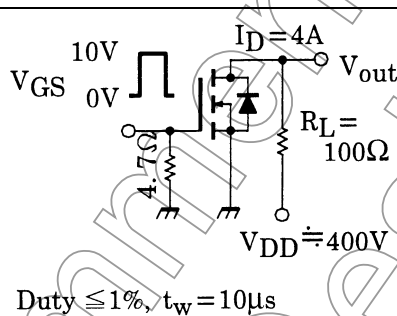
This transistor is an electrostatic sensitive device.

Please handle with caution.



Weight: 4.6 g (typ.)

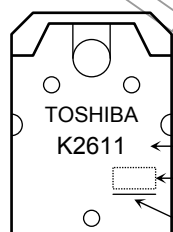
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 10	μA
Gate-source breakdown voltage		$V_{(BR) GSS}$	$I_G = \pm 10 \mu\text{A}, V_{DS} = 0 \text{ V}$	± 30	—	—	V
Drain cut-off current		I_{DSS}	$V_{DS} = 720 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR) DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	900	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	2.0	—	4.0	V
Drain-source ON-resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	—	1.2	1.4	Ω
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 15 \text{ V}, I_D = 4 \text{ A}$	3.0	7.0	—	S
Input capacitance		C_{iss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	2040	—	pF
Reverse transfer capacitance		C_{rss}		—	45	—	
Output capacitance		C_{oss}		—	190	—	
Switching time	Rise time	t_r		—	25	—	ns
	Turn-on time	t_{on}		—	60	—	
	Fall time	t_f		—	20	—	
	Turn-off time	t_{off}		—	95	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 9 \text{ A}$	—	58	—	nC
Gate-source charge		Q_{gs}		—	32	—	
Gate-drain ("miller") Charge		Q_{gd}		—	26	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	9	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	27	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 9 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.9	V
Reverse recovery time	t_{rr}	$I_{DR} = 9 \text{ A}, V_{GS} = 0 \text{ V}, dI_{DR} / dt = 100 \text{ A} / \mu\text{s}$	—	1.6	—	μs
Reverse recovery charge	Q_{rr}		—	20	—	μC

Marking



Part No. (or abbreviation code)

Lot No.

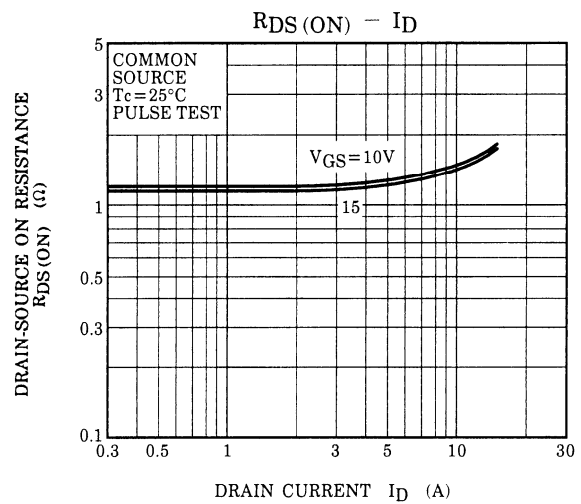
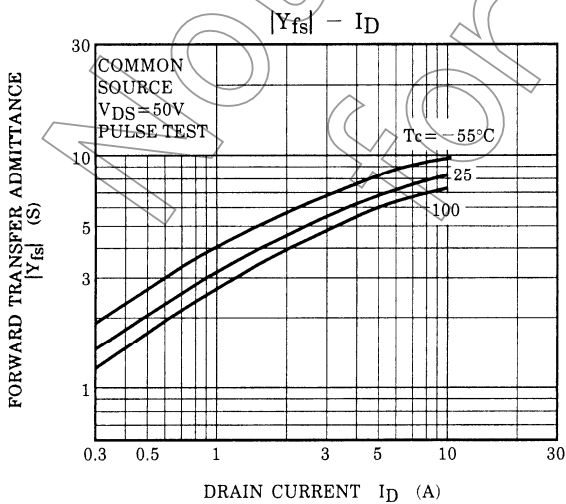
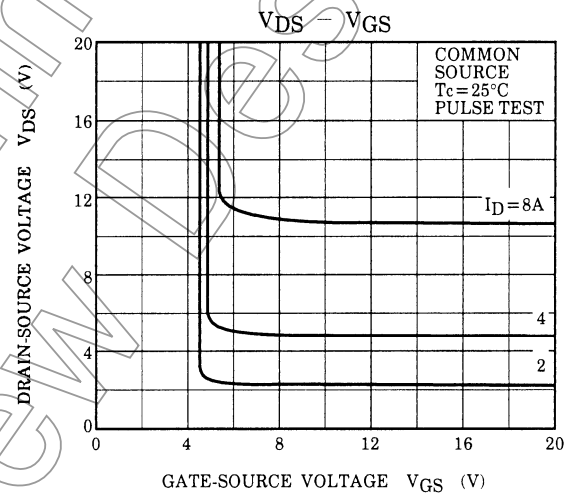
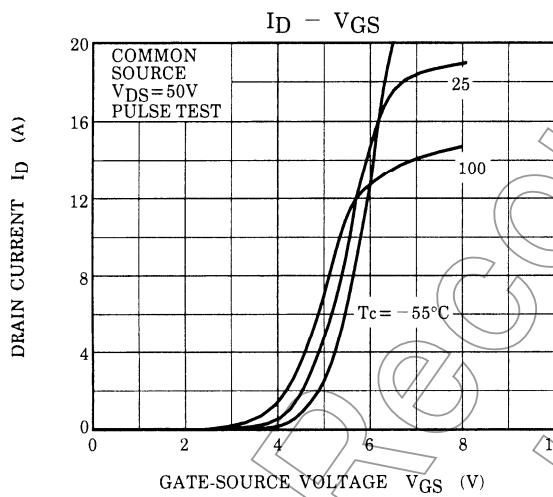
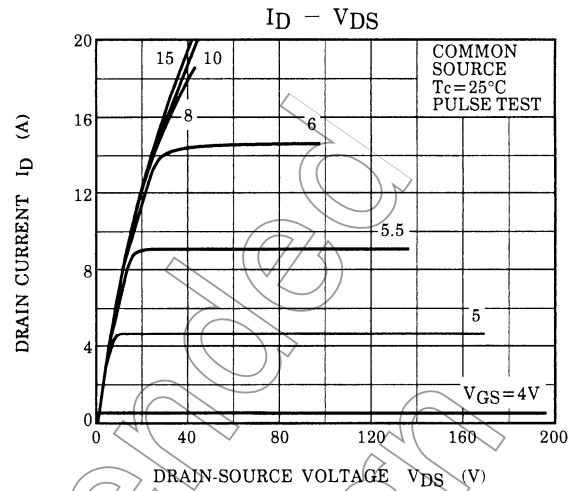
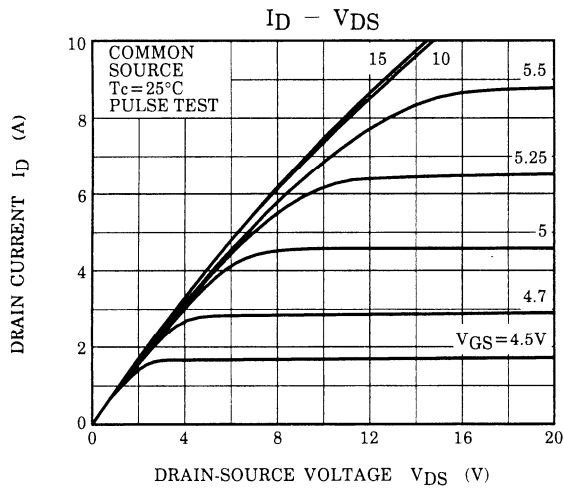
Note 4

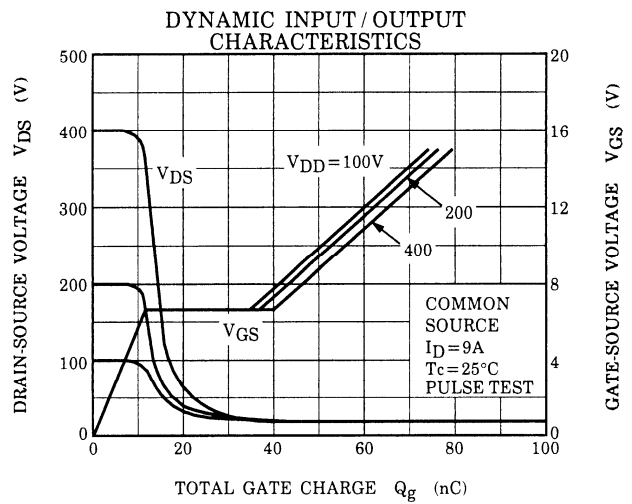
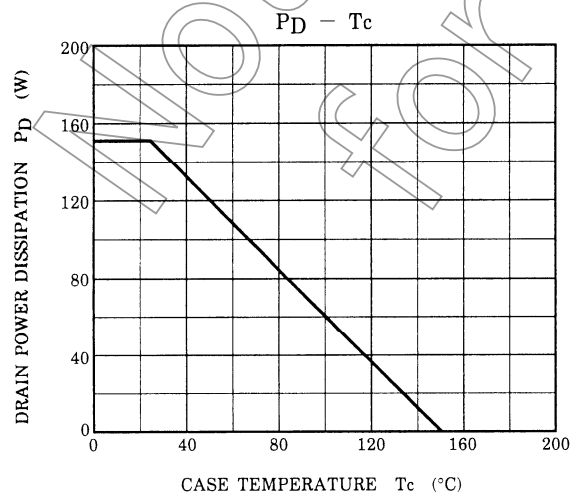
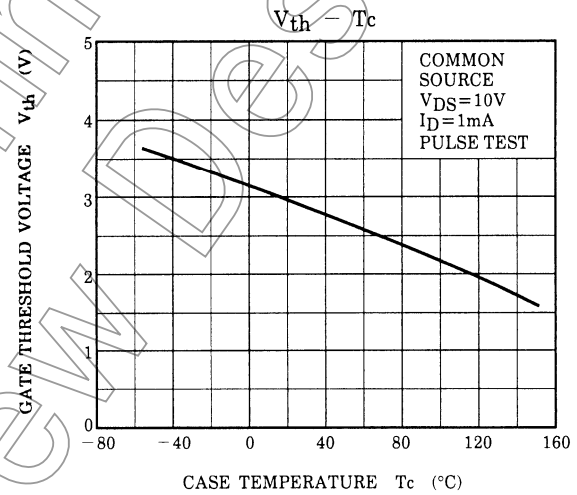
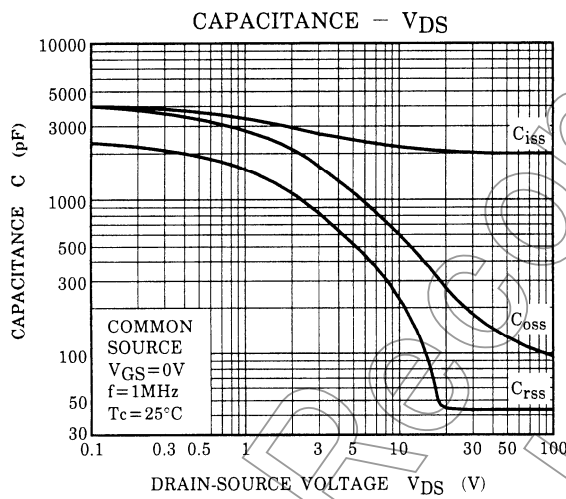
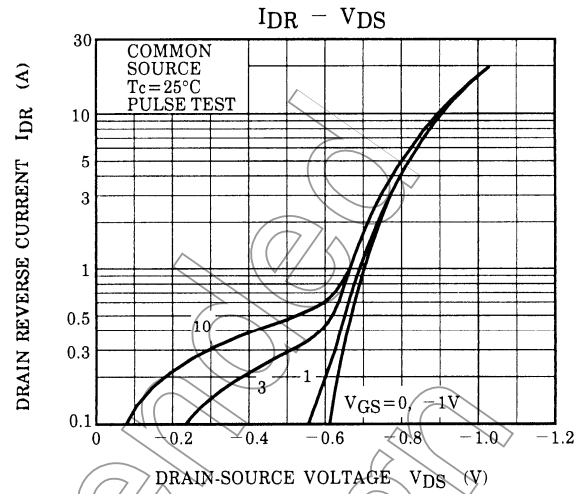
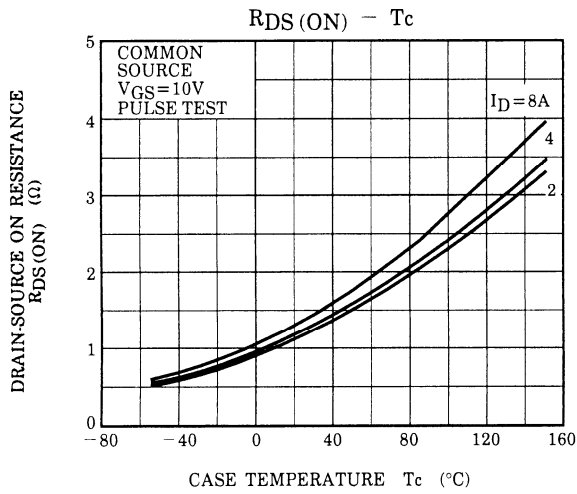
Note 4: A line under a Lot No. identifies the indication of product Labels.

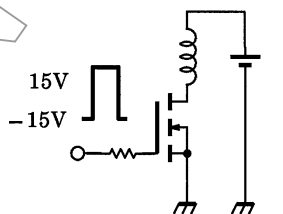
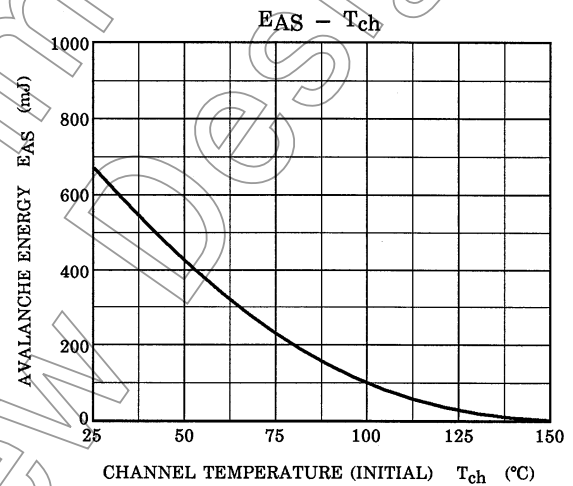
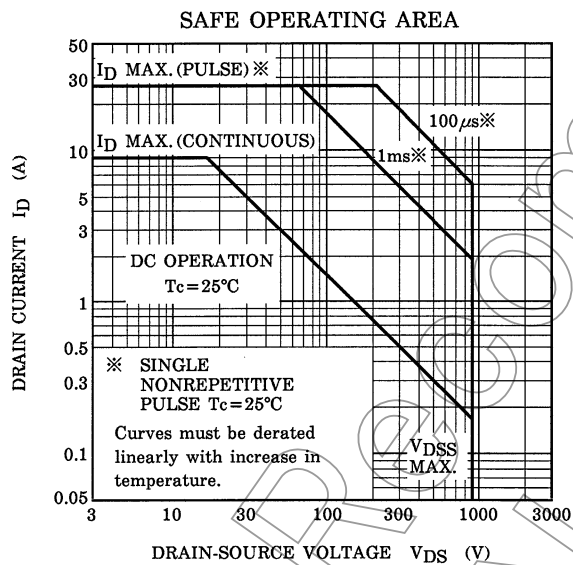
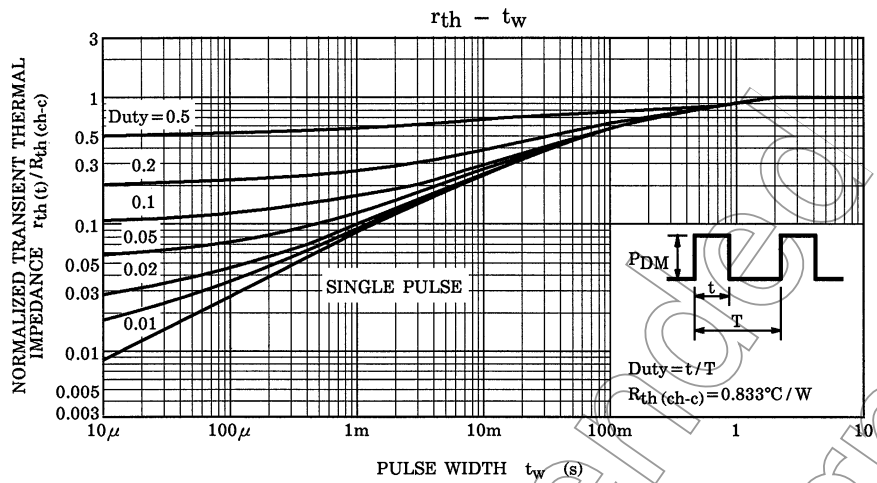
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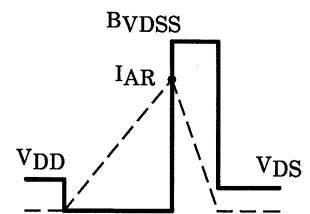
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TEST CIRCUIT



WAVE FORM

$$R_G = 25 \, \Omega$$

$$V_{DD} = 90 \, \text{V}, L = 15 \, \text{mH}$$

$$EAS = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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