

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

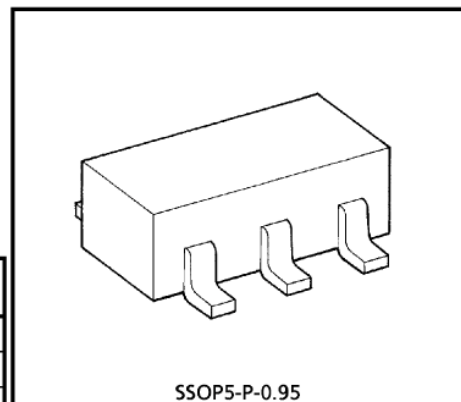
# TC4S71F

## 2 INPUT OR GATE

The TC4S71F is 2-input positive logic OR gates. Gate output with inverter buffer improve the input-output characteristics and even if the load capacitance increases, it can be stopped the change of propagation time.

### MAXIMUM RATINGS (Ta = 25°C)

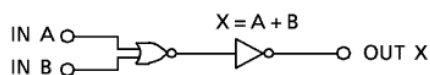
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V <sub>DD</sub>	V <sub>SS</sub> - 0.5 ~ V <sub>SS</sub> + 20	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> - 0.5 ~ V <sub>DD</sub> + 0.5	V
Output Voltage	V <sub>OUT</sub>	V <sub>SS</sub> - 0.5 ~ V <sub>DD</sub> + 0.5	V
DC Input Current	I <sub>IN</sub>	± 10	mA
Power Dissipation	P <sub>D</sub>	200	mW
Operating Temperature Range	T <sub>opr</sub>	-40 ~ 85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 ~ 150	°C
Lead Temperature (10s)	T <sub>L</sub>	260	°C



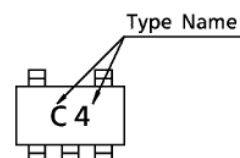
SSOP5-P-0.95

Weight : 0.016g (Typ.)

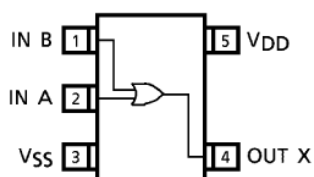
### LOGIC DIAGRAM



### MARKING



### PIN CONFIGURATION (TOP VIEW)



RECOMMENDED OPERATING CONDITIONS ( $V_{SS} = 0V$ )

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	
DC Supply Voltage	$V_{DD}$	—	3	—	18	V
Input Voltage	$V_{IN}$	—	0	—	$V_{DD}$	V

STATIC ELECTRICAL CHARACTERISTICS ( $V_{SS} = 0V$ )

CHARACTERISTIC	SYM-BOL	TEST CONDITION	$V_{DD}$ (V)	- 40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	$V_{OH}$	$ I_{OUT}  < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V	
			10	9.95	—	9.95	10.00	—	9.95	—		
			15	14.95	—	14.95	15.00	—	14.95	—		
Low-Level Output Voltage	$V_{OL}$	$ I_{OUT}  < 1\mu A$ $V_{IN} = V_{SS}$	5	—	0.05	—	0.00	0.05	—	0.05	V	
			10	—	0.05	—	0.00	0.05	—	0.05		
			15	—	0.05	—	0.00	0.05	—	0.05		
Output High Current	$I_{OH}$	$V_{OH} = 4.6V$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA	
		$V_{OH} = 2.5V$	5	-2.5	—	-2.1	-4.0	—	-1.7	—		
		$V_{OH} = 9.5V$	10	-1.5	—	-1.3	-2.2	—	-1.1	—		
		$V_{IN} = V_{DD}, V_{SS}$	15	-4.0	—	-3.4	-9.0	—	-2.8	—		
Output Low Current	$I_{OL}$	$V_{OL} = 0.4V$	5	0.61	—	0.51	1.2	—	0.42	—	mA	
		$V_{OL} = 0.5V$	10	1.5	—	1.3	3.2	—	1.1	—		
		$V_{OL} = 1.5V$	15	4.0	—	3.4	12.0	—	2.8	—		
		$V_{IN} = V_{SS}$										
Input High Voltage	$V_{IH}$	$V_{OUT} = 4.5V$	5	3.5	—	3.5	2.75	—	3.5	—	V	
		$V_{OUT} = 9.0V$	10	7.0	—	7.0	5.5	—	7.0	—		
		$V_{OUT} = 13.5V$	15	11.0	—	11.0	8.25	—	11.0	—		
		$ I_{OUT}  < 1\mu A$										
Input Low Voltage	$V_{IL}$	$V_{OUT} = 4.5V, 0.5V$	5	—	1.5	—	2.25	1.5	—	1.5	V	
		$V_{OUT} = 9.0V, 1.0V$	10	—	3.0	—	4.5	3.0	—	3.0		
		$V_{OUT} = 13.5V, 1.5V$	15	—	4.0	—	6.75	4.0	—	4.0		
		$ I_{OUT}  < 1\mu A$										
Input Current	H Level	$I_{IH}$	$V_{IH} = 18V$	18	—	0.1	—	$10^{-5}$	0.1	—	1.0	$\mu A$
	L Level	$I_{IL}$	$V_{IL} = 0V$	18	—	-0.1	—	$-10^{-5}$	-0.1	—	-1.0	
Quiescent Device Current	$I_{DD}$	$V_{IN} = V_{SS}, V_{DD}$ *	5	—	0.25	—	0.001	0.25	—	7.5	$\mu A$	
			10	—	0.5	—	0.001	0.5	—	15		
			15	—	1.0	—	0.002	1.0	—	30		

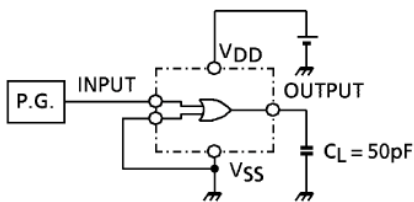
\* All valid input combinations.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $C_L = 50\text{pF}$ )

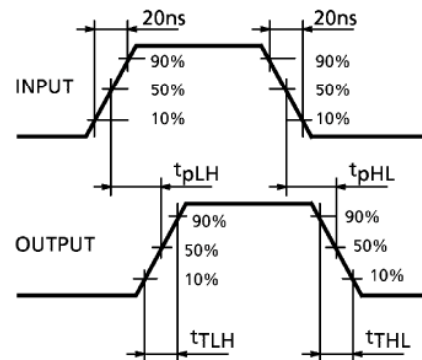
CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{DD}$ (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	$t_{TLH}$	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time (High to Low)	$t_{THL}$	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time	$t_{pLH}$	—	5	—	65	200	ns
			10	—	30	100	
			15	—	25	80	
Propagation Delay Time	$t_{pHL}$	—	5	—	65	200	ns
			10	—	30	100	
			15	—	25	80	
Input Capacitance	$C_{IN}$	—	—	5	7.5	pF	

**CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS**

TEST CIRCUIT

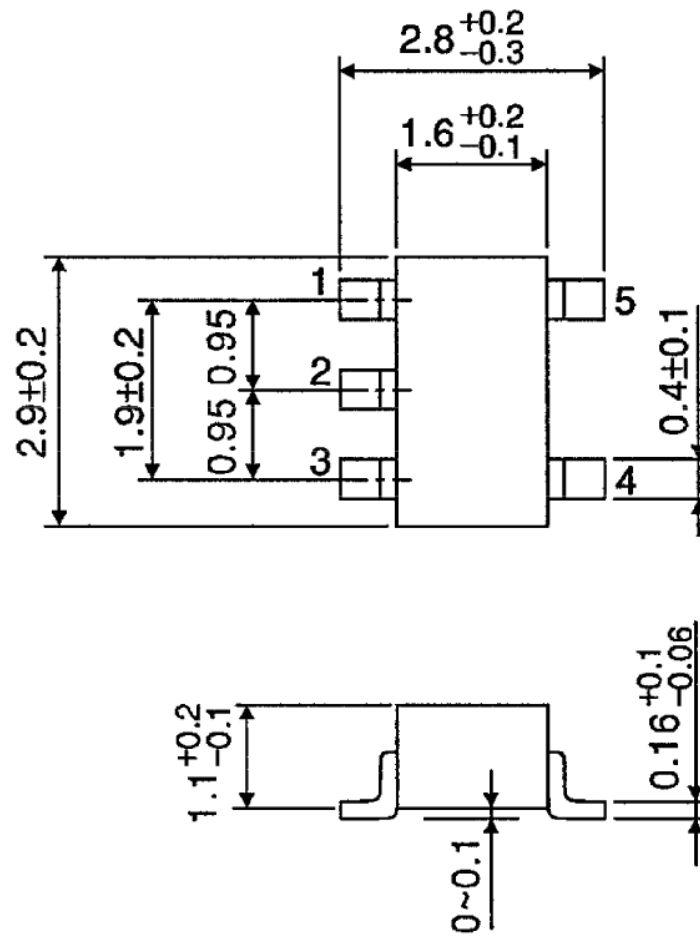


WAVEFORM



PACKAGE DIMENSIONS  
SSOP5-P-0.95

Unit : mm



Weight : 0.016g (Typ.)

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