

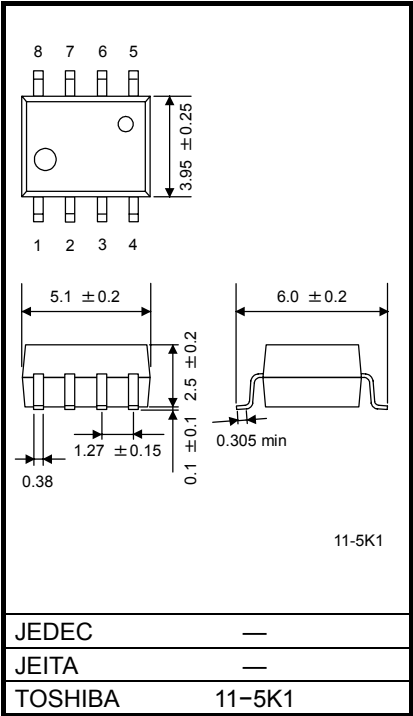
TLP2108

Isolated Bus Drivers
High Speed Line Receivers
Microprocessor System Interfaces

The Toshiba TLP2108 consists of GaAlAs light emitting diodes and integrated high-gain, high-speed photodetectors.
The TLP2108 is housed in the SO8 package.
The photodetector has a totem-pole output stage that can source and sink current.
The photodetector has an internal Faraday shield that provides a guaranteed common-mode transient immunity of $\pm 10\text{ kV}/\mu\text{s}$.
The TLP2108 provides an inverting logic output. A noninverting logic version, the TLP2105, is also available.

- Inverting logic output (totem-pole output)
- Guaranteed performance over -40 to 100°C
- Power supply voltage: 4.5 to 20 V
- Input threshold current: $I_{FHL} = 1.6\text{ mA}$ (max)
- Switching time (t_{pLH} / t_{pHL}): 250 ns (max)
- Common-mode transient immunity: $\pm 10\text{ kV}/\mu\text{s}$
- Isolation voltage: 2500 Vrms

Unit: mm

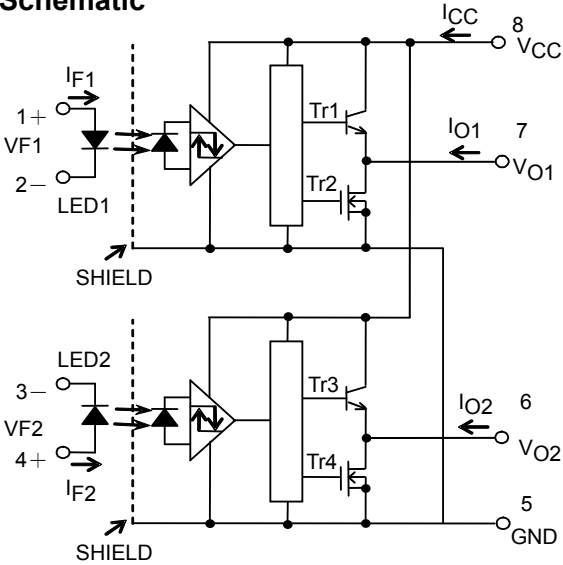


Weight: 0.21 g (typ.)

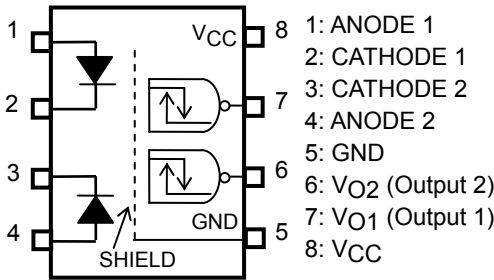
Truth Table

Input	LED1(2)	Tr1(3)	Tr2(4)	Output 1(2)
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

Schematic



Pin Configuration (Top View)



Absolute Maximum Ratings (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Note 1)	I _F	20	mA
	Forward current derating (Ta≥75°C)	ΔI _F /ΔTa	-0.48	mA/°C
	Peak Transient Forward Current (Note 1,2)	I _{FPT}	1	A
	Reverse Voltage (Note 1)	V _R	5	V
DETECTOR	Output Current 1 (Ta ≤ 25°C) (Note 1)	I _{O1}	25/-15	mA
	Output Current 2 (Ta = 100°C) (Note 1)	I _{O2}	5/-5	mA
	Output Voltage (Note 1)	V _O	-0.5 to 20	V
	Supply Voltage	V _{CC}	-0.5 to 20	V
Operating Temperature Range		T _{opr}	-40 to 100	°C
Storage Temperature Range		T _{stg}	-55 to 125	°C
Lead Soldering Temperature (10 s)		T _{sol}	260	°C
Isolation Voltage (AC, 1 min, R.H. ≤ 60%, Ta=25°C) (Note 3)		BV _s	2500	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Each Channel.

Note 2: Pulse width ≤ 1μs, 300 pps.

Note 3: This device is regarded as a two terminal device: pins 1, 2, 3 and 4 are shorted together, as are pins 5, 6, 7 and 8.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current , ON	I _{F(ON)}	2	—	10	mA
Input Voltage , OFF	V _{F(OFF)}	0	—	0.8	V
Supply Voltage*	V _{CC}	4.5	—	20	V
Operating Temperature	T _{opr}	-40	—	100	°C

* This item denotes operating range, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics

(Unless otherwise specified, Ta=-40 to 100°C, V_{CC}=4.5 to 20 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Forward Voltage	V _F	—	I _F =10 mA, Ta=25°C	1.45	1.57	1.75	V
Temperature Coefficient of Forward Voltage	ΔV _F /ΔTa	—	I _F =10 mA	—	-2.0	—	mV/°C
Input Reverse Current	I _R	—	V _R =5 V, Ta=25°C	—	—	10	μA
Input Capacitance	C _T	—	V=0, f=1 MHz, Ta=25°C	—	45	—	pF
Logic Low Output Voltage	V _{OL}	1	I _{OL} =3.5 mA, I _F =5 mA	—	0.2	0.6	V
Logic High Output Voltage	V _{OH}	2	I _{OH} =-2.6 mA, V _F =0.8 V	V _{CC} =4.5 V	2.7	4.0	V
				V _{CC} =20 V	17.4	18.1	
Logic Low Supply Current	I _{CCCL}	3	I _{F1} =I _{F2} =5 mA	V _{CC} =20 V	—	—	6.0
				V _{CC} =5.5 V	—	—	6.0
Logic High Supply Current	I _{CCCH}	4	V _F =0 V	V _{CC} =20 V	—	—	6.0
				V _{CC} =5.5 V	—	—	6.0
Logic Low Short Circuit Output Current (Note 4)	I _{OSL}	5	I _F =5 mA	V _{CC} =V _O =5.5 V	15	80	mA
				V _{CC} =V _O =20 V	20	90	
Logic High Short Circuit Output Current (Note 4)	I _{OSH}	6	V _F =0 V V _O =GND	V _{CC} =5.5 V	-5	-15	mA
				V _{CC} =20 V	-10	-20	
Input Current Logic High Output	I _{FHL}	—	I _O =3.5 mA, V _O <0.6 V	—	0.4	1.6	mA
Input Voltage Logic Low Output	V _{FLH}	—	I _O =-2.6 mA, V _O >2.4 V	0.8	—	—	V
Input Current Hysteresis	I _{HYS}	—	V _{CC} =5 V	—	0.05	—	mA

*All typical values are at Ta=25°C, V_{CC}=5 V unless otherwise specified

Note 4: Duration of output short circuit time should not exceed 10 ms.

Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C _S	V _S = 0, f = 1 MHz (Note 3)	—	0.8	—	pF
Isolation resistance	R _S	R.H. ≤ 60%, V _S = 500 V (Note 3)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 1 minute	2500	—	—	V _{rms}
		AC, 1 second, in oil	—	5000	—	
		DC, 1 minute, in oil	—	5000	—	V _{dc}

Switching Characteristics

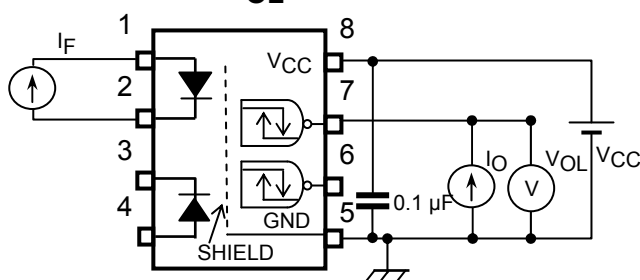
(Unless otherwise specified, $T_a = -40$ to 100°C , $V_{CC} = 4.5$ to 20 V)(Each Channel)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time to Logic High output	t_{pLH}	7,8	$I_F = 3 \rightarrow 0\text{ mA}$	30	150	250	ns
Propagation Delay Time to Logic Low output	t_{pHL}		$I_F = 0 \rightarrow 3\text{ mA}$	30	150	250	ns
Switching Time Dispersion between ON and OFF	$ t_{pHL} - t_{pLH} $		—	—	—	220	ns
Rise Time (10 – 90 %)	t_r		$I_F = 3 \rightarrow 0\text{ mA}$, $V_{CC} = 5\text{ V}$	—	30	75	ns
Fall Time (90 – 10 %)	t_f		$I_F = 0 \rightarrow 3\text{ mA}$, $V_{CC} = 5\text{ V}$	—	30	75	ns
Common Mode transient Immunity at High Level Output	CM_H	9	$V_{CM} = 1000\text{ V}_{p-p}$, $I_F = 0\text{ mA}$, $V_{CC} = 20\text{ V}$, $T_a = 25^\circ\text{C}$	10000	—	—	$\text{V}/\mu\text{s}$
Common Mode transient Immunity at Low Level Output	CM_L		$V_{CM} = 1000\text{ V}_{p-p}$, $I_F = 5\text{ mA}$, $V_{CC} = 20\text{ V}$, $T_a = 25^\circ\text{C}$	-10000	—	—	$\text{V}/\mu\text{s}$

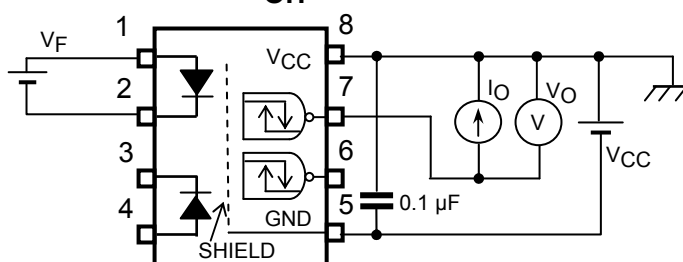
*All typical values are at $T_a = 25^\circ\text{C}$

Note 5: A ceramic capacitor (0.1 μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

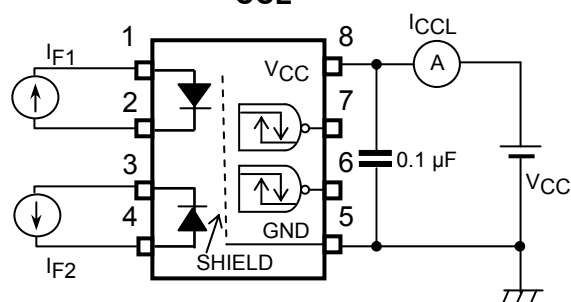
TEST CIRCUIT 1: V_{OL} Test Circuit



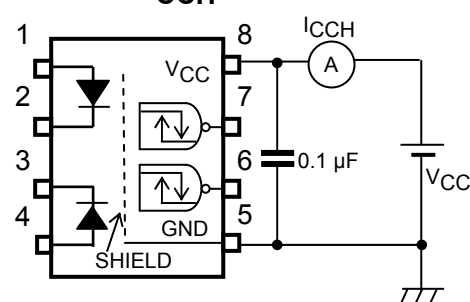
TEST CIRCUIT 2: V_{OH} Test Circuit



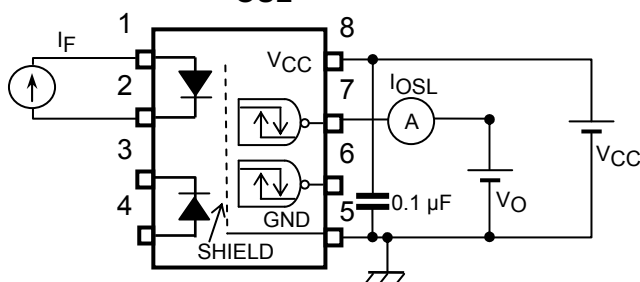
TEST CIRCUIT 3: I_{CCL} Test Circuit



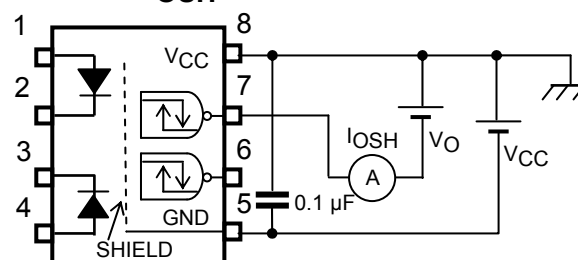
TEST CIRCUIT 4: I_{CCH} Test Circuit



TEST CIRCUIT 5: I_{OSL} Test Circuit



TEST CIRCUIT 6: I_{OSH} Test Circuit



The diagram shows two waveforms: the input signal I_F (top) and the output signal V_{OH} (bottom). The input I_F is a trapezoidal pulse with a high level at 50%. The output V_{OH} is a trapezoidal pulse with a high level at 90% and a low level at 10%. The output voltage levels are labeled V_{OH} and V_{OL} , with a 1.3 V difference indicated between them. The timing parameters are defined as follows:

- t_{pHL} : Propagation delay from input high to output low.
- t_{pLH} : Propagation delay from input low to output high.
- t_f : Fall time of the output signal.
- t_r : Rise time of the output signal.

The diagram shows two waveforms over time. The top waveform is the input current I_F , which is zero until a rising edge, then rises to a constant high level, then falls back to zero at a falling edge. The bottom waveform is the output voltage V_O , which is at V_{OH} until the rising edge, then falls to V_{OL} with a delay t_{pHL} . It remains at V_{OL} until the falling edge, then rises back to V_{OH} with a delay t_{pLH} . The falling edge of V_O passes through a 1.3 V level, and the rising edge passes through a 10% level. The total fall time is t_f and the total rise time is t_r .

Timing diagram showing the relationship between V_{CM} , $SW\ B$, and V_O .

- V_{CM} (Common Mode Voltage) is a trapezoidal wave with a peak of 1000 V, a 90% rise time, and a 10% fall time.
- $SW\ B$ (Switch B) is a square wave with $I_F = 0\ mA$.
- V_O (Output Voltage) shows a 17V dip during the $SW\ B$ high phase and a 1V peak during the $SW\ B$ low phase.
- $SW\ A$ (Switch A) is a square wave with $I_F = 5\ mA$.

$$C_{M_H} = \frac{800(V)}{t_f(\mu s)} \quad C_{M_L} = \frac{800(V)}{t_r(\mu s)}$$

Specification for Embossed-Tape Packing (TP) for SO8 Coupler

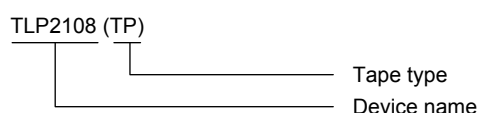
1. Applicable Package

Package	Product Type
SO8	Photocoupler

2. Product Naming System

Type of package used for shipment is denoted by a symbol suffix after a product number. The method of classification is as below.

(Example)



3. Tape Dimensions

3.1 Orientation of Device in Relation to Direction of Tape Movement

Device orientation in the recesses is as shown in Figure 1.

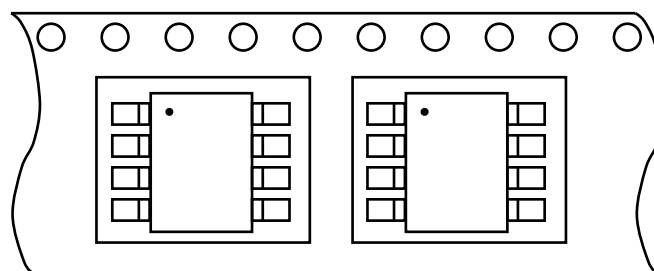


Figure 1 Device Orientation

3.2 Tape Packing Quantity: 2500 devices per reel

3.3 Empty Device Recesses Are as Shown in Table 1.

Table 1 Empty Device Recesses

	Standard	Remarks
Occurrences of 2 or more successive empty device recesses	0	Within any given 40-mm section of tape, not including leader and trailer
Single empty device recesses	6 devices (max) per reel	Not including leader and trailer

3.4 Start and End of Tape

The start of the tape has 50 or more empty holes. The end of tape has 50 or more empty holes and two empty turns only for a cover tape.

3.5 Tape Specification

- (1) Tape material: Plastic (protection against electrostatics)
- (2) Dimensions: The tape dimensions are as shown in Figure 2 and table 2.

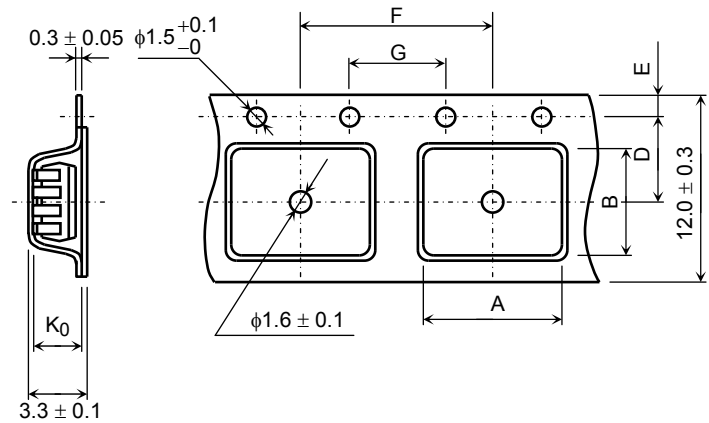


Figure 2 Tape Forms

Table 2 Tape Dimensions

Unit: mm
Unless otherwise specified: ±0.1

Symbol	Dimension	Remark
A	6.5	—
B	5.6	—
D	5.5	Center line of indented square hole and sprocket hole
E	1.75	Distance between tape edge and hole center
F	8.0	Cumulative error $\begin{smallmatrix} +0.1 \\ -0.3 \end{smallmatrix}$ (max) per 10 feed holes
G	4.0	Cumulative error $\begin{smallmatrix} +0.1 \\ -0.3 \end{smallmatrix}$ (max) per 10 feed holes
K ₀	3.1	Internal space

3.6 Reel

- (1) Material: Plastic
- (2) Dimensions: The reel dimensions are as shown in Figure 3 and Table 3.

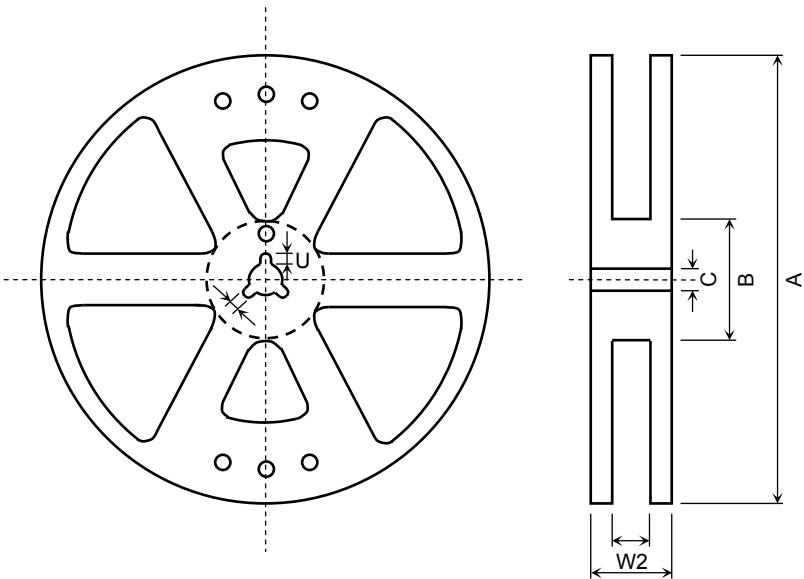


Figure 3 Reel Form

Table 3 Reel Dimensions

Unit: mm

Symbol	Dimension
A	$\Phi 330 \pm 2$
B	$\Phi 80 \pm 1$
C	$\Phi 13 \pm 0.5$
E	2.0 ± 0.5
U	4.0 ± 0.5
W1	13.5 ± 0.5
W2	17.5 ± 1.0

4. Packing

Either one reel or five reels of photocoupler are packed in a shipping carton.

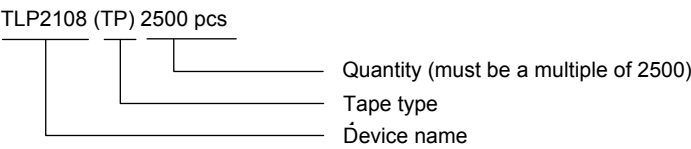
5. Label Indication

The carton bears a label indicating the product number, the symbol representing classification of standard, the quantity, the lot number and the Toshiba company name.

6. Ordering Method

When placing an order, please specify the product number, the tape type and the quantity as shown in the following example.

(Example)

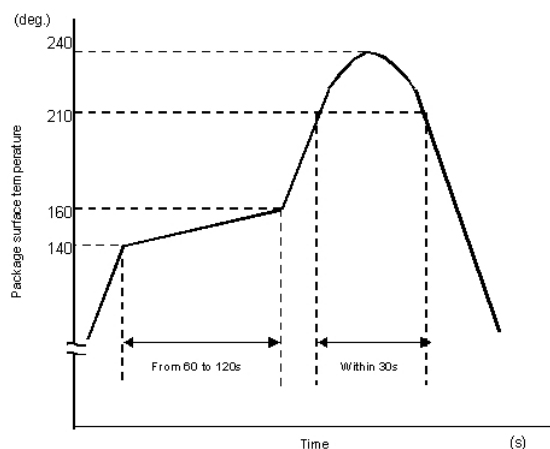


Precautions Of Surface Mounting Type Photocoupler Soldering & General Storage

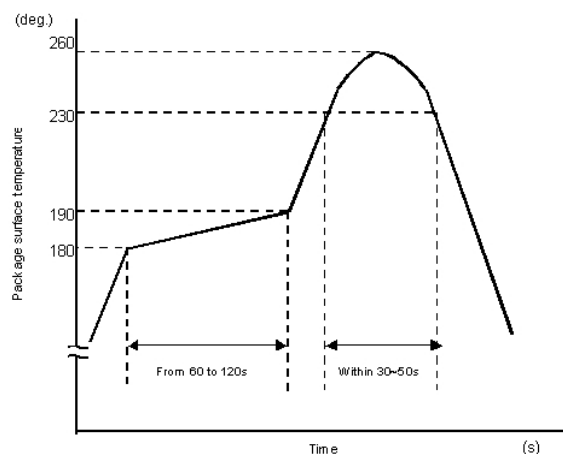
(1) Precautions for Soldering

1) When Using Soldering Reflow

- An example of a temperature profile when Sn-Pb eutectic solder is used:



- An example of a temperature profile when lead(Pb)-free solder is used:



- Reflow soldering must be performed once or twice.
- The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

2) When using soldering Flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)

- Apply preheating of 150deg.C for 60 to 120 seconds.
- Mounting condition of 260deg.C or less within 10 seconds is recommended.
- Flow soldering must be performed once

3) When using soldering Iron (Applicable to both eutectic solder and Lead(Pb)-Free solder)

- Complete soldering within 10 seconds for lead temperature not exceeding 260 deg.C or within 3 seconds not exceeding 350 deg.C.
- Heating by soldering iron must be only once per 1 lead

(2) Precautions for General Storage

- 1) Do not store devices at any place where they will be exposed to moisture or direct sunlight.
- 2) When transportation or storage of devices, follow the cautions indicated on the carton box.
- 3) The storage area temperature should be kept within a temperature range of 5 degree C to 35 degree C, and relative humidity should be maintained at between 45% and 75%.
- 4) Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.
- 5) Use storage areas where there is minimal temperature fluctuation. Because rapid temperature changes can cause condensation to occur on stored devices, resulting in lead oxidation or corrosion, as a result, the solderability of the leads will be degraded.
- 6) When repacking devices, use anti-static containers.
- 7) Do not apply any external force or load directly to devices while they are in storage.
- 8) If devices have been stored for more than two years, even though the above conditions have been followed, it is recommended that solderability of them should be tested before they are used.

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