

TOSHIBA Photocoupler GaAlAs Ired &amp; Photo IC

# TLP2530, TLP2531

Digital Logic Isolation

Line Receiver

Power Supply Control

Switching Power Supply

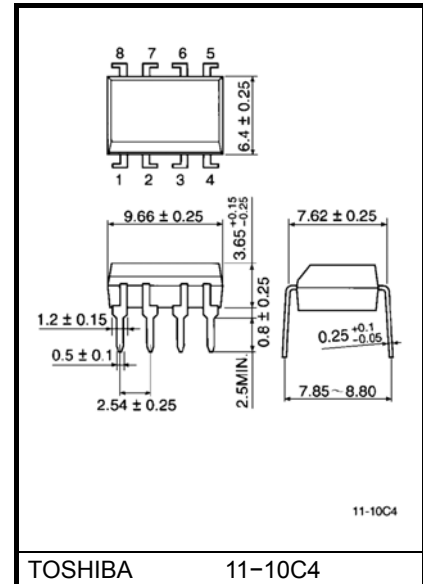
Transistor Inverter

The TOSHIBA TLP2530 and TLP2531 dual photocouplers consist of a pair of GaAlAs light emitting diode and integrated photodetector. This unit is 8-lead DIP.

Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

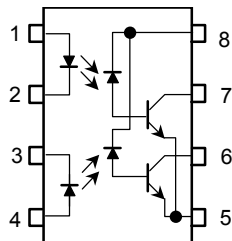
- TTL compatible
- Switching speed:  $t_{pHL}=0.3\mu s$ ,  $t_{pLH}=0.3\mu s$ (typ.)  
(@ $R_L=1.9k\Omega$ )
- Guaranteed performance over temp:  $0\sim 70^\circ C$
- Isolation voltage: 2500 Vrms(min.)
- UL recognized: UL1577, file no. E67349

Unit in mm



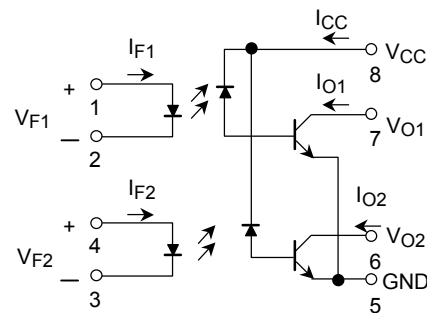
Weight: 0.54 g (typ.)

## Pin Configuration (top view)



1. : Anode.1
2. : Cathode.1
3. : Cathode.2
4. : Anode.2
5. : Gnd
6. :  $V_{O2}$ (output 2)
7. :  $V_{O1}$ (output 1)
8. :  $V_{CC}$

## Schematic



## Absolute Maximum Ratings

Characteristic		Symbol	Rating	Unit
LED	Forward current(each channel) (Note 1)	$I_F$	25	mA
	Pulse forward current (Each Channel) (Note 2)	$I_{FP}$	50	mA
	Total pulse forward current (each channel) (Note 3)	$I_{FPT}$	1	A
	Reverse voltage(each channel)	$V_R$	5	V
	Diode power dissipation (each channel) (Note 4)	$P_D$	45	mW
Detector	Output current(each channel)	$I_O$	8	mA
	Peak output current (each channel)	$I_{OP}$	16	mA
	Supply voltage	$V_{CC}$	-0.5~15	V
	Output voltage(each channel)	$V_O$	-0.5~15	V
	Output power dissipation (each channel) (Note 5)	$P_O$	35	mW
Operating temperature range		$T_{opr}$	-55~100	°C
Storage temperature range		$T_{stg}$	-55~125	°C
Lead solder temperature(10s)**		$T_{sol}$	260	°C
Isolation voltage (AC, 1min., R.H.≤ 60%) (Note 7)		$BV_S$	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8mA above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width. Derate 1.6mA / °C above 70°C.

(Note 3) Pulse width 1μs, 300pps.

(Note 4) Derate 0.9mW / °C above 70°C.

(Note 5) Derate 1mW / °C above 70°C.

\*\*2mm below seating plane.

## Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	$V_{CC}$	0	—	12	V
Forward current, each channel	$I_F$	—	16	25	mA
Operating temperature	$T_{opr}$	-25	—	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

## Electrical Characteristics

Over Recommended Temperature ( $T_a = 0^\circ\text{C} \sim 70^\circ\text{C}$ , unless otherwise noted)

Characteristic		Symbol	Test Condition	Min.	Typ.**	Max.	Unit
Current transfer ratio (each channel)	TLP2530	CTR	$I_F = 16\text{mA}$ , $V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}$ , $T_a = 25^\circ\text{C}$ (Note 6)	7	30	—	%
	TLP2531			19	30	—	
	TLP2530	CTR	$I_F = 16\text{mA}$ , $V_O = 0.5\text{V}$ $V_{CC} = 4.5\text{V}$ (Note 6)	5	—	—	%
	TLP2531			15	—	—	
Logic low output voltage (each channel)	TLP2530	$V_{OL}$	$I_F = 16\text{mA}$ , $I_O = 1.1\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.1	0.4	V
	TLP2531		$I_F = 16\text{mA}$ , $I_O = 2.4\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.1	0.4	V
Logic high output current (each channel)		$I_{OH}$	$I_F = 0\text{mA}$ , $V_O = V_{CC} = 5.5\text{V}$ $T_a = 25^\circ\text{C}$	—	3	500	nA
			$I_F = 0\text{mA}$ , $V_O = V_{CC} = 15\text{V}$	—	—	50	$\mu\text{A}$
Logic low supply current		$I_{CCL}$	$I_{F1} = I_{F2} = 16\text{mA}$ $V_{O1} = V_{O2} = \text{Open}$ $V_{CC} = 15\text{V}$	—	160	—	$\mu\text{A}$
Logic high supply current		$I_{CCH}$	$I_{F1} = I_{F2} = 0\text{mA}$ $V_{O1} = V_{O2} = \text{Open}$ $V_{CC} = 15\text{V}$	—	0.05	4	$\mu\text{A}$
Input forward voltage (each channel)		$V_F$	$I_F = 16\text{mA}$ , $T_a = 25^\circ\text{C}$	—	1.65	1.7	V
Temperature coefficient of forward voltage (each channel)		$\Delta V_F / \Delta T_a$	$I_F = 16\text{mA}$	—	-2	—	mV/ $^\circ\text{C}$
Input reverse breakdown voltage (each channel)		$BV_R$	$I_R = 10\mu\text{A}$ , $T_a = 25^\circ\text{C}$	5	—	—	V
Input capacitance (each channel)		$C_{IN}$	$f = 1\text{MHz}$ , $V_F = 0$	—	60	—	pF
Input-output insulation leakage current		$I_{I-O}$	Relative humidity = 45% $t = 5\text{s}$ , $V_{I-O} = 3000V_{dc}$ $T_a = 25^\circ\text{C}$ (Note 7)	—	—	1.0	$\mu\text{A}$
Resistance (input-output)		$R_{I-O}$	$V_{I-O} = 500V_{dc}$ (Note 7)	—	$10^{12}$	—	$\Omega$
Capacitance (input-output)		$C_{I-O}$	$f = 1\text{MHz}$ (Note 7)	—	0.6	—	pF
Input-input leakage current		$I_{I-I}$	Relative humidity = 45% $t = 5\text{s}$ , $V_{I-I} = 500\text{V}$ (Note 8)	—	0.005	—	$\mu\text{A}$
Resistance (input-input)		$R_{I-I}$	$V_{I-I} = 500V_{dc}$ (Note 8)	—	$10^{11}$	—	$\Omega$
Capacitance (input-input)		$C_{I-I}$	$f = 1\text{MHz}$ (Note 8)	—	0.25	—	pF

\*\*All typicals at  $T_a = 25^\circ\text{C}$ .

**Switching Characteristics (unless otherwise specified, Ta = 25°C, VCC = 5V, IF = 16mA)**

Characteristic		Symbol	Test Cir-cuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time to logic low at output (each channel)	TLP2530	t <sub>pHL</sub>	1	R <sub>L</sub> = 4.1kΩ	—	0.3	1.5	μs
	TLP2531			R <sub>L</sub> = 1.9kΩ	—	0.2	0.8	
Propagation delay time to logic high at output (each channel)	TLP2530	t <sub>pLH</sub>	1	R <sub>L</sub> = 4.1kΩ	—	0.5	1.5	μs
	TLP2531			R <sub>L</sub> = 1.9kΩ	—	0.3	0.8	
Common mode transient immunity at logic high level output (each channel, Note 9)	TLP2530	CM <sub>H</sub>	2	I <sub>F</sub> = 0mA, V <sub>CM</sub> = 400V <sub>p-p</sub> R <sub>L</sub> = 4.1kΩ	—	1500	—	V / μs
	TLP2531			I <sub>F</sub> = 0mA, V <sub>CM</sub> = 400V <sub>p-p</sub> R <sub>L</sub> = 1.9kΩ	—	1500	—	
Common mode transient immunity at logic low level output (each channel, Note 9)	TLP2530	CM <sub>L</sub>	2	V <sub>CM</sub> = 400V <sub>p-p</sub> R <sub>L</sub> = 4.1kΩ, I <sub>F</sub> = 16mA	—	–1500	—	V / μs
	TLP2531			V <sub>CM</sub> = 400V <sub>p-p</sub> R <sub>L</sub> = 1.9kΩ, I <sub>F</sub> = 16mA	—	–1500	—	
Bandwidth (each channel, Note 10)		BW	3	R <sub>L</sub> = 100Ω	—	2	—	MHz

(Note 6) DC current transfer ratio is defined as the ratio of output collector current, I<sub>O</sub>, to the forward LED input current, I<sub>F</sub>, times 100%.

(Note 7) Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

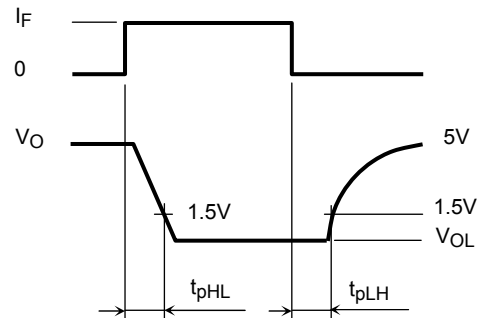
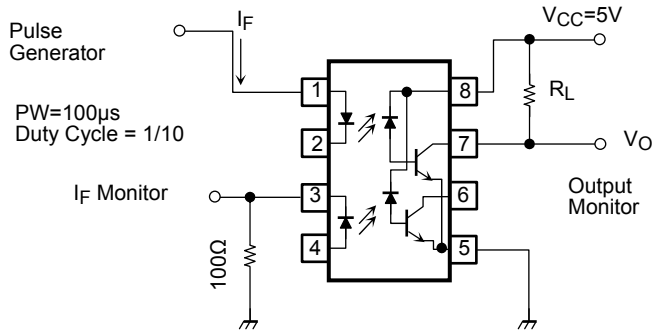
(Note 8) Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

(Note 9) Common mode transient immunity in logic high level is the maximum tolerable (positive) dV<sub>cm</sub> / dt on the leading edge of the common mode pulse, V<sub>cm</sub>, to assure that the output will remain in a logic high state(i.e., V<sub>O</sub> > 2.0V).

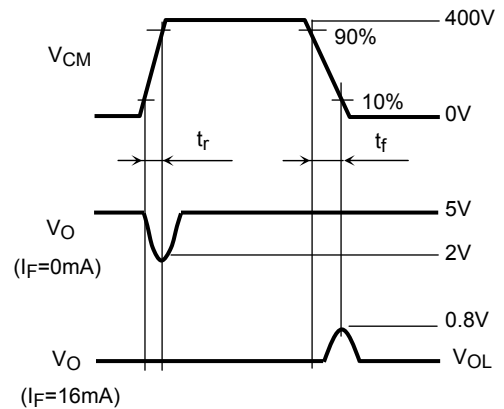
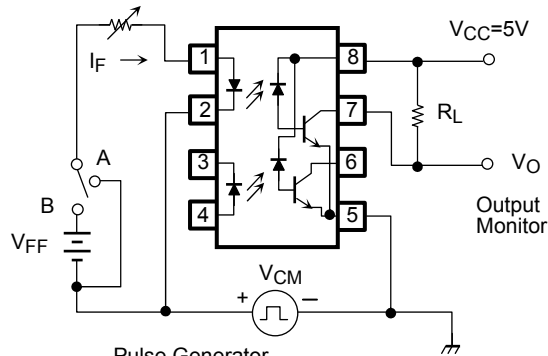
Common mode transient immunity in logic low Level is the maximum tolerable (negative) dV<sub>cm</sub> / dt on the trailing edge of the common mode pulse signal, V<sub>cm</sub>, to assure that the output will remain in logic low state(i.e., V<sub>O</sub> > 0.8V).

(Note 10) The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

## Test Circuit 1: Switching Time, $t_{pHL}$ , $t_{pLH}$

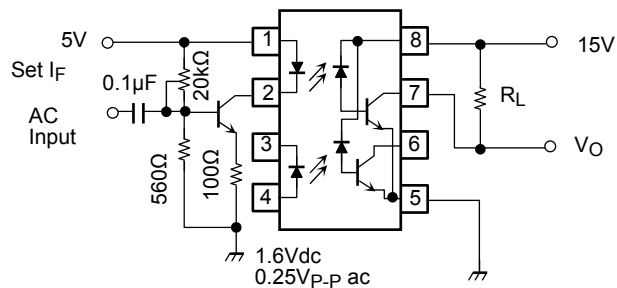


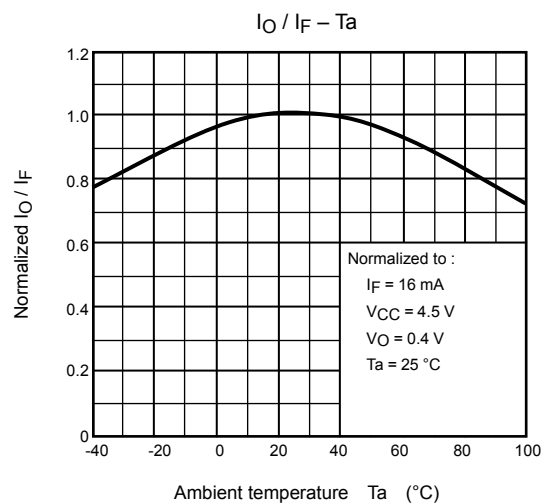
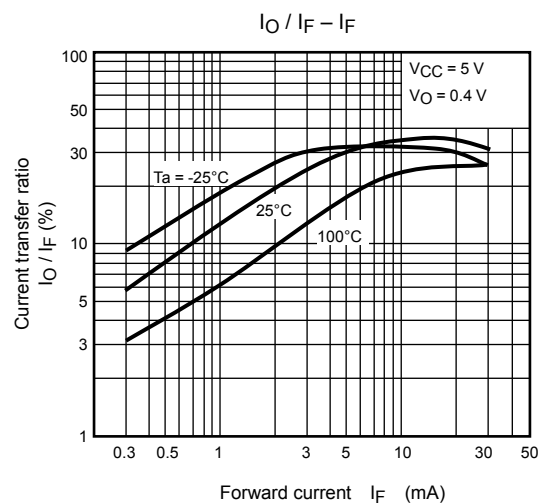
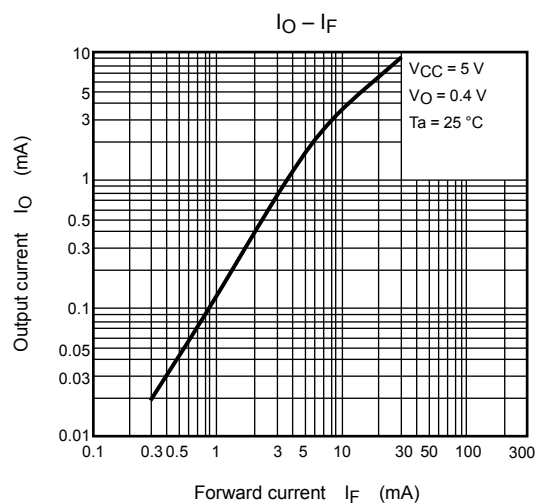
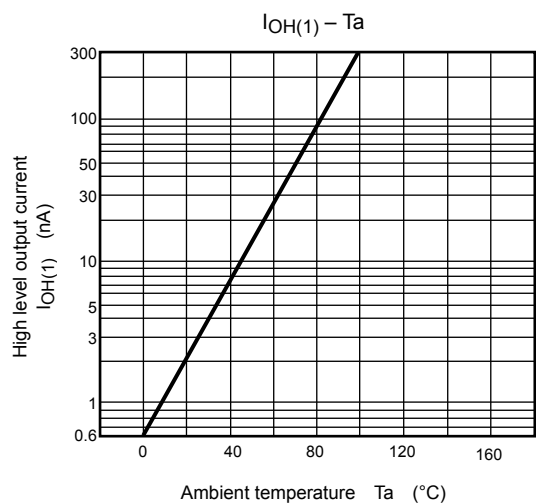
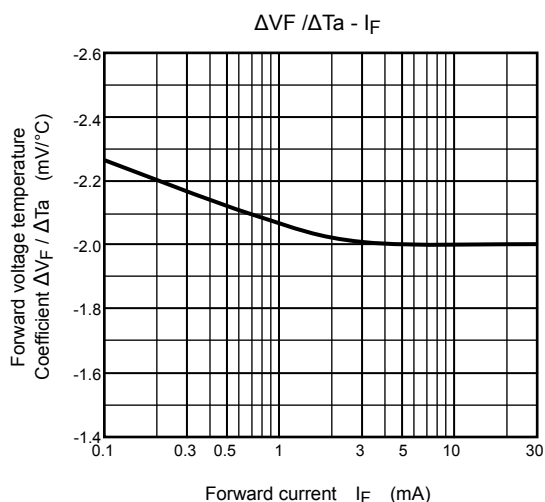
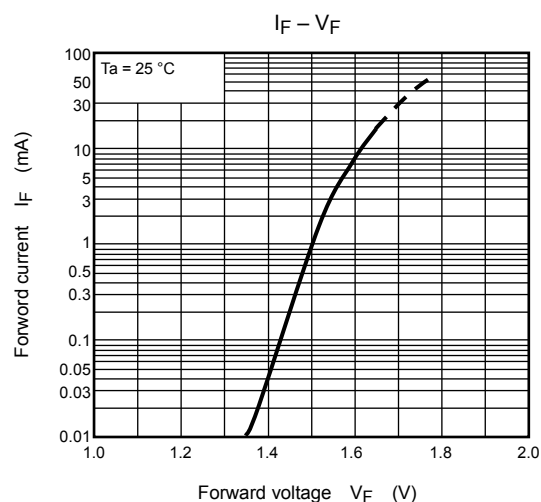
## Test Circuit 2: Transient Immunity And Typical Waveform

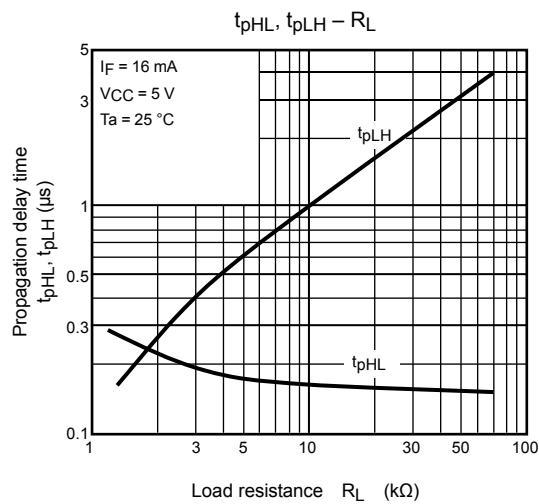
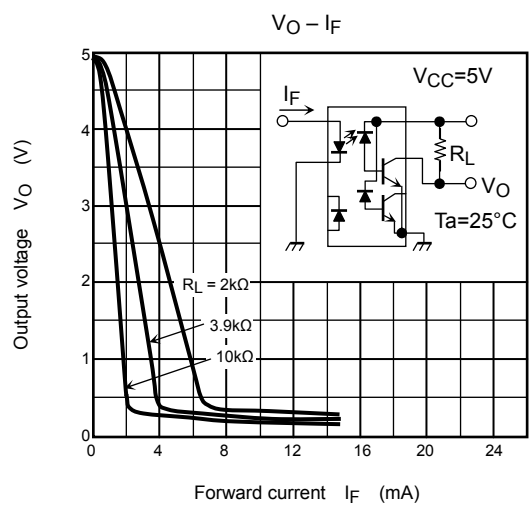
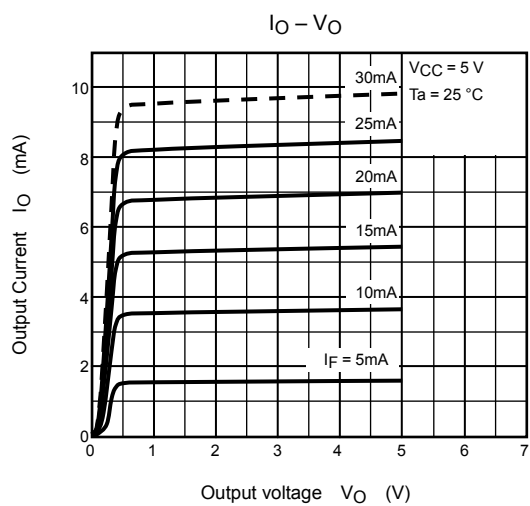


$$CM_H = \frac{320(V)}{t_r(\mu s)}, CM_L = \frac{320(V)}{t_f(\mu s)}$$

## Test Circuit 3: Frequency Response







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