

# TLP715

### Isolated Bus Drivers

### High Speed Line Receivers

### Microprocessor System Interfaces

The Toshiba TLP715 consists of a GaAlAs light-emitting diode and an integrated high-gain, high-speed photodetector. This unit is a 6-pin SDIP. The TLP715 is 50% smaller than the 8-PIN DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The detector has a totem pole output stage to provide both source and sink driving. The detector IC has an internal shield that provides a guaranteed common-mode transient immunity of 10 kV /  $\mu$ s.

The TLP715 is buffer logic type. For inverter logic type, the TLP718 is in line-up.

- Buffer logic output (totem pole output)
- Guaranteed performance over temperature :  $-40$  to  $100^{\circ}\text{C}$
- Power supply voltage : 4.5 to 20 V
- Input current:  $I_{FLH} = 3\text{mA}$  (Max)
- Switching time (  $t_{PLH}$  /  $t_{PHL}$  ) : 250 ns (Max)
- Common-mode transient immunity :  $\pm 10\text{ kV} / \mu\text{s}$  (Min)
- Isolation voltage : 5000 Vrms (Min)
- UL recognized  
UL1577, File No.E67349
- c-UL recognized  
CSA Component Acceptance Service No. 5A, File No.E67349
- Option (D4)  
TÜV recognized / VDE under application : DIN EN60747-5-5

Maximum Operating Insulation Voltage :  $890\text{ V}_{PK}$

Highest Permissible Over Voltage :  $8000\text{ V}_{PK}$

**(Note) : When a EN60747-5-5 approved type is needed,  
Please designate "Option(D4)"**

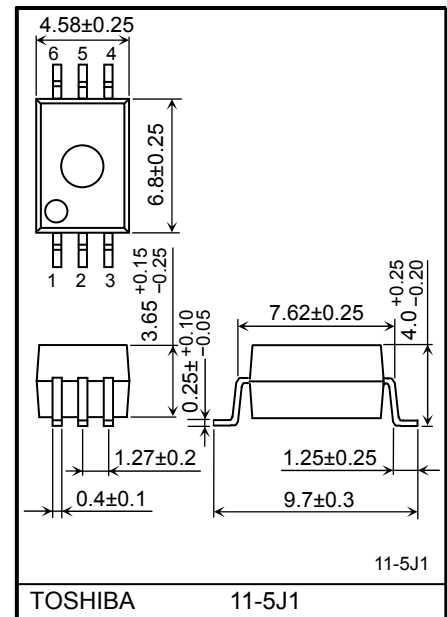
- Construction Mechanical Rating

	7.62 mm pitch TLPXXX type	10.16 mm pitch TLPXXXF type
Creepage Distance	7.0 mm (Min)	8.0 mm (Min)
Clearance	7.0 mm (Min)	8.0 mm (Min)
Insulation Thickness	0.4 mm (Min)	0.4 mm (Min)

### Truth Table

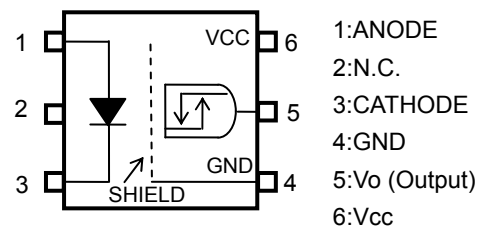
Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Unit in mm

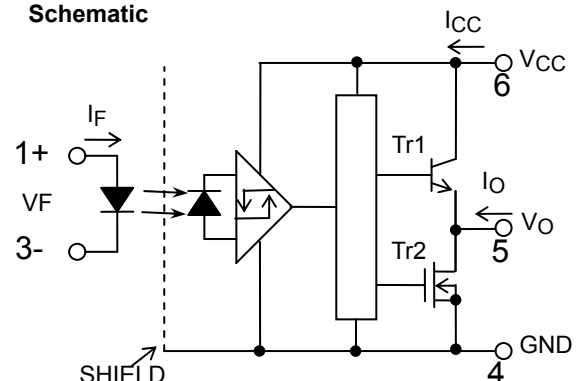


Weight: 0.26 g (typ.)

### Pin Configuration (Top View)



### Schematic



0.1  $\mu$ F bypass capacitor must be connected between pins 6 and 4. (Note 5)

## Absolute Maximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Ta ≤ 83°C)	I <sub>F</sub>	20	mA
	Forward Current Derating (Ta ≥ 83°C)	ΔI <sub>F</sub> /ΔTa	-0.48	mA/°C
	Peak Transient Forward Current (Note 1)	I <sub>FPT</sub>	1	A
	Reverse Voltage	V <sub>R</sub>	5	V
	Junction Temperature	T <sub>J</sub>	125	°C
DETECTOR	Output Current 1 (Ta ≤ 25°C)	I <sub>O1</sub>	25 / -15	mA
	Output Current 2 (Ta ≤ 100°C)	I <sub>O2</sub>	13 / -13	mA
	Output Voltage	V <sub>O</sub>	-0.5 to 20	V
	Supply Voltage	V <sub>CC</sub>	-0.5 to 20	V
	Junction Temperature	T <sub>J</sub>	125	°C
Operating Temperature Range		T <sub>opr</sub>	-40 to 100	°C
Storage Temperature Range		T <sub>stg</sub>	-55 to 125	°C
Lead Solder Temperature (10 s)		T <sub>sol</sub>	260	°C
Isolation Voltage (AC, 1 min., R.H. ≤ 60%, Ta = 25°C) (Note 2)		BVs	5000	V <sub>rms</sub>

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width PW ≤ 1μs, 300pps.

Note 2: Device Considered a two terminal device : pins 1,2 and 3 shorted together and pins 4,5 and 6 shorted together.

## Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current, ON	I <sub>F</sub> (ON)	4.5	-	10	mA
Input Voltage, OFF	V <sub>F</sub> (OFF)	0	-	0.8	V
Supply Voltage*	V <sub>CC</sub>	4.5	-	20	V
Operating Temperature	T <sub>opr</sub>	-40	-	100	°C

\* This item denotes operating ranges, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

## Electrical Characteristics

(Unless otherwise specified, Ta = -40 to 100°C, VCC = 4.5 to 20 V.)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP. *	MAX	UNIT
Input forward voltage	V <sub>F</sub>	-	I <sub>F</sub> = 5 mA, Ta = 25°C	1.4	1.6	1.7	V
Temperature coefficient of forward voltage	ΔV <sub>F</sub> /ΔTa	-	I <sub>F</sub> = 5 mA	-	-2.0	-	mV/°C
Input reverse current	I <sub>R</sub>	-	V <sub>R</sub> = 5 V, Ta = 25°C	-	-	10	μA
Input capacitance	C <sub>T</sub>	-	V = 0 V, f = 1 MHz, Ta = 25°C	-	45	-	pF
Logic LOW output voltage	V <sub>OL</sub>	1	I <sub>OL</sub> = 3.5 mA, V <sub>F</sub> = 0.8 V	-	0.2	0.6	V
Logic HIGH output voltage	V <sub>OH</sub> (Note3)	2	I <sub>OH</sub> = -2.6 mA, V <sub>CC</sub> = 4.5 V	2.7	3.5	-	V
			I <sub>F</sub> = 5 mA, V <sub>CC</sub> = 20 V	17.4	19	-	
Logic LOW supply current	I <sub>CCL</sub>	3	V <sub>F</sub> = 0V	-	-	3.0	mA
Logic HIGH supply current	I <sub>CCH</sub>	4	I <sub>F</sub> = 5 mA	-	-	3.0	mA
Logic LOW short circuit output current (Note4)	I <sub>OSL</sub>	5	V <sub>F</sub> = 0V, V <sub>CC</sub> = V <sub>O</sub> = 5.5 V	15	80	-	mA
			V <sub>CC</sub> = V <sub>O</sub> = 20 V	20	90	-	
Logic HIGH short circuit output current (Note4)	I <sub>OSH</sub>	6	I <sub>F</sub> = 5mA, V <sub>CC</sub> = 5.5 V	-5	-15	-	mA
			V <sub>O</sub> = GND, V <sub>CC</sub> = 20 V	-10	-20	-	
Input current logic HIGH output	I <sub>FLH</sub>	-	I <sub>O</sub> = -2.6 mA, V <sub>O</sub> > 2.4 V	-	0.4	3	mA
Input voltage logic LOW output	V <sub>FHL</sub>	-	I <sub>O</sub> = 3.5 mA, V <sub>O</sub> < 0.6V	0.8	-	-	V
Input current hysteresis	I <sub>HYS</sub>	-	V <sub>CC</sub> = 5 V	-	0.05	-	mA

\* All typical values are at Ta=25°C, VCC=5 V unless otherwise specified

Note 3: V<sub>OH</sub> = V<sub>CC</sub> - V<sub>O</sub> [V]

Note 4: Duration of output short circuit time should not exceed 10 ms.

Note 5: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

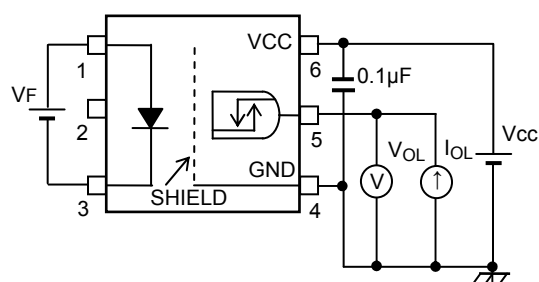
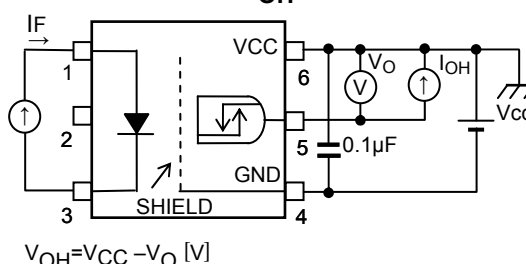
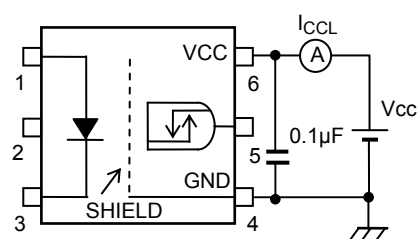
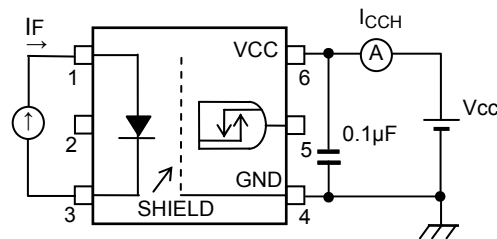
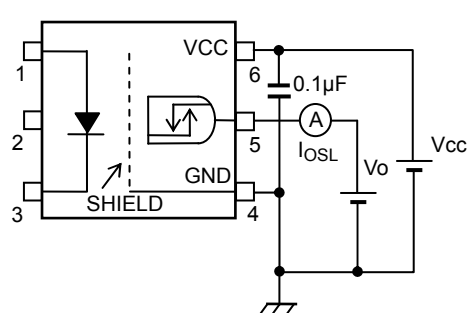
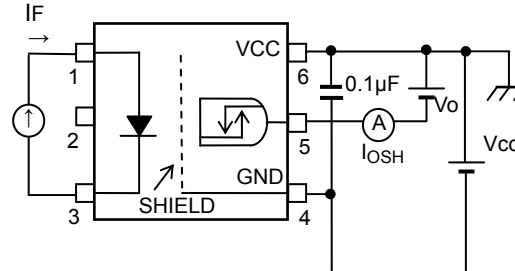
## Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Capacitance input to output	C <sub>S</sub>	V = 0 V, f = 1 MHz (Note 2)	-	1.0	-	pF
Isolation resistance	R <sub>S</sub>	R.H. ≤ 60%, V <sub>S</sub> = 500 V (Note 2)	1×10 <sup>12</sup>	10 <sup>14</sup>	-	Ω
Isolation voltage	BV <sub>S</sub>	AC, 1 minute	5000	-	-	V <sub>rms</sub>
		AC, 1 second, in oil	-	10000	-	
		DC, 1 minute, in oil	-	10000	-	V <sub>dc</sub>

## Switching Characteristics

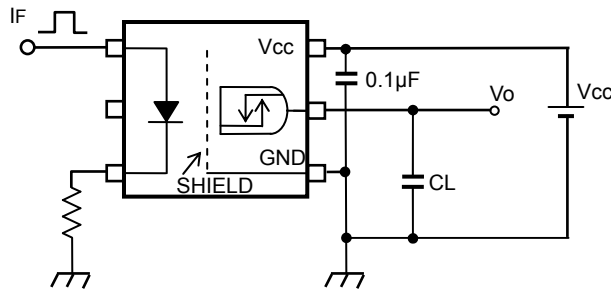
(Unless otherwise specified,  $T_a = -40$  to  $100^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $20$  V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP. *	MAX	UNIT
Propagation delay time to logic HIGH output	$t_{pLH}$	7,8	$I_F = 0 \rightarrow 3$ mA	30	120	250	ns
Propagation delay time to logic LOW output	$t_{pHL}$		$I_F = 3 \rightarrow 0$ mA	30	120	250	ns
Switching time dispersion between ON and OFF	$ t_{pLH} - t_{pHL} $		-	-	-	220	ns
Rise Time (10 – 90 %)	$t_r$		$I_F = 0 \rightarrow 3$ mA, $V_{CC} = 5$ V	-	30	-	ns
Fall Time (90 – 10 %)	$t_f$		$I_F = 3 \rightarrow 0$ mA, $V_{CC} = 5$ V	-	30	-	ns
Common-mode transient Immunity at HIGH level output	$CM_H$	9	$V_{CM} = 1000$ Vp-p, $I_F = 5$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$	10000	-	-	V/ $\mu\text{s}$
Common-mode transient Immunity at LOW level output	$CM_L$		$V_{CM} = 1000$ Vp-p, $I_F = 0$ mA, $V_{CC} = 20$ V, $T_a = 25^\circ\text{C}$	-10000	-	-	V/ $\mu\text{s}$

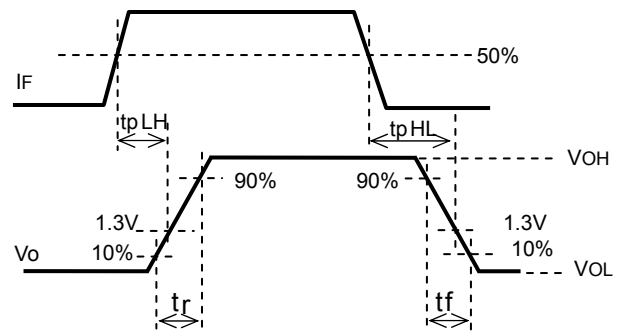
\*All typical values are at  $T_a = 25^\circ\text{C}$ .TEST CIRCUIT 1 :  $V_{OL}$ TEST CIRCUIT 2 :  $V_{OH}$ TEST CIRCUIT 3 :  $I_{CCL}$ TEST CIRCUIT 4 :  $I_{CCH}$ TEST CIRCUIT 5 :  $I_{OSL}$ TEST CIRCUIT 6 :  $I_{OSH}$ 

## TEST CIRCUIT 7: Switching Time Test Circuit

$I_F = 3 \text{ mA (P.G)}$   
( $f = 50 \text{ kHz}$ , duty=50%  
less than  $t_r = t_f = 5 \text{ ns}$ )

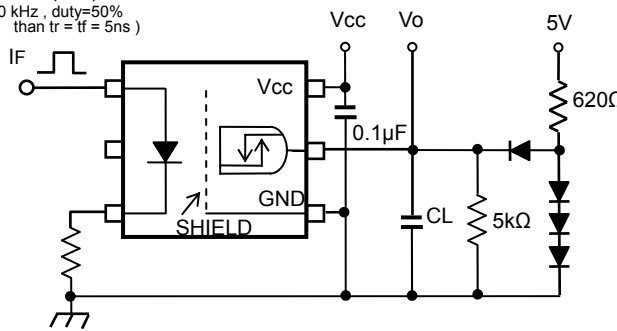


CL: stray capacitance of probe and wiring (to 15 pF)

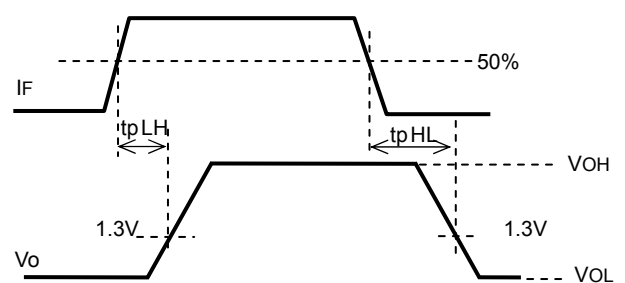


## TEST CIRCUIT 8: Switching Time Test Circuit

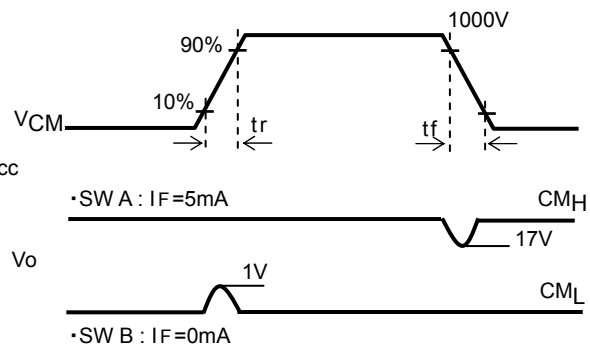
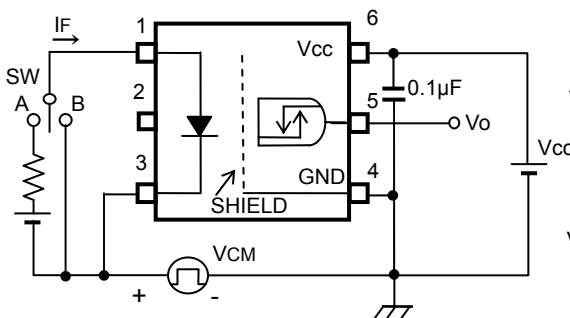
$I_F = 3 \text{ mA (P.G)}$   
( $f = 50 \text{ kHz}$ , duty=50%  
less than  $t_r = t_f = 5 \text{ ns}$ )



CL: stray capacitance of probe and wiring (to 15 pF)



## TEST CIRCUIT 9: Common-Mode Transient Immunity Test Circuit



• SW A :  $I_F = 5 \text{ mA}$

• SW B :  $I_F = 0 \text{ mA}$

$$CM_L = \frac{800(V)}{t_r(\mu s)} \quad CM_H = -\frac{800(V)}{t_f(\mu s)}$$

$CM_H$  ( $CM_L$ ) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the high (low) state.

## EN60747-5-5 Option:(D4)

Types : TLP715, TLP715F

Type designations for "option: (D4)", which are tested under EN60747 requirements.

Ex.: TLP715 (D4-TP,F)

D4 : EN60747 option

TP : Standard tape & reel type

F : [[G]]/RoHS COMPATIBLE


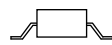
Note: Use TOSHIBA standard type number for safety standard application.

Ex.: TLP715 (D4-TP,F) → TLP715

### EN60747 Isolation Characteristics

Description		Symbol	Rating	Unit
Application classification				
for rated mains voltage $\leq 300V_{rms}$ for rated mains voltage $\leq 600V_{rms}$			I-IV I-III	—
Climatic classification			40/ 100 / 21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	$V_{IORM}$	890	Vpk
	TLPxxxFtype		1140	
Input to output test voltage, method A $V_{pr}=1.5 \times V_{IORM}$ , type and sample test $t_p=10s$ , partial discharge $<5pC$	TLPxxx type	$V_{pr}$	1335	Vpk
	TLPxxxFtype		1710	
Input to output test voltage, method B $V_{pr}=1.875 \times V_{IORM}$ , 100% production test $t_p=1s$ , partial discharge $<5pC$	TLPxxx type	$V_{pr}$	1670	Vpk
	TLPxxxFtype		2140	
Highest permissible overvoltage (transient overvoltage, $t_{pr} = 60s$ )		$V_{TR}$	8000	Vpk
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current $I_F$ , $P_{Si} = 0$ ) power (output or total power dissipation) temperature		$I_{Si}$ $P_{Si}$ $T_{Si}$	300 700 150	mA mW °C
Insulation resistance, input-output $V_{IO} = 500V$ , $T_a=25^\circ C$ $V_{IO} = 500V$ , $T_a=100^\circ C$ $V_{IO} = 500V$ , $T_a=T_{Si}$		$R_{Si}$	$\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^9$	$\Omega$

Insulation Related Specifications

		 7.62mm pitch TLPxxx type	 10.16mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0mm	8.0mm
Minimum clearance	Cl	7.0mm	8.0mm
Minimum insulation thickness	ti	0.4mm	
Comperative tracking index	CTI	175	

- 1. If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e.g.at a standard distance between soldering eye centres of 7.5mm). If this is not permissible, the user shall take suitable measures.
- 2. This photocoupler is suitable for ‘safe electrical isolation’ only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Marking on product for EN60747   Option:(D4)   :   **4**

Marking Example :

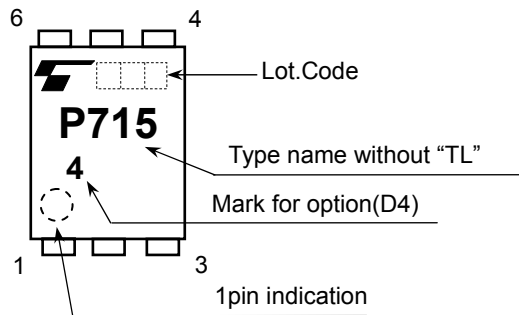


Figure 1 Partial discharge measurement procedure according to EN60747  
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests,  
destructive tests)

$t_1, t_2$  = 1 to 10 s  
 $t_3, t_4$  = 1 s  
 $t_p$ (Measuring time for  
partial discharge) = 10 s  
 $t_b$  = 12 s  
 $t_{ini}$  = 60 s

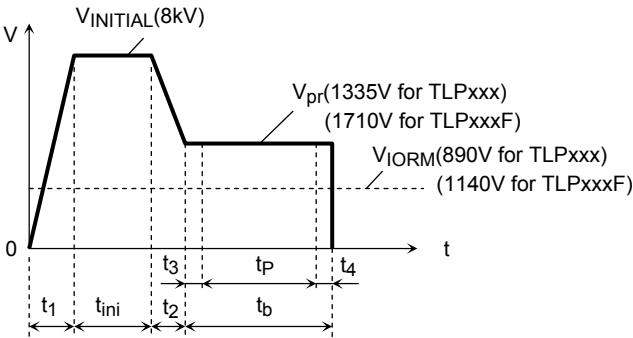


Figure 2 Partial discharge measurement procedure according to EN60747  
Non-destructive test for 100% inspection.

Method B

(for sample test, non-  
destructive test)

$t_3, t_4$  = 0.1 s  
 $t_p$ (Measuring time for  
partial discharge) = 1 s  
 $t_b$  = 1.2 s

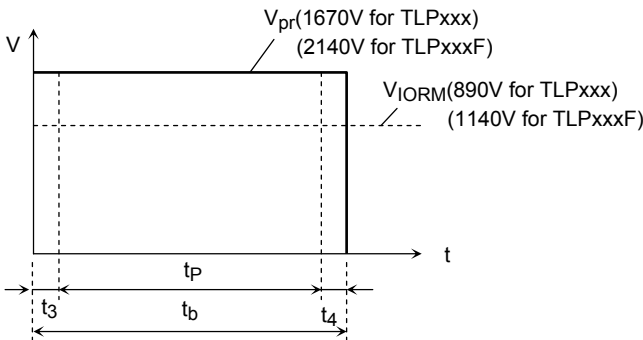
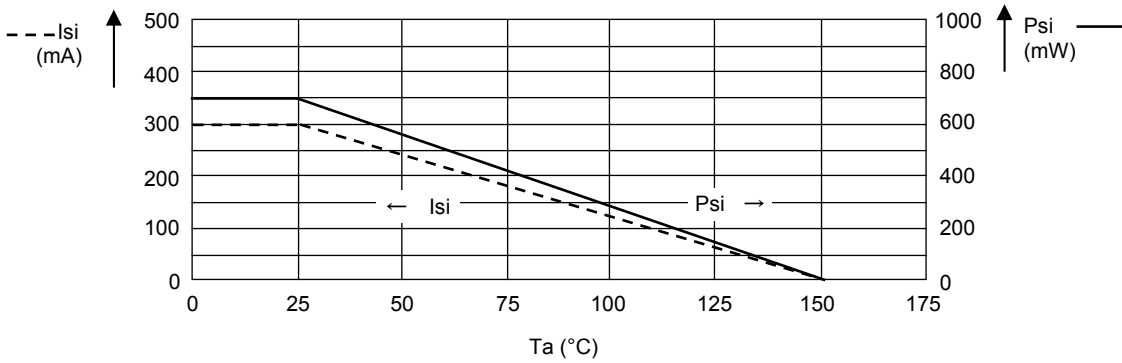


Figure 3 Dependency of maximum safety ratings on ambient temperature (for  
photodetector failure)





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