

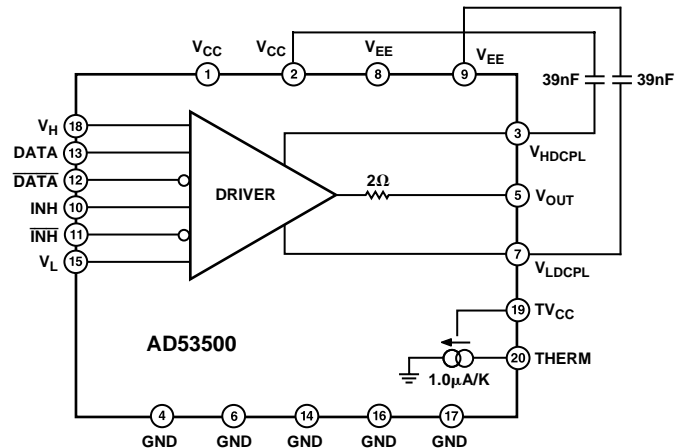
### FEATURES

- 2 V to +6 V Output Range
- 2.5  $\Omega$  Output Resistance
- 2.5 ns Tr/Tf for a 3 V Step
- 300 MHz Toggle Rate
- Can Drive 25  $\Omega$  Lines and Lower
- Peak Dynamic Current Capability of 400 mA
- Inhibit Leakage <1  $\mu$ A
- On-Chip Temperature Sensor

### APPLICATIONS

- Automatic Test Equipment
- Semiconductor Test Systems
- Board Test Systems
- Instrumentation and Characterization Equipment

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT DESCRIPTION:

The AD53500 is a complete high speed driver designed for use in digital or mixed signal test systems where high speed and high output drive capabilities are needed. Combining a high speed monolithic process and a unique surface mount package, this product attains superb electrical performance while preserving optimum packing densities and long-term reliability thanks to an ultrasmall 20-lead, PSOP package with built-in heat sink.

High and low reference levels can be set within a -2 V to +6 V range with low offset voltage and high gain accuracy. A 2.5  $\Omega$  output resistance allows use of an external backmatch resistor for application to 50  $\Omega$ , 25  $\Omega$  or other complex impedance load requirements. Without a backmatch resistor it is also capable of driving highly capacitive loads, typically achieving a rise/fall time

of less than 10 ns with a 1000 pF capacitance. To test I/O devices, the pin driver can be switched into a high impedance state (Inhibit Mode), electrically removing the driver from the path. The pin driver leakage current in inhibit is typically less than 1  $\mu$ A and output capacitance is typically less than 18 pF.

Transitions from HI/LO or to inhibit are controlled through the data and inhibit inputs. The input circuitry utilizes high-speed differential inputs with a common-mode range of -2 V to +5 V. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single-ended CMOS or TTL logic source or any combination over the common-mode range. The analog logic HI/LO inputs are equally easy to interface, typically requiring 50  $\mu$ A of bias current.

### REV. 0

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# AD53500—SPECIFICATIONS

(All specifications are at  $T_j = +85^\circ\text{C} \pm 5^\circ\text{C}$ ,  $+V_S = +10\text{ V} \pm 3\%$ ,  $-V_S = +6\text{ V} \pm 3\%$  unless otherwise noted. All temperature coefficients are measured over  $T_j = 75^\circ\text{C} - 95^\circ\text{C}$ ). (In test figures, voltmeter loading is  $1\text{ M}\Omega$  or greater, scope probe loading is  $100\text{ k}\Omega$  in parallel with  $5\text{ pF}$ .)  $39\text{ nF}$  capacitors must be connected between  $V_{CC}$  and  $V_{HDCPL}$  and between  $V_{EE}$  and  $V_{LDCPL}$ .)

Parameter	Min	Typ	Max	Units	Test Conditions
<b>DIFFERENTIAL INPUT CHARACTERISTICS</b> (DATA to $\overline{\text{DATA}}$ , INH to $\overline{\text{INH}}$ )					
Common-Mode Input Voltage	-2		+5	Volts	ECL = $-0.8\text{ V} / -1.8\text{ V}$ , TTL = $0\text{ V} / 5\text{ V}$ $V_{CM} = -2\text{ V}, +5\text{ V}$
Differential Input Range		ECL or TTL			
Bias Current		$\pm 100$		$\mu\text{A}$	
<b>REFERENCE INPUTS</b>					
Bias Currents	-50		+50	$\mu\text{A}$	$V_L, V_H = 5\text{ V}$
<b>OUTPUT CHARACTERISTICS</b>					
Logic High Range	+1		+6	Volts	DATA = H, $V_L = -2\text{ V}$ , $V_H = +1\text{ V}$ to $+6\text{ V}$
Logic Low Range	-2		+2	Volts	DATA = L, $V_L = -2\text{ V}$ to $+2\text{ V}$ , $V_H = +6\text{ V}$
Amplitude ( $V_H$ and $V_L$ )	0.1		8	Volts	$V_L = -0.05\text{ V}$ , $V_H = +0.05\text{ V}$ and $V_L = -2\text{ V}$ , $V_H = +6\text{ V}$
$V_H, V_L$ Interaction	-10		+10	mV	100 mV Output Amplitude
Absolute Accuracy					
$V_H$ Offset	-100		+100	mV	DATA = H, $V_H = 0\text{ V}$ , $V_L = -2\text{ V}$
$V_H$ Gain + Linearity Error		$\pm 0.3 \pm 5$		% of $V_H$ + mV	DATA = H, $V_L = -2\text{ V}$ , $V_H = +1\text{ V}$ to $+6\text{ V}$
$V_L$ Offset	-100		+100	mV	DATA = L, $V_L = 0\text{ V}$ , $V_H = +6\text{ V}$
$V_L$ Gain + Linearity Error		$\pm 0.3 \pm 5$		% of $V_L$ + mV	DATA = L, $V_L = -2\text{ V}$ to $+2\text{ V}$ , $V_H = +6\text{ V}$
Offset TC, $V_H$ or $V_L$		0.5		mV/ $^\circ\text{C}$	$V_L, V_H = 0\text{ V}, +5\text{ V}$ and $-2\text{ V}, 0\text{ V}$
Output Resistance	1.5	2.5	5.5	$\Omega$	$V_H = +3\text{ V}$ , $V_L = 0\text{ V}$ , $I_{OUT} = 0, -30\text{ mA}, +30\text{ mA}$
Dynamic Current Limit		400		mA	$C_{BYP} = 39\text{ nF}$ , $V_H = +5\text{ V}$ , $V_L = 0\text{ V}$
Static Current Limit	60		180	mA	$C_{LOAD} = 1000\text{ pF}$ , $Tr/Tf = 10\text{ ns}$
	-180		-60	mA	Output to $-2\text{ V}$ , $V_H = +6\text{ V}$ , $V_L = -1\text{ V}$ , DATA = H and Output to $+6\text{ V}$ , $V_H = +6\text{ V}$ , $V_L = -2\text{ V}$ , DATA = L
<b>DYNAMIC PERFORMANCE, DRIVE</b> ( $V_H$ and $V_L$ )					
Propagation Delay Time		2.5		ns	Measured at 50%, $V_H = +400\text{ mV}$ , $V_L = -400\text{ mV}$
Propagation Delay TC		1		ps/ $^\circ\text{C}$	Measured at 50%, $V_H = +400\text{ mV}$ , $V_L = -400\text{ mV}$
Delay Matching, Edge-to-Edge		100		ps	Measured at 50%, $V_H = +400\text{ mV}$ , $V_L = -400\text{ mV}$
Rise and Fall Time					
1 V Swing		0.85		ns	Measured 20%–80%, $V_L = 0\text{ V}$ , $V_H = 1\text{ V}$
3 V Swing		2.5		ns	Measured 10%–90%, $V_L = 0\text{ V}$ , $V_H = 3\text{ V}$
5 V Swing		4.0		ns	Measured 10%–90%, $V_L = 2\text{ V}$ , $V_H = 3\text{ V}$
Rise and Fall Time TC					
1 V Swing		$\pm 1$		ps/ $^\circ\text{C}$	Measured 20%–80%, $V_L = 0\text{ V}$ , $V_H = 1\text{ V}$
3 V Swing		$\pm 2$		ps/ $^\circ\text{C}$	Measured 10%–90%, $V_L = 0\text{ V}$ , $V_H = 3\text{ V}$
5 V Swing		$\pm 3$		ps/ $^\circ\text{C}$	Measured 10%–90%, $V_L = 0\text{ V}$ , $V_H = 5\text{ V}$
Overshoot, Undershoot and Preshoot		+5.0 +30		% of Step + mV	$V_H - V_L = 0.5\text{ V}, 1\text{ V}, 3\text{ V}, 8\text{ V}$
Settling Time					
to 15 mV		40		ns	$V_L = 0\text{ V}$ , $V_H = 0.5\text{ V}$
to 4 mV		8		$\mu\text{s}$	$V_L = 0\text{ V}$ , $V_H = 0.5\text{ V}$
Delay Change vs. Pulsewidth		100		ps	$V_L = 0\text{ V}$ , $V_H = 2\text{ V}$ , Pulsewidth = $2.5\text{ ns}$ / Period = $10\text{ ns}$ and Pulsewidth = $30\text{ ns}$ / Period = $120\text{ ns}$
Minimum Pulsewidth					
3 V Swing		3.8		ns	$V_L = 0\text{ V}$ , $V_H = 3\text{ V}$ , Output = $2.7\text{ V p-p}$ , Measure at 50%
5 V Swing		5.5		ns	$V_L = 0\text{ V}$ , $V_H = 5\text{ V}$ , Output = $4.5\text{ V p-p}$ , Measure at 50%
Toggle Rate		300		MHz	$V_L = -1.8\text{ V}$ , $V_H = -0.8\text{ V}$ , $V_{OUT} > 600\text{ mV p-p}$

Parameter	Min	Typ	Max	Units	Test Conditions
<b>DYNAMIC PERFORMANCE, INHIBIT</b>					
Delay Time, Active to Inhibit	2		10	ns	Measured at 50%, $V_H = +2$ V, $V_L = -2$ V, 50 $\Omega$ Terminated to Ground
Delay Time, Inhibit to Active	2		10	ns	Measured at 50%, $V_H = +2$ V, $V_L = -2$ V, 50 $\Omega$ Terminated to Ground
I/O Spike		<200		mV, p-p	$V_H = 0$ V, $V_L = 0$ V
Output Leakage	-1.0		+1.0	$\mu$ A	$V_{OUT} = -2$ V to +6 V
Output Capacitance		18		pF	Driver Inhibited
PSRR, Drive Mode		35		dB	$V_S = V_S \pm 3\%$
<b>POWER SUPPLIES</b>					
Total Supply Range		16		V	
Positive Supply		+10		V	
Negative Supply		-6		V	
Positive Supply Current		85	95	mA	
Negative Supply Current		88	98	mA	
Total Power Dissipation		1.37	1.54	W	
Temperature Sensor Gain Factor		1.0		$\mu$ A/K	$R_{LOAD} = 10$ k $\Omega$ , $V_{SOURCE} = +10$ V

**NOTES**

Connecting or shorting the decoupling capacitors to ground will result in the destruction of the device.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>****Power Supply Voltage**

+ $V_S$ to GND	+11 V
- $V_S$ to GND	-7 V
+ $V_S$ to - $V_S$	+18 V

**Inputs**

DATA, $\overline{\text{DATA}}$ , INH, $\overline{\text{INH}}$	+5 V, -3 V
DATA to $\overline{\text{DATA}}$ , INH to $\overline{\text{INH}}$	$\pm 3$ V
$V_{HB}$ , $V_L$ to GND	+7 V, -3 V
$V_H$ to $V_L$	+10 V, 0 V

**Outputs**

$V_{OUT}$ Short Circuit Duration to Ground	Indefinite <sup>2</sup>
$V_{OUT}$ Range in Inhibit Mode	See Figure 1
$V_{HDCPL}$	Do Not Connect Except for Cap to $V_{CC}$ <sup>3</sup>
$V_{LDCPL}$	Do Not Connect Except for Cap to $V_{EE}$ <sup>3</sup>
THERM	+ $V_S$ , 0 V

**Environmental**

Operating Temperature (Junction)	+175°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec) <sup>4</sup>	+260°C

**NOTES**

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Output short circuit protection is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.

<sup>3</sup>The  $V_{HDCPL}$  and  $V_{LDCPL}$  capacitors may be replaced by a low value resistor for higher dc-current drive capability.

<sup>4</sup>To ensure lead coplanarity ( $\pm 0.002$  inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C  $\pm 5$ °C (75°F  $\pm 10$ °F) with relative humidity not to exceed 65%.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53500 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

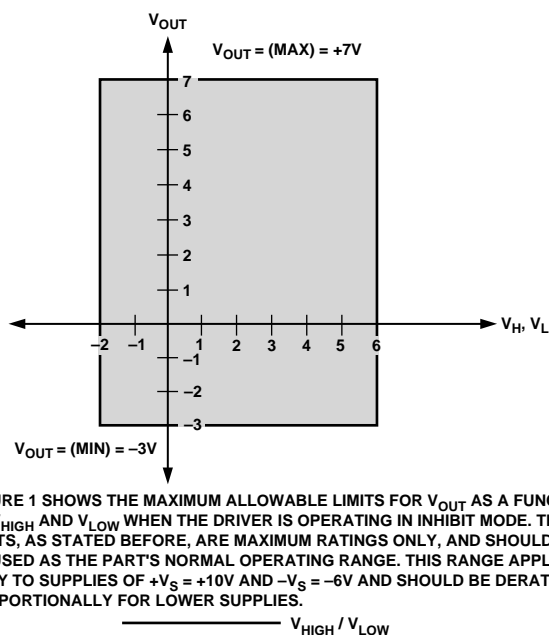


FIGURE 1 SHOWS THE MAXIMUM ALLOWABLE LIMITS FOR  $V_{OUT}$  AS A FUNCTION OF  $V_{HIGH}$  AND  $V_{LOW}$  WHEN THE DRIVER IS OPERATING IN INHIBIT MODE. THE LIMITS, AS STATED BEFORE, ARE MAXIMUM RATINGS ONLY, AND SHOULD NOT BE USED AS THE PART'S NORMAL OPERATING RANGE. THIS RANGE APPLIES ONLY TO SUPPLIES OF + $V_S = +10$  V AND - $V_S = -6$  V AND SHOULD BE DERATED PROPORTIONALLY FOR LOWER SUPPLIES.

Figure 1. Absolute Maximum Ratings for  $V_{OUT}$



# AD53500

## PIN CONFIGURATION

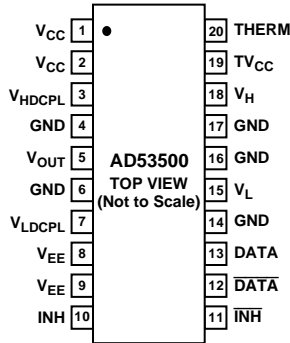


Table I. Pin Driver Truth Table

DATA	$\overline{\text{DATA}}$	INH	$\overline{\text{INH}}$	Output State
0	1	0	1	$V_L$
1	0	0	1	$V_H$
0	1	1	0	Hi-Z
1	0	1	0	Hi-Z

Table II. Package Thermal Characteristics

Air Flow, FM	$\theta_{JC}$ , °C/W	$\theta_{JA}$ , °C/W
50	3.28	49.1
400	3.91	33.74

## PIN FUNCTION DESCRIPTIONS

Pin Name	Pin Number	Description
$V_{CC}$	1, 2	Positive Power Supply. Both pins should be connected to minimize inductance and allow maximum speed of operation. $V_{CC}$ should be decoupled to GND with a low inductance 0.1 $\mu\text{F}$ capacitor.
$V_{EE}$	8, 9	Negative Power Supply. Both pins should be connected to keep the inductance down and allow maximum speed of operation. $V_{EE}$ should be decoupled to GND with a low inductance 0.1 $\mu\text{F}$ capacitor.
GND	4, 6, 14, 16, 17	Device Ground. These pins should be connected to the circuit board's ground plane at the pins.
$V_L$	15	Analog input that sets the voltage level of a Logic 0 of the driver. Determines the driver output for $\overline{\text{DATA}} > \text{DATA}$ .
$V_H$	18	Analog input that sets the voltage level of a Logic 1 of the driver. Determines the driver output for $\text{DATA} > \overline{\text{DATA}}$ .
$V_{OUT}$	5	The Driver Output.
$V_{HDCPL}$	3	Internal supply decoupling for the output stage. This pin is connected to $V_{CC}$ through a 39 nF (minimum) capacitor.
$V_{LDCPL}$	7	Internal supply decoupling for the output stage. This pin is connected to $V_{EE}$ through a 39 nF (minimum) capacitor.
INH, $\overline{\text{INH}}$	10, 11	Differential inputs that control the high impedance state of the driver. When $\text{INH} > \overline{\text{INH}}$ , the driver goes into a high impedance state.
DATA, $\overline{\text{DATA}}$	13, 12	Differential inputs that determine the high and low state of the driver. Driver output is high for $\text{DATA} > \overline{\text{DATA}}$ .
$TV_{CC}$	19	Temperature Sensor Startup Pin. This pin should be connected to $V_{CC}$ .
THERM	20	Temperature sensor output pin. A resistor (10 k $\Omega$ ) should be connected between THERM and $V_{CC}$ . The approximate die temperature can be determined by measuring the current through the resistor. The typical scale factor is 1 $\mu\text{A}/\text{K}$ .

## ORDERING GUIDE

Model	Package Description	Shipment Method, Quantity Per Shipping Container	Package Option
AD53500JRP	20-Lead Power SOIC	Tube, 38 Pieces	RP-20

## APPLICATION INFORMATION

### Power Supply Distribution, Bypassing and Sequencing

The AD53500 draws substantial transient currents from its power supplies when switching between states and careful design of the power distribution and bypassing is key to obtaining specified performance. Supplies should be distributed using broad, low inductance traces or (preferably) planes in a multi-layered board with a dedicated ground-plane layer. All of the device's power supply pins should be used to minimize the internal inductance presented by the part's bond wires. Each supply must be bypassed to ground with at least one 0.1  $\mu\text{F}$  capacitor; chip-style capacitors are preferable as they minimize inductance. One or more 10  $\mu\text{F}$  (or greater) Tantalum capacitors per board are also advisable to provide additional local energy storage.

The AD53500's current-limit circuitry also requires external bypass capacitors. Figure 2 shows a simplified schematic of the positive current-limit circuit. Excessive collector current in output transistor Q49 creates a voltage drop across the 5  $\Omega$  resistor, which turns on PNP transistor Q48. Q48 diverts the rising-edge slew current, shutting down the current mirror and removing the output stage's base drive. The  $V_{\text{HDCPL}}$  pin should be bypassed to the positive supply with a 0.039  $\mu\text{F}$  capacitor, while the  $V_{\text{LDCPL}}$  pin (not shown) requires a similar capacitor to the negative supply. These capacitors ensure that the AD53500 does not current-limit during normal output transitions up its full 8 V rated step size. Both capacitors must have minimum-length connections to the AD53500. Here again, chip capacitors are ideal.

Several points about the current-limit circuitry should be noted. First, the limiting currents are not tightly controlled, as they are functions of both absolute transistor  $V_{\text{BE}}$  and junction temperature; higher dc output current is available at lower junction temperatures. Second, it is essential to connect the  $V_{\text{HDCPL}}$

capacitor to the positive supply (and the  $V_{\text{LDCPL}}$  capacitor to the negative supply)—failure to do so causes considerable thermal stress in the current-limiting resistor(s) during normal supply sequencing and may ultimately cause them to fail, rendering the part nonfunctional. Finally, the AD53500 may appear to function normally for small output steps (less than 3 V or so) if one or both of these caps is absent, but it may exhibit excessive rise or fall times for steps of larger amplitude.

The AD53500 does not require special power-supply sequencing. However, good design practice dictates that digital and analog control signals not be applied to the part before the supplies are stable. Violating this guideline will not normally destroy the part, but the active inputs can draw considerable current until the main supplies are applied.

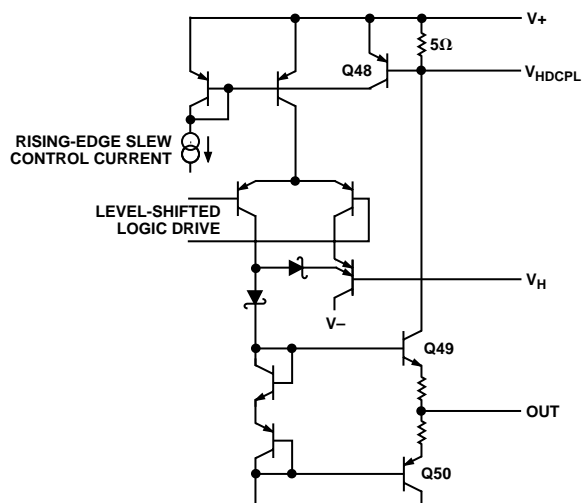
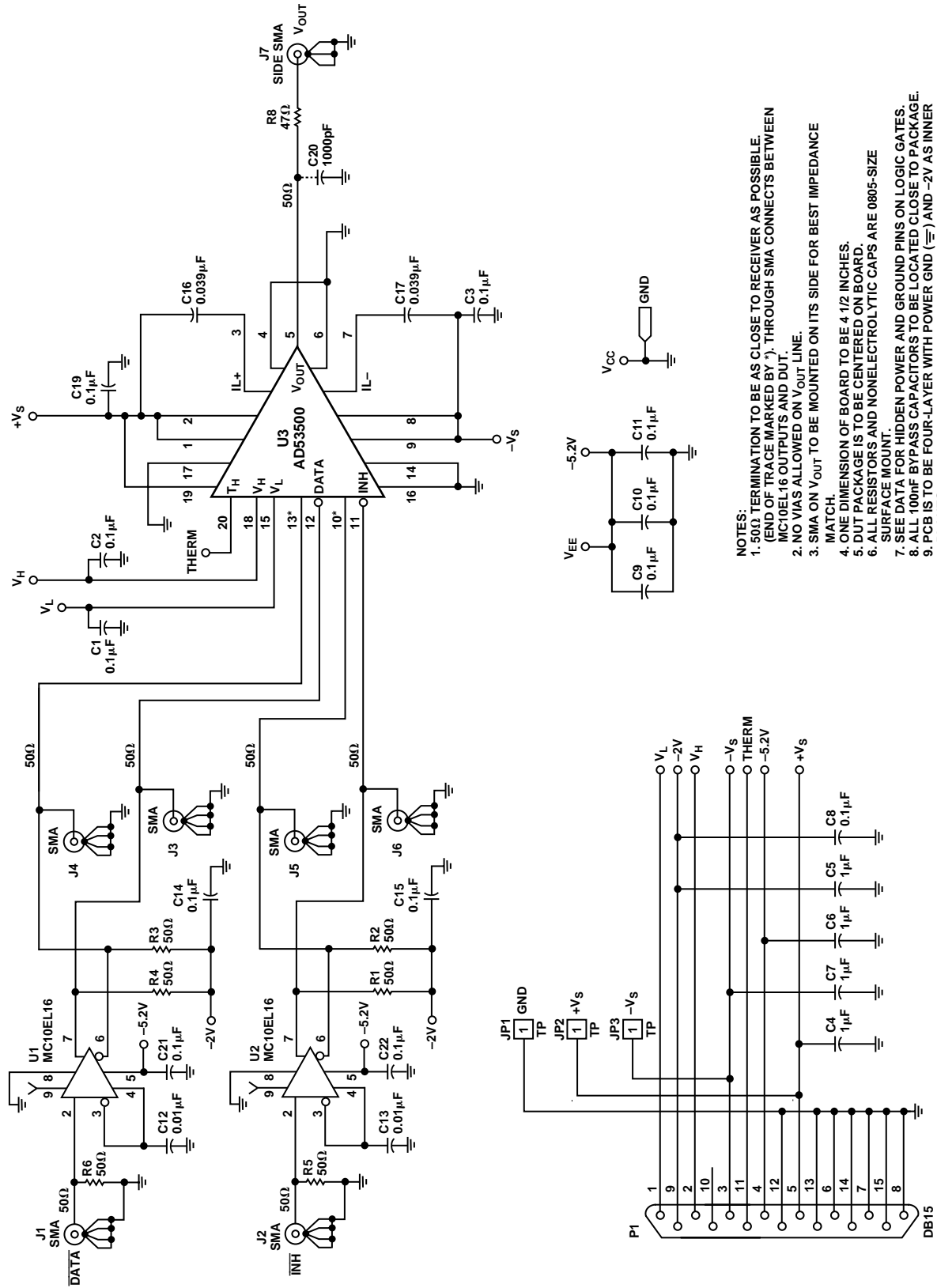


Figure 2. Simplified Schematic of the AD53500 Output Stage and Positive Current-Limit Circuitry



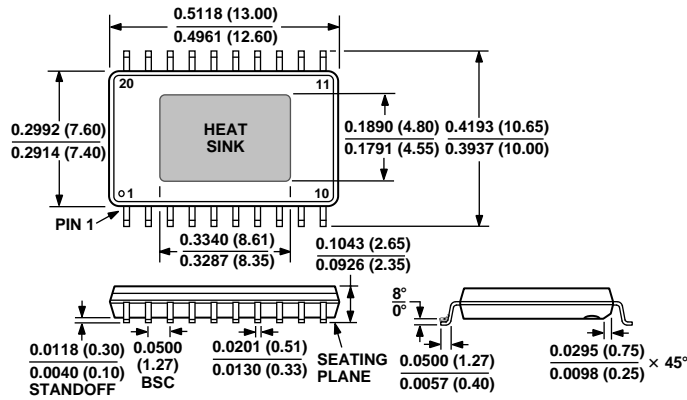
- NOTES:**
1. 50Ω TERMINATION TO BE AS CLOSE TO RECEIVER AS POSSIBLE. (END OF TRACE MARKED BY ♯), THROUGH SMA CONNECTS BETWEEN MC10EL16 OUTPUTS AND DUT.
  2. NO VIAS ALLOWED ON V<sub>OUT</sub> LINE.
  3. SMA ON V<sub>OUT</sub> TO BE MOUNTED ON ITS SIDE FOR BEST IMPEDANCE MATCH.
  4. ONE DIMENSION OF BOARD TO BE 4 1/2 INCHES.
  5. DUT PACKAGE IS TO BE CENTERED ON BOARD.
  6. ALL RESISTORS AND NONELECTROLYTIC CAPS ARE 0805-SIZE SURFACE MOUNT.
  7. SEE DATA FOR HIDDEN POWER AND GROUND PINS ON LOGIC GATES.
  8. ALL 100nF BYPASS CAPACITORS TO BE LOCATED CLOSE TO PACKAGE.
  9. PCB IS TO BE FOUR-LAYER WITH POWER GND (≡) AND -2V AS INNER PLANES.

Figure 3. Evaluation Board Schematic

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**20-Lead Thermally Enhanced Small Outline Package (PSOP)  
(RP-20)**



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