ANALOG DEVICES

8-Bit low cost signal conditioning ADC

AD670

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD670

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD670-703D	8-Bit low cost signal conditioning ADC
AD670-713D	Radiation tested, 8-Bit low cost signal conditioning ADC

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
D	CDIP2-T20	20-Lead ceramic, metal sealed, side-brazed leads

3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

V_{CC} to ground ..... 0V to +7.5V
Digital inputs)Pins 11-15) .....-0.5V to V_{CC} +0.5V
Digital outputs (Pins 1-9) ..... Momentary short to VCD or ground
Analog inputs (Pins 16-19) ..... ±30V
Power dissipation 450mW
Storage temperature range.....-65°C to +150°C
Lead temperature range (soldering) .....+300°C
Operating temperature range.....-55°C to +125°C

3.1 Thermal Characteristics:

Thermal Resistance, Sidebrazed (D) Package

Junction-to-Case (Θ JC) = 25°C/W Max

Junction-to-Ambient (Θ JA) = 85°C/W Max

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Terminal	Function
1	DBO LSB
2	DB1
3	DB2
4	DB3
5	DB4
6	DB5
7	DB6
8	DB7 MSB
9	Status output
10	Power ground
11	BPO/ UPO
12	Format (See note)
13	R/W
14	CS
15	CE
16	$-V_{IN}$ High
17	$-V_{IN}$ Low
18	$+V_{IN}$ High
19	$+V_{IN}$ Low
20	V_{CC}

NOTE: Twos complement or $\overline{straightbinary}$.

Figure 1 - Terminal connections.

$R/\overline{W}$	$\overline{CS}$	$\overline{CE}$	Operation	Output
X	X	X	Converting (see note 1)	Three-state
0	0	0	Write/convert (see note 2)	Three-state
1	0	0	Read (see note 2)	Data valid
X	X	1	None (see note 3)	Three-state
X	1	X	None (see note 3)	Three-state

NOTES:

1. Status output high.
2. Status output low
3. Status output don't care

Figure 2. Control signal truth table.

Mode	Range	Min	Max	Unit
Unipolar	Low	0	255	mV
Unipolar	High	0	2.55	V
Bipolar	Low	-128	+127	mV
Bipolar	High	-1.28	+1.27	V

Figure 3. Differential input signal range truth table.

BPO/ $\overline{UPO}$	Format	Input range/output format
0	0	Unipolar/straight binary
1	0	Bipolar/offset binary
0	1	Unipolar/2's complement
1	1	Bipolar/2's complement

Figure 4. Input selection/output format truth table.

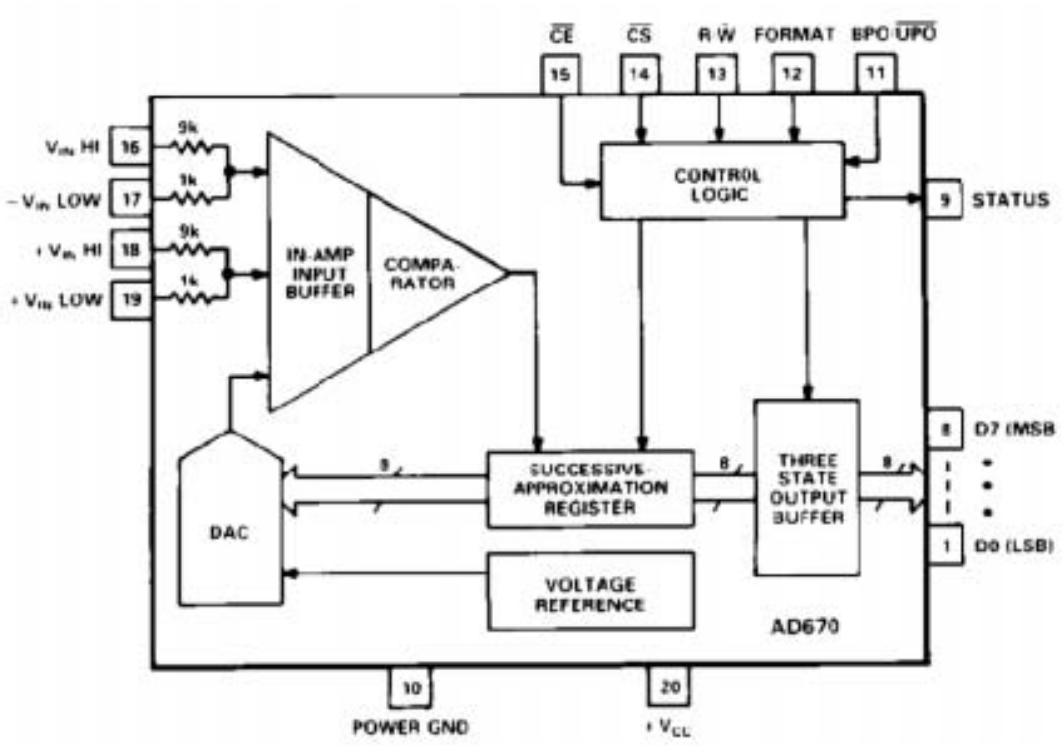

Figure 5. Block diagram

4.0 Electrical Table:

Table I

Parameter See notes at end of table	Symbol	Conditions V_{CC} = +5V	Sub-group	Limit Min	Limit Max	Units
Relative accuracy 1/	RA		1		±½	LSB
			2, 3		±1	
Differential nonlinearity 2/ 3/	DNL		1, 2, 3	8		Bits
Gain Error 1/	A_E		1		±1.5	LSB
			2, 3		±2.5	
Unipolar offset error	O_E	0V to +2.55V input range FS	1		±1	
			2,3		±2	
Bipolar Zero Error	BPZE	-1.28V to +1.27V FS	1		±1	
			2, 3		±2	
Input resistance 3/	R_{IN}	2.55V input range	1	8	12	KΩ
Input bias current 3/	I_B	255 mV input range	1, 2, 3		±750	nA
Input offset current 3/	I_{OS}	255 mV input range	1, 2, 3		±200	
Absolute input signal range 3/ 4/ 5/	V_{ABS}	Low range	1	-0.34	V_{CC}-3.3V	V
			2, 3	-.15	V_{CC} - 3.5V	
		High range	1	-3.4	V_{CC}	
			2, 3	-1.5	V_{CC}	
Power supply rejection ratio	PSRR	2.55V FS, V_{CC} = +4.75V to +5.5V	1, 2, 3		±0.015	%FS/%
Power supply current	I_{CC}	V_{CC} = 5.5V (DBO-DB7, R/W - high); (STATUS, CE, CS, FORMAT, BPO, UPO - LOW)	1, 2, 3		45	mA
Digital input high voltage 3/	V_{IH}		1, 2, 3	2.0		V
Digital input low voltage 3/	V_{IL}		1		0.8	
			2, 3		0.7	
Digital input high current 3/	I_{IH}	V_{IH} = 5V	1, 2, 3		100	µA
Digital input low current 3/	I_{IL}	V_{IL} = 0V	1, 2, 3		-100	
Digital output low voltage	V_{OL}	I_{OL} = 1.6mA, V_{CC} = 5.5V	1, 2, 3		0.4	V
Digital output high voltage	V_{OH}	I_{OH} = 0.5mA, V_{CC} = 4.5V	1, 2, 3	2.4		
Digital output low current	I_{OL}	V_{OL} = 0.4V, V_{CC} = 5.5V	1, 2, 3	-1.6		mA
Digital output high current	I_{OH}	V_{OH} = 2.4V, V_{CC} = 4.5V	1, 2, 3	0.5		
Common mode rejection ratio 3/ 7/	CMRR	V_{CM} = -0.34V to (V_{CC} -3.6V)	1		±1	LSB
		V_{CM} = -0.15V to (V_{CC} -3.8V)	2, 3		±2	
Three-state leakage current 3/	I_{OZ}	$V_{applied}$ = 0V & 5V	1, 2, 3		±40	µA
Functional tests 8/			7, 8			

Table I (continued)							
Parameter See notes at end of table	Symbol	Conditions V_{CC} = +5V		Sub-group	Limit Min	Limit Max	Units
Bus access time 3/	t_{TD}	See fig. 5, R_L = 3KΩ, C_L = 90pF		9		250	nS
Output float delay 3/	t_{DT}	See fig. 5, R_L = 3KΩ				150	
Write/start pulse width 3/	t_W	See fig. 6, R_L = 3KΩ, C_L = 90pF			300		
Input data setup time	t_{DS}	6/			200		
Input data hold time	t_{DH}				10		
R/W setup before control	t_{RWC}				0		
Delay to convert start	t_{DC}					700	
Delay from STATUS OUTPUT to data read	t_{SD}					250	
Data hold time	t_{DH}				25		
Conversion time 3/	t_C	V_{CC} = +5V		9		10	µS
			6/	10, 11		13	

TABLE I NOTES:

1/ Tested on both 2.55V full scale and -1.28V to 1.27V full scale.
2/ Minimum resolution for which there are no missing codes.
3/ Parameter is tested at V_{CC} = +5V, but is guaranteed from V_{CC} = 4.5V to V_{CC} = 5.5V
4/ The absolute input signal range defines the limits of input signal value from either the (+) or (-) input to ground (as a function of V_{CC}) over which the device will produce distinct output codes.
5/ The differential input signal range defines the input signal span over which distinct output codes are produced. As this range is exceeded, the device ceases to change output state (see fig. 4).
6/ Guaranteed, if not tested, to the specified limits.
7/ 255 mV range. CMRR tested with 0V and full scale applied to analog inputs output change measured from 0 to VCM maximum and 0 to VCM minimum and will not exceed specified limits.
8/ Subgroups 7 and 8 shall include verification of the truth table. (Fig. 3 and Fig. 4)

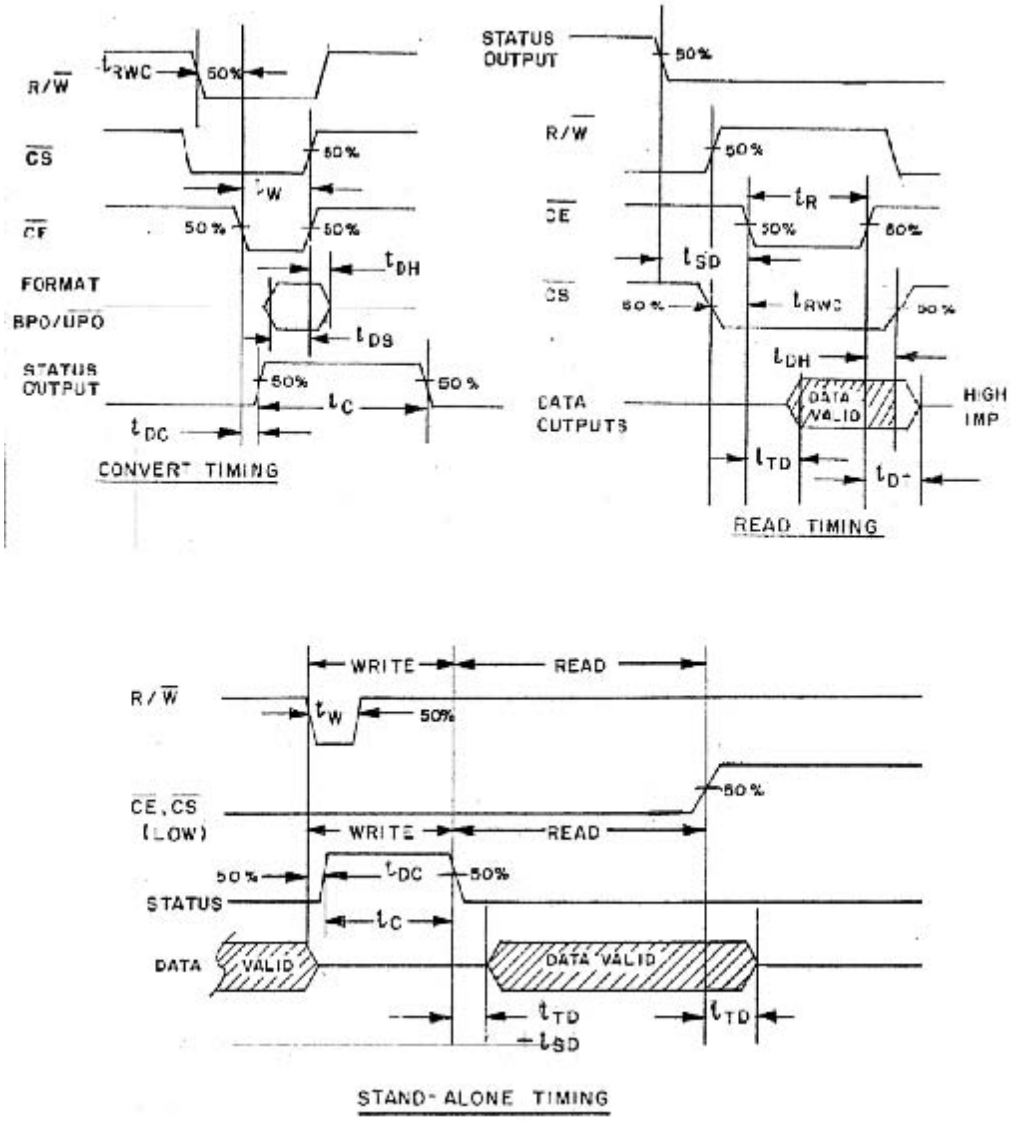

Figure 6. Timing diagram

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 7, 8, 9 1/ 2/
Group A Test Requirements	1, 2, 3, 7, 8, 9
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

1/ PDA applies to Subgroup 1. Delta's excluded from PDA.
2/ See Table III for delta parameters. See table I for conditions.

4.2 Table III. Lifetest / Burn-in delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
A_E	±1.5	±1.5	±1.5	LSB
V_{OS}	±1	±1	±1	LSB
B_{PZE}	±1	±1	±1	LSB

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition D.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Aug. 9, 2000
B	Various corrections made to Table I to make compatible with 883. SMD has errors. Correct BI to dynamic. Update Table III.	Sept. 17, 2001
C	Update web address, BI condition is D	Jan. 25, 2002
D	Change BP2E to BPZE on table III (typo) Change Table I BOE to BPZE	Nov. 27, 2002
E	Update web address. Delete burn-in circuit	Jun. 20, 2003
F	Update header/footer & add to 1.0 Scope description.	Feb. 25, 2008

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