12-Bit, 105 MSPS/125 MSPS, IF Sampling ADC

AD9433

FEATURES

- IF sampling up to 350 MHz
- SNR: 67.5 dB, f_{IN} up to Nyquist at 105 MSPS
- SFDR: 83 dBc, f_{IN} = 70 MHz at 105 MSPS
- SFDR: 72 dBc, f_{IN} = 150 MHz at 105 MSPS
- 2 V p-p analog input range
- On-chip clock duty cycle stabilization
- On-chip reference and track-and-hold
- SFDR optimization circuit
- Excellent linearity
  - DNL: ±0.25 LSB (typical)
  - INL: ±0.5 LSB (typical)
- 750 MHz full power analog bandwidth
- Power dissipation: 1.35 W (typical) at 125 MSPS
- Twos complement or offset binary data format
- 5.0 V analog supply operation
- 2.5 V to 3.3 V TTL/CMOS outputs

APPLICATIONS

- Cellular infrastructure communication systems
  - 3G single- and multicarrier receivers
  - IF sampling schemes
- Wideband carrier frequency systems
  - Point-to-point radios
  - LMDS, wireless broadband
  - MMDS base station units
  - Cable reverse path
- Communications test equipment
- Radar and satellite ground systems

GENERAL INTRODUCTION

The AD9433 is a 12-bit, monolithic sampling analog-to-digital converter (ADC) with an on-chip track-and-hold circuit and is designed for ease of use. The product operates up to a 125 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband and high IF carrier systems.

The ADC requires a 5 V analog power supply and a differential encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL-/CMOS-compatible, and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

FUNCTIONAL BLOCK DIAGRAM

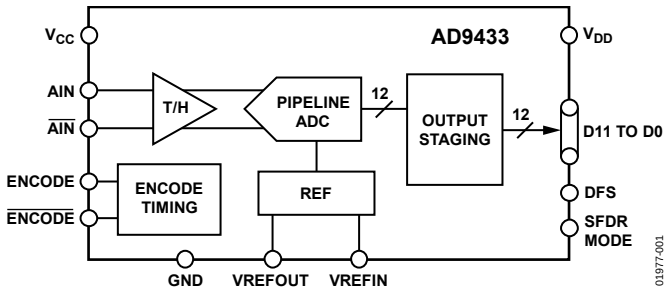

Figure 1.

A user-selectable, on-chip proprietary circuit optimizes spurious-free dynamic range (SFDR) vs. signal-to-noise and distortion (SINAD) ratio performance for different input signal frequencies, providing as much as 83 dBc SFDR performance over the dc to 70 MHz band.

The encode clock supports either differential or single-ended input and is PECL-compatible. The output format is user-selectable for offset binary or twos complement and provides an overrange (OR) signal.

Fabricated on an advanced BiCMOS process, the AD9433 is available in a 52-lead thin quad flat package (TQFP_EP) that is specified over the industrial temperature range of −40°C to +85°C. The AD9433 is pin-compatible with the AD9432.

PRODUCT HIGHLIGHTS

1. IF Sampling.
   The AD9433 maintains outstanding ac performance up to input frequencies of 350 MHz. Suitable for 3G wideband cellular IF sampling receivers.
2. Pin-Compatibility with the AD9432.
   The AD9433 has the same footprint and pin layout as the AD9432 12-bit 80 MSPS/105 MSPS ADC.
3. SFDR Performance.
   A user-selectable, on-chip circuit optimizes SFDR performance as much as 83 dBc from dc to 70 MHz.
4. Sampling Rate.
   At 125 MSPS, the AD9433 is ideally suited for wireless and wired broadband applications such as LMDS/MMDS and cable reverse path.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

6/09—Rev. 0 to Rev. A

Updated Format ..... Universal
Reorganized Layout ..... Universal
Added TQFP_EP Package ..... Universal
Deleted LQFP_ED Package ..... Universal
Changes to Thermal Characteristics Section 6
Changes to Pin Configuration and Function Descriptions Section 7
Deleted Evaluation Board Section 16
Updated Outline Dimensions 20
Changes to Ordering Guide 20

10/01—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

V_{DD} = 3.3 V, V_{CC} = 5 V; internal reference; differential encode input, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	105 MSPS Min	105 MSPS Typ	105 MSPS Max	125 MSPS Min	125 MSPS Typ	125 MSPS Max	Unit
RESOLUTION				12			12		Bits
ACCURACY									
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Offset Error	Full	VI	−5	0	+5	−5	0	+5	mV
Gain Error[1]	25°C	I	−7	±1	+3	−7	±1	+3	% FS
Differential Nonlinearity (DNL)[2]	25°C	I	−0.75	±0.25	+0.75	−0.75	±0.3	+0.75	LSB
	Full	VI	−1		+1	−1		+1	LSB
Integral Nonlinearity (INL)[2]	25°C	I	−1.0	±0.5	+1.0	−1.0	±0.5	+1.0	LSB
	Full	VI	−1.3		+1.3	−1.3		+1.3	LSB
THERMAL DRIFT									
Offset Error	Full	V		−50			−50		ppm/°C
Gain Error[1]	Full	V		−125			−125		ppm/°C
Reference	Full	V		±80			±80		ppm/°C
REFERENCE									
Internal Reference Voltage (VREFOUT)	Full	I	2.4	2.5	2.6	2.4	2.5	2.6	V
Output Current (VREFOUT)	Full	V		100			100		µA
Input Current (VREFIN)	Full	IV			50			50	µA
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Input Voltage Range	Full	V		2.0			2.0		V p-p
Common-Mode Voltage	Full	V		4.0			4.0		V
Input Resistance	Full	VI	2	3	4	2	3	4	kΩ
Input Capacitance	Full	V		4			4		pF
Analog Bandwidth, Full Power	Full	V		750			750		MHz
POWER SUPPLY									
V_{CC}	Full	IV	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{DD}	Full	IV	2.7		3.3	2.7		3.3	V
Power Dissipation[3]	Full	VI		1275	1425		1350	1500	mW
I_{VCC}[3]	Full	VI		255	285		270	300	mA
I_{VDD}[3]	Full	VI		12.5	14		16	18	mA
Power Supply Rejection Ratio (PSRR)	25°C	I		±3			±3		mV/V
ENCODE INPUTS									
Internal Common-Mode Bias	Full	V		3.75			3.75		V
Differential Input (ENCODE, $\overline{ENCODE}$)	Full	V		500			500		mV
Input Voltage Range	Full	IV	−0.5		V_{CC} + 0.05	−0.5		V_{CC} + 0.05	V
Input Common-Mode Range	Full	IV	2.0		4.25	2.0		4.25	V
Input Resistance	Full	VI		6			6		kΩ
Input Capacitance	25°C	V		3			3		pF
DIGITAL INPUTS									
Input High Voltage	Full	I	2.0			2.0			V
Input Low Voltage	Full	I			0.8			0.8	V
Input High Current (VIN = 5 V)	Full	V		50			50		µA
Input Low Current (VIN = 0 V)	Full	V		50			50		µA

Parameter	Temp	Test Level	105 MSPS Min	105 MSPS Typ	105 MSPS Max	125 MSPS Min	125 MSPS Typ	125 MSPS Max	Unit
DIGITAL OUTPUTS									
Logic 1 Voltage	Full	VI	V_{DD} – 0.05			V_{DD} – 0.05			V
Logic 0 Voltage	Full	VI			0.05			0.05	V
Output Coding			Twos complement or offset binary			Twos complement or offset binary			

[1] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 2.5 V external reference and a 2 V p-p differential analog input).
[2] SFDR mode disabled (SFDR MODE = GND) for DNL and INL specifications.
[3] Power dissipation measured with rated encode and a dc analog input (outputs static, I_{VDD} = 0). I_{VCC} and I_{VDD} measured with 10.3 MHz analog input @ –0.5 dBFS.

AC SPECIFICATIONS

V_{DD} = 3.3 V, V_{CC} = 5 V; differential encode input, unless otherwise noted.

Table 2.

Parameter	Temp	Test Level	105 MSPS Min	105 MSPS Typ	105 MSPS Max	125 MSPS Min	125 MSPS Typ	125 MSPS Max	Unit
DYNAMIC PERFORMANCE[1]									
Signal-to-Noise Ratio (SNR) (Without Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	66.5	68.0		66.0	67.7		dB
f_{IN} = 49 MHz	25°C	I	65.5	67.5		64.0	66.0		dB
f_{IN} = 70 MHz	25°C	V		67.0			65.4		dB
f_{IN} = 150 MHz	25°C	V		65.4			62.0		dB
f_{IN} = 250 MHz	25°C	V		63.7			60.0		dB
Signal-to-Noise and Distortion (SINAD) Ratio (with Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	66.0	68.0		65.0	67.0		dB
f_{IN} = 49 MHz	25°C	I	64.0	67.5		63.5	65.5		dB
f_{IN} = 70 MHz	25°C	V		66.9			64.5		dB
f_{IN} = 150 MHz	25°C	V		64.0			61.5		dB
f_{IN} = 250 MHz	25°C	V		61.2			57.7		dB
Effective Number of Bits (ENOB)									
f_{IN} = 10.3 MHz	25°C	I		11.1			10.9		Bits
f_{IN} = 49 MHz	25°C	I		11.0			10.7		Bits
f_{IN} = 70 MHz	25°C	V		10.9			10.6		Bits
f_{IN} = 150 MHz	25°C	V		10.4			10.0		Bits
f_{IN} = 250 MHz	25°C	V		9.9			9.4		Bits
Second-Order and Third-Order Harmonic Distortion									
f_{IN} = 10.3 MHz	25°C	I	–78	–85		–76	–85		dBc
f_{IN} = 49 MHz	25°C	I	–73	–80		–72	–76		dBc
f_{IN} = 70 MHz	25°C	V		–83			–78		dBc
f_{IN} = 150 MHz	25°C	V		–72			–67		dBc
f_{IN} = 250 MHz	25°C	V		–67			–65		dBc
Worst Other Harmonic or Spur (Excluding Second-Order and Third-Order Harmonics)									
f_{IN} = 10.3 MHz	25°C	I	–88	–92		–84	–90		dBc
f_{IN} = 49 MHz	25°C	I	–82	–89		–82	–87		dBc
f_{IN} = 70 MHz	25°C	V		–87			–85		dBc
f_{IN} = 150 MHz	25°C	V		–87			–84		dBc
f_{IN} = 250 MHz	25°C	V		–85			–76		dBc
Two-Tone Intermodulation Distortion (IMD3)									
f_{IN1} = 49.3 MHz; f_{IN2} = 50.3 MHz	25°C	V		–92			–90		dBc
f_{IN1} = 150 MHz; f_{IN2} = 151 MHz	25°C	V		–80			–76		dBc

[1] SNR/harmonics based on an analog input voltage of –0.5 dBFS referenced to a 2 V full-scale input range. Harmonics are specified with the SFDR mode enabled (SFDR MODE = 5 V). SNR/SINAD specified with the SFDR mode disabled (SFDR MODE = ground).

SWITCHING SPECIFICATIONS

V_{DD} = 3.3 V, V_{CC} = 5 V; differential encode input, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	105 MSPS Min	105 MSPS Typ	105 MSPS Max	125 MSPS Min	125 MSPS Typ	125 MSPS Max	Unit
Encode Rate	Full	IV	10		105	10		125	MSPS
Encode Pulse Width High (t_{EH})	Full	IV	2.9			2.4			ns
Encode Pulse Width Low (t_{EL})	Full	IV	2.9			2.4			ns
Aperture Delay (t_A)	25°C	V		2.1			2.1		ns
Aperture Uncertainty (Jitter)[1]	25°C	V		0.25			0.25		ps rms
Output Valid Time (t_V)[2]	Full	VI	2.5	4.0		2.5	4.0		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		4.0	5.5		4.0	5.5	ns
Output Rise Time (t_R)[2]	Full	V		2.1			2.1		ns
Output Fall Time (t_F)[2]	Full	V		1.9			1.9		ns
Out-of-Range Recovery Time	25°C	V		2			2		ns
Transient Response Time	25°C	V		2			2		ns
Latency	Full	IV		10			10		Cycles

[1] Aperture uncertainty includes contribution of the AD9433, crystal clock reference, and encode drive circuit.
[2] t_V and t_{PD} are measured from the transition points of the ENCODE input to the 50%/50% levels of the digital output swing. The digital output load during testing is not to exceed an ac load of 10 pF or a dc current of 50 µA. Rise and fall times are measured from 10% to 90%.

TIMING DIAGRAM

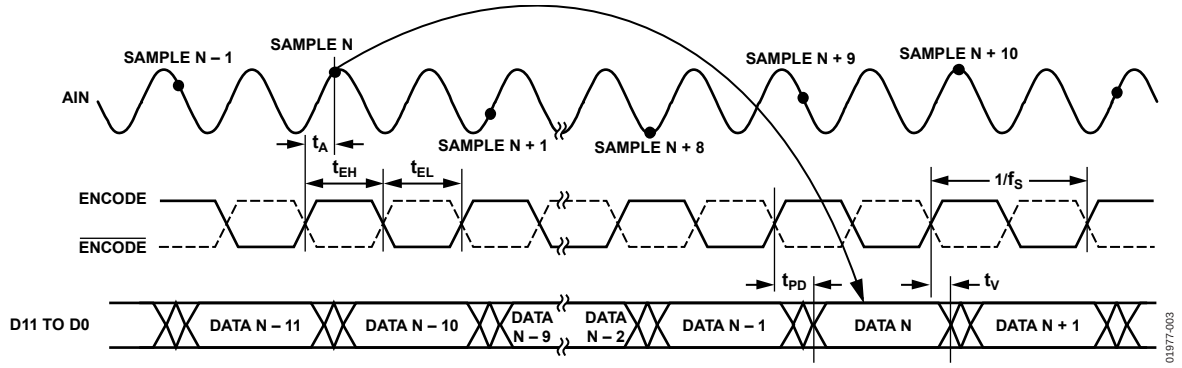


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD}	−0.5 V to +6.0 V
V_{CC}	−0.5 V to +6.0 V
Analog Inputs	−0.5 V to V_{CC} + 0.5 V
Digital Inputs	−0.5 V to V_{DD} + 0.5 V
Digital Output Current	20 mA
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature (T_J)	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I 100% production tested.
II 100% production tested at 25°C and sample tested at specified temperatures.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Parameter is a typical value only.
VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range.

THERMAL CHARACTERISTICS

Table 5 lists AD9433 thermal characteristics for simulated typical performance in a 4-layer JEDEC board, horizontal orientation.

Table 5. Thermal Resistance

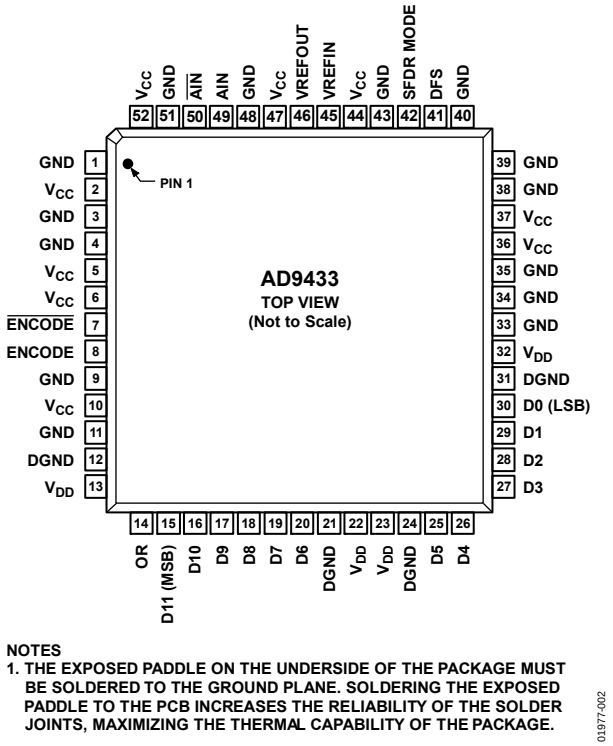
Package Type	θ_{JA}	θ_{JMA}	θ_{JC}	Unit
52-Lead TQFP_EP (SV-52-2)[1]			2	°C/W
No Airflow	19.3			°C/W
1.0 m/s Airflow		16		°C/W

[1] Bottom of package (exposed pad soldered to ground plane).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE ON THE UNDERSIDE OF THE PACKAGE MUST BE SOLDERED TO THE GROUND PLANE. SOLDERING THE EXPOSED PADDLE TO THE PCB INCREASES THE RELIABILITY OF THE SOLDER JOINTS, MAXIMIZING THE THERMAL CAPABILITY OF THE PACKAGE.

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Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 9, 11, 33, 34, 35, 38, 39, 40, 43, 48, 51	GND	Analog Ground.
2, 5, 6, 10, 36, 37, 44, 47, 52	V_{CC}	Analog Supply (5 V).
7	$\overline{\text{ENCODE}}$	Encode Clock for ADC, Complementary.
8	ENCODE	Encode Clock for ADC, True. ADC samples on rising edge of ENCODE.
12, 21, 24, 31	DGND	Digital Output Ground.
13, 22, 23, 32	V_{DD}	Digital Output Power Supply (3 V).
14	OR	Out-of-Range Output.
15 to 20, 25 to 30	D11 to D6, D5 to D0	Digital Output.
41	DFS	Data Format Select. Logic low = twos complement, logic high = offset binary; floats low.
42	SFDR MODE	CMOS Control Pin. This pin enables SFDR mode, a proprietary circuit that can improve the SFDR performance of the AD9433. SFDR mode is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by nonlinearities in the ADC transfer function. Set this pin to 0 for normal operation; floats low.
45	VREFIN	Reference Input for ADC (2.5 V Typical). Bypass with 0.1 µF capacitor to ground.
46	VREFOUT	Internal Reference Output (2.5 V Typical).
49	AIN	Analog Input, True.
50	$\overline{\text{AIN}}$	Analog Input, Complementary.
	Exposed Pad (EP)	The exposed paddle on the underside of the package must be soldered to the ground plane. Soldering the exposed paddle to the PCB increases the reliability of the solder joints, maximizing the thermal capability of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

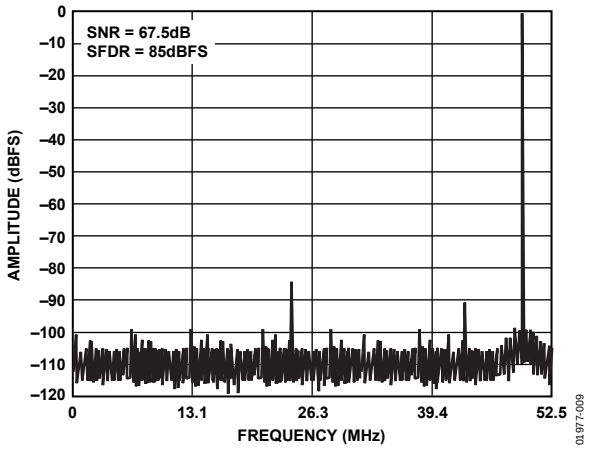

Figure 4. FFT: f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Mode Enabled

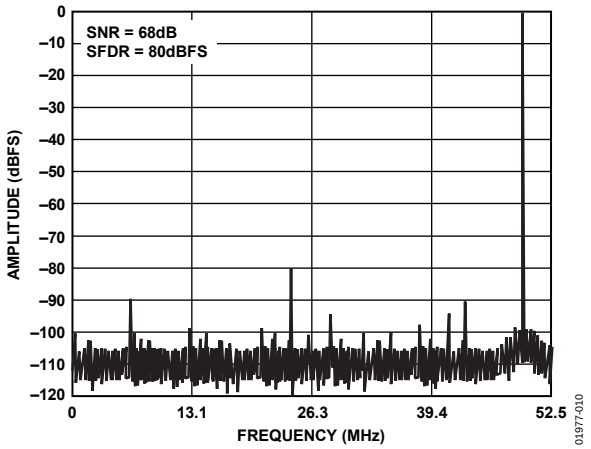

Figure 5. FFT: f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Mode Disabled

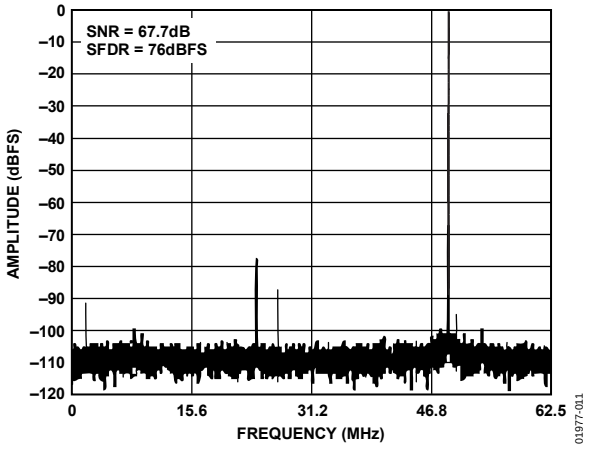

Figure 6. FFT: f_S = 125 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ –0.5 dBFS, SFDR Mode Enabled

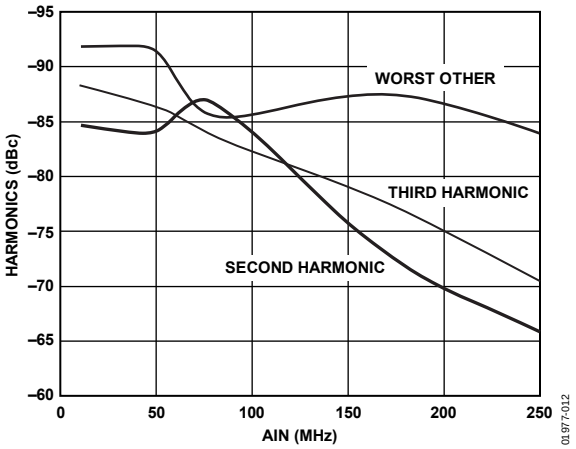

Figure 7. Harmonics (Second, Third, Worst Other) vs. AIN Frequency, AIN @ –0.5 dBFS, f_S = 105 MSPS, SFDR Mode Enabled

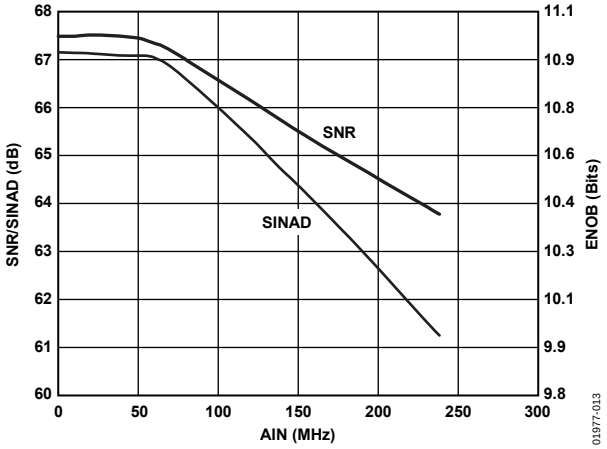

Figure 8. SNR/SINAD and ENOB vs. AIN Frequency, Differential AIN @ –0.5 dBFS, f_S = 105 MSPS, SFDR Mode Disabled

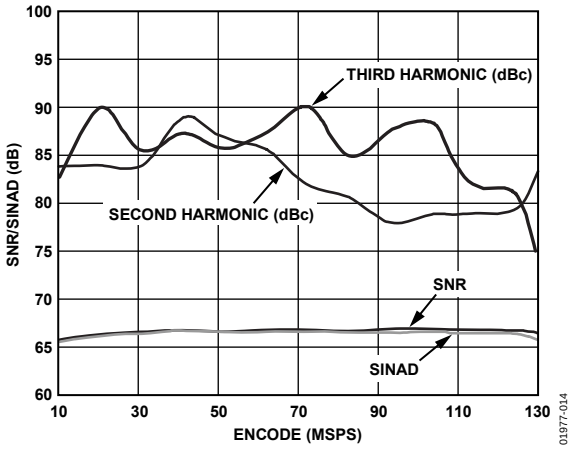

Figure 9. SNR/SINAD and Harmonic Distortion vs. Encode Frequency, Differential AIN @ –0.5 dBFS

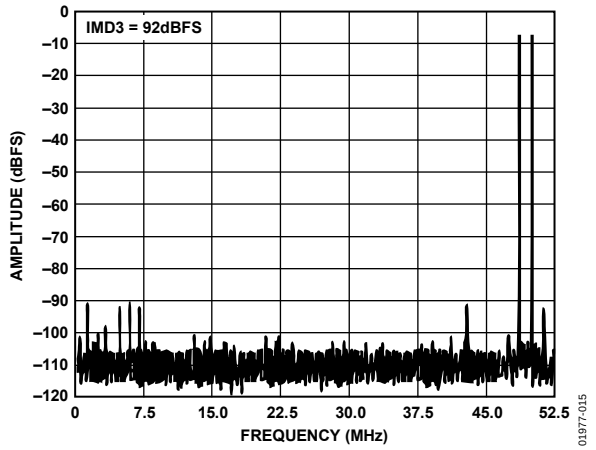

Figure 10. FFT: f_S = 105 MSPS, f_{IN} = 49.3 MHz and 50.3 MHz, Differential AIN @ −7 dBFS for Each Tone, SFDR Mode Enabled

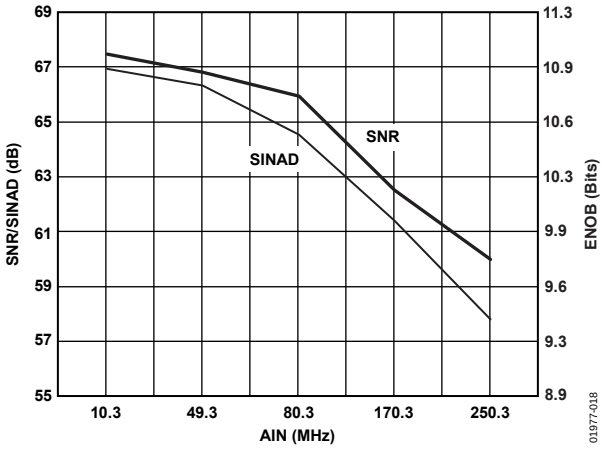

Figure 13. SNR/SINAD and ENOB vs. AIN Frequency, Differential AIN @ −0.5 dBFS, f_S = 125 MSPS, SFDR Mode Enabled

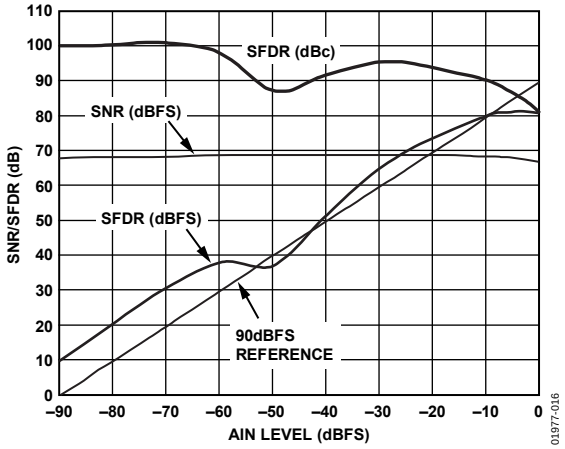

Figure 11. SNR and SFDR vs. AIN Level, f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN, SFDR Mode Enabled

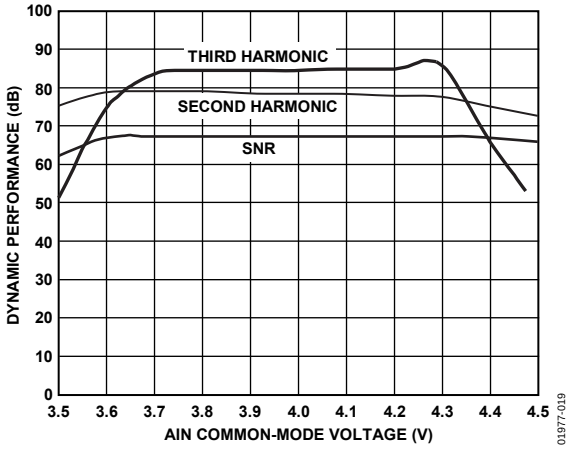

Figure 14. Dynamic Performance vs. AIN Common-Mode Voltage, Differential AIN @ −0.5 dBFS, f_{IN} = 49.3 MHz, f_S = 105 MSPS

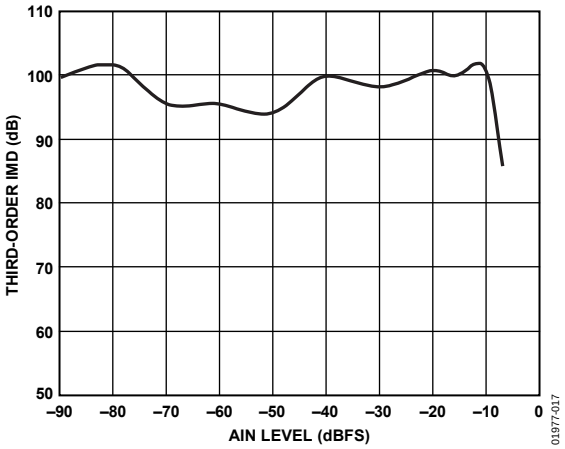

Figure 12. Third-Order IMD vs. AIN Level, f_S = 105 MSPS, f_{IN} = 49.3 MHz and 50.3 MHz, Differential AIN, SFDR Mode Enabled

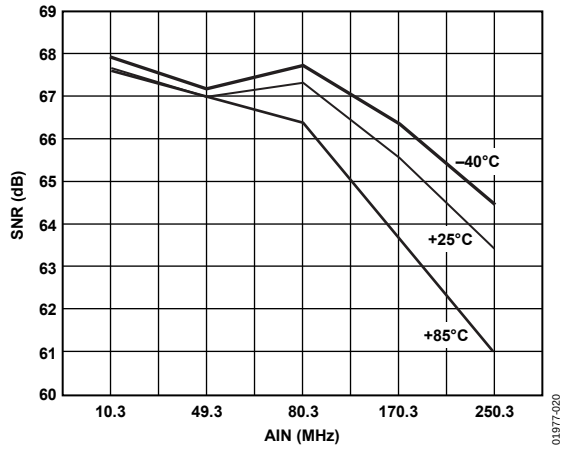

Figure 15. SNR vs. AIN Frequency over Temperature, f_S = 105 MSPS, Differential AIN, SFDR Mode Disabled

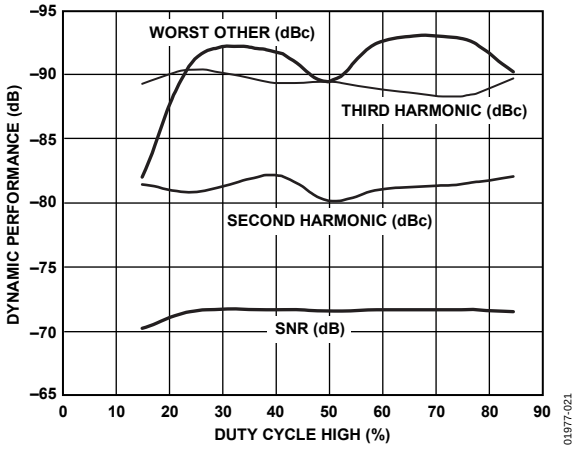

Figure 16. Dynamic Performance vs. Encode Duty Cycle, f_S = 105 MSPS, f_{IN} = 49.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

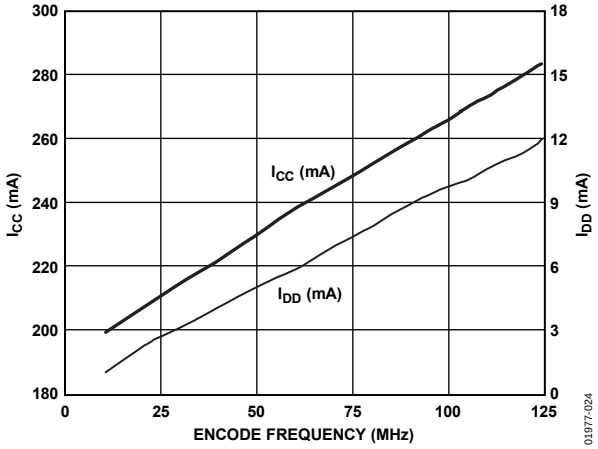

Figure 19. I_{DD} and I_{CC} vs. Encode Rate, f_{IN} = 10.3 MHz, Differential AIN @ −0.5 dBFS

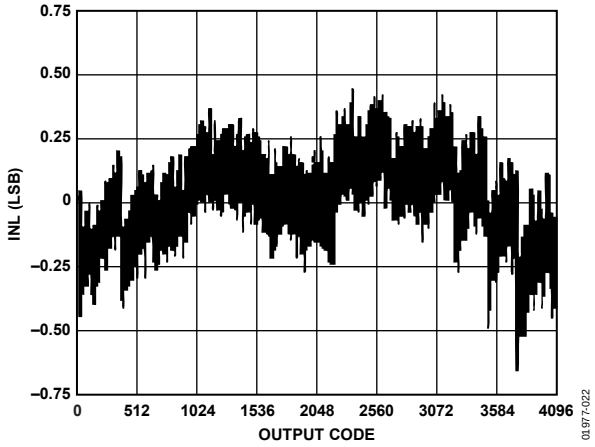

Figure 17. Integral Nonlinearity vs. Output Code with SFDR Mode Disabled

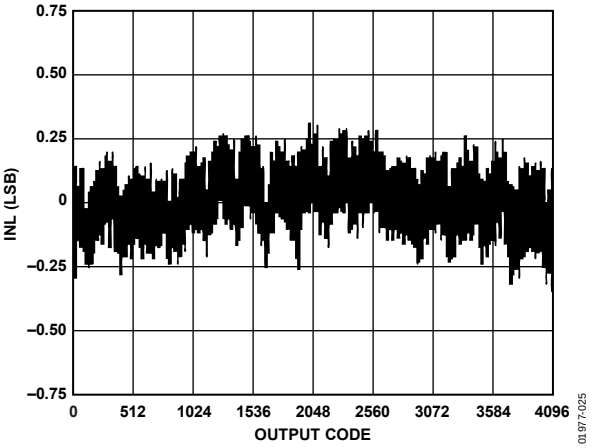

Figure 20. Integral Nonlinearity vs. Output Code with SFDR Mode Enabled

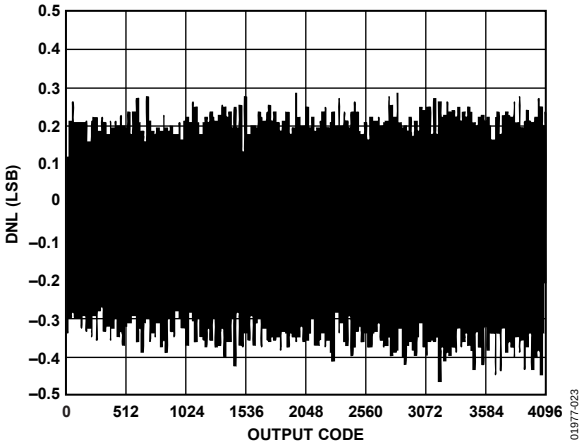

Figure 18. Differential Nonlinearity vs. Output Code

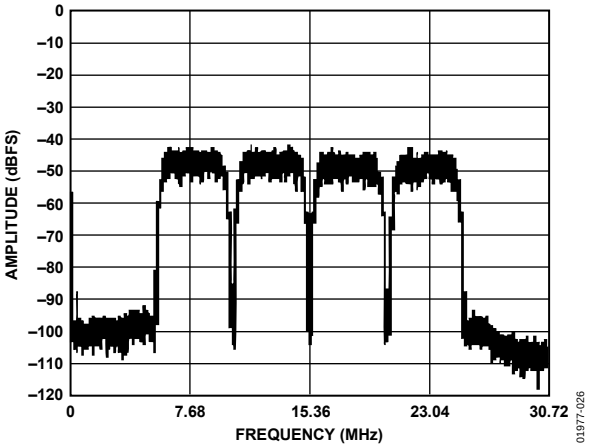

Figure 21. FFT: f_S = 61.44 MSPS, f_{IN} = 46.08 MHz, Four WCDMA Carriers, Differential AIN, SFDR Mode Enabled

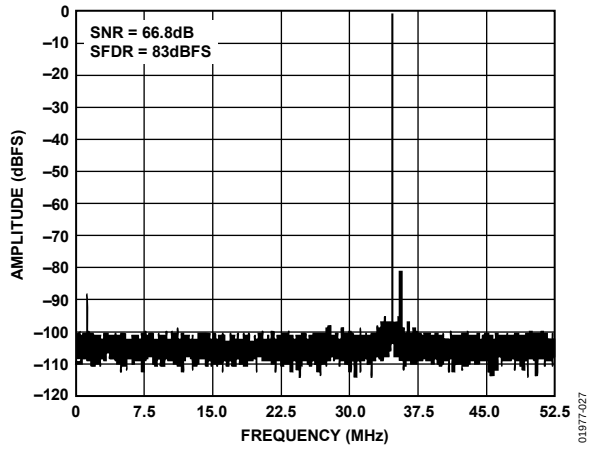

Figure 22. FFT: f_S = 105 MSPS, f_{IN} = 70.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

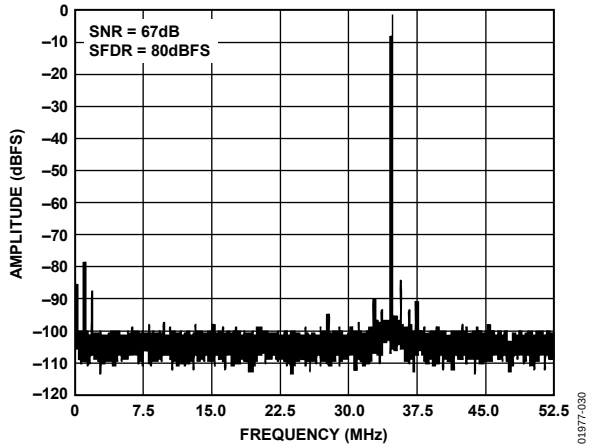

Figure 23. FFT: f_S = 105 MSPS, f_{IN} = 70.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Disabled

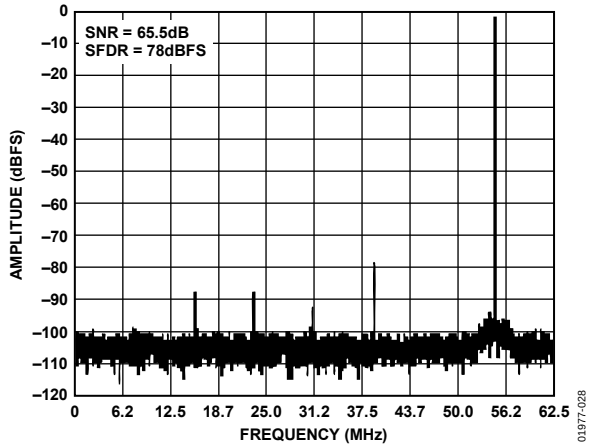

Figure 24. FFT: f_S = 125 MSPS, f_{IN} = 70.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

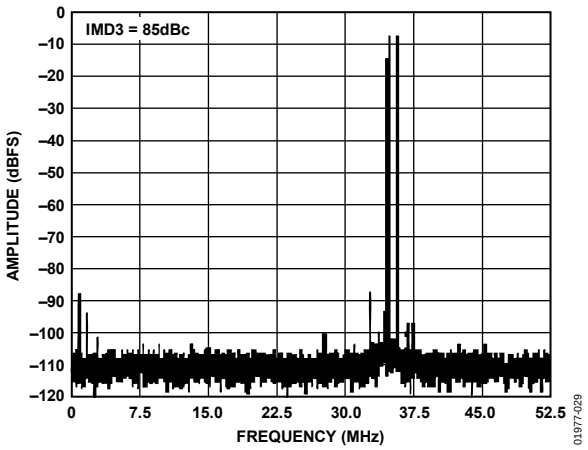

Figure 25. FFT: f_S = 105 MSPS, f_{IN} = 69.3 MHz and 70.3 MHz, Differential AIN @ −7 dBFS for Each Tone, SFDR Mode Enabled

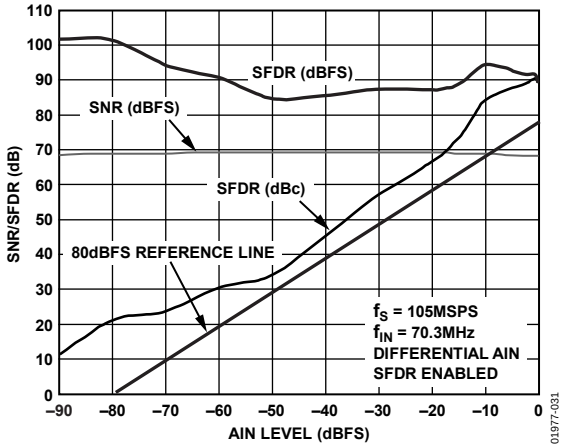

Figure 26. SNR and SFDR vs. AIN Level, f_S = 105 MSPS, f_{IN} = 70.3 MHz, Differential AIN, SFDR Mode Enabled

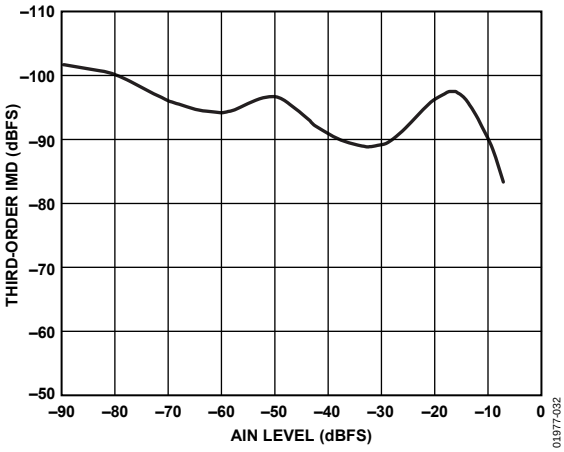

Figure 27. Third-Order IMD vs. AIN Level, f_S = 105 MSPS, f_{IN} = 70.3 MHz and 69.3 MHz, Differential AIN, SFDR Mode Enabled

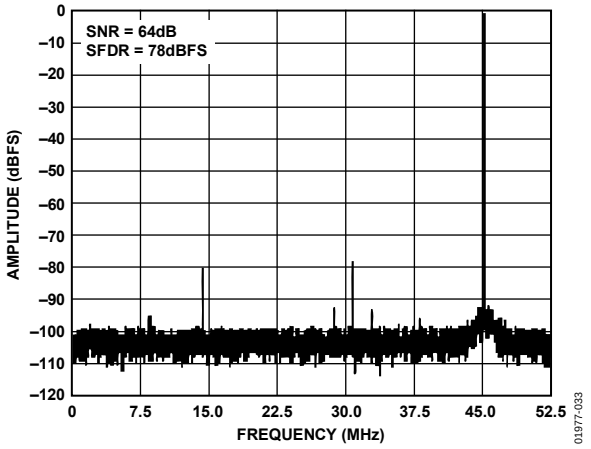

Figure 28. FFT: f_S = 105 MSPS, f_{IN} = 150.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

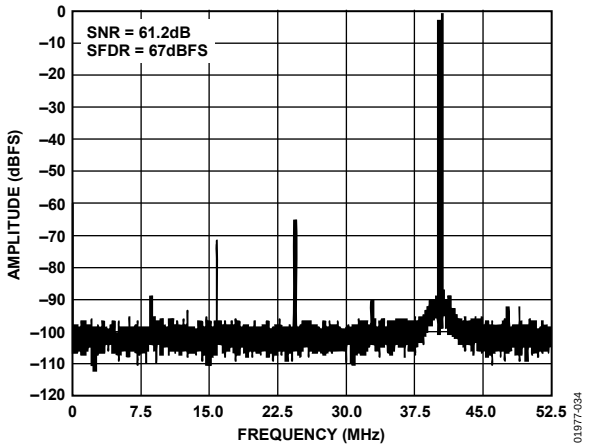

Figure 29. FFT: f_S = 105 MSPS, f_{IN} = 250.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

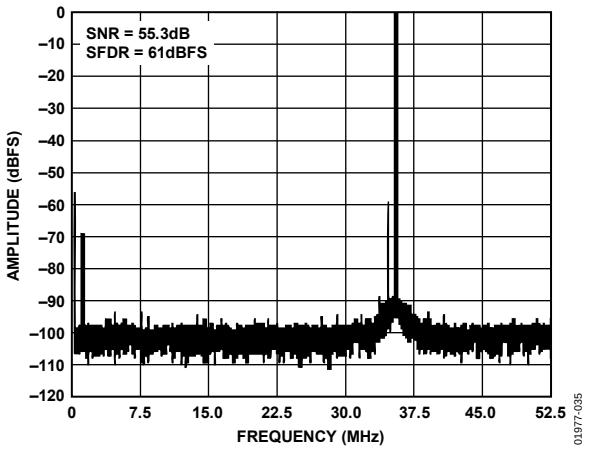

Figure 30. FFT: f_S = 105 MSPS, f_{IN} = 350.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

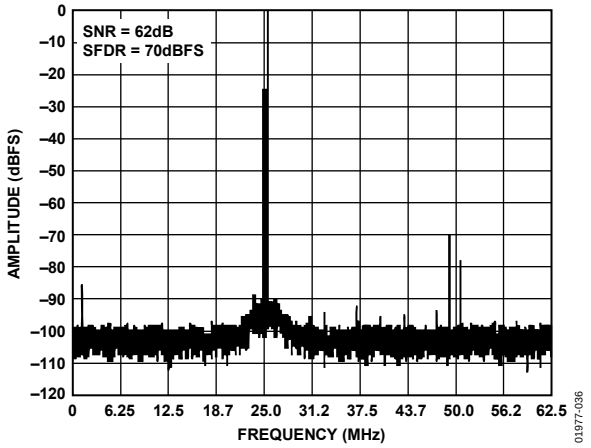

Figure 31. FFT: f_S = 125 MSPS, f_{IN} = 150.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

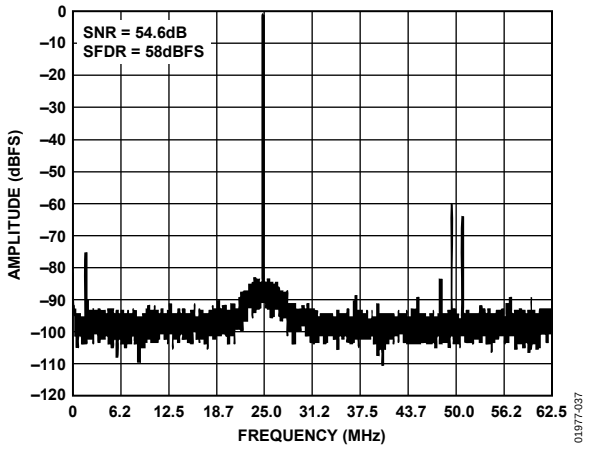

Figure 32. FFT: f_S = 125 MSPS, f_{IN} = 350.3 MHz, Differential AIN @ −0.5 dBFS, SFDR Mode Enabled

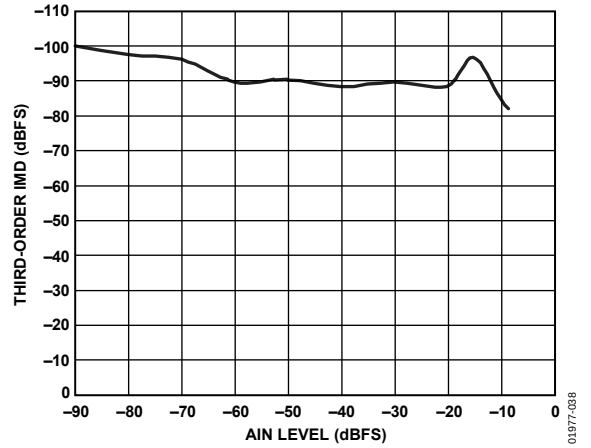

Figure 33. Third-Order IMD vs. AIN Level, f_S = 105 MSPS, f_{IN} = 150.3 MHz and 151.3 MHz, Differential AIN, SFDR Mode Enabled

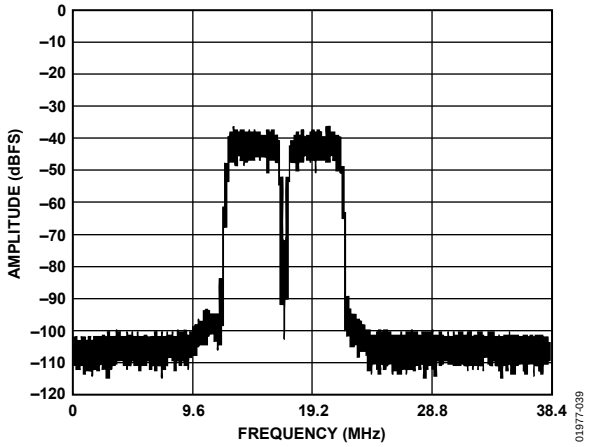

Figure 34. FFT: f_S = 76.8 MSPS, f_{IN} = 59.6 MHz, Two WCDMA Carriers, Differential AIN, SFDR Mode Enabled

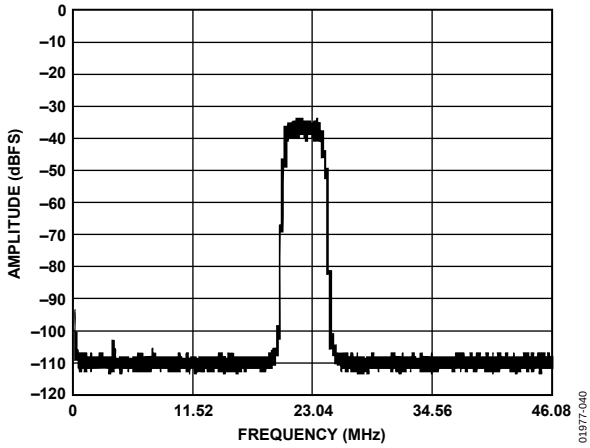

Figure 35. FFT: f_S = 92.16 MSPS, f_{IN} = 70.3 MHz, WCDMA @ 70.0 MHz, SFDR Mode Enabled

TERMINOLOGY

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Analog Input Resistance, Differential Analog Input Capacitance, and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180° out of phase. Peak-to-peak differential voltage is computed by rotating the input phase 180° and taking the peak measurement again. The difference is then computed between both peak measurements.

Differential Nonlinearity (DNL)
The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
The effective number of bits (ENOB) is calculated from the measured SNR based on the following equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76\ \text{dB} + 20\ \log\left(\frac{Full-Scale\ Amplitude}{Input\ Amplitude}\right)}{6.02}$$

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the encode pulse should be left in the Logic 1 state to achieve the rated performance. Pulse width low is the minimum amount of time that the encode pulse should be left in the Logic 0 state. At a given clock rate, these specifications define an acceptable encode duty cycle.

Full-Scale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{FullScale} = 10\log\left(\frac{\frac{V^2 FullScale_{rms}}{Z}}{0.001}\right)$$

Gain Error
The difference between the measured and the ideal full-scale input voltage range of the ADC.

Harmonic Distortion
The ratio of the rms signal amplitude fundamental frequency to the rms signal amplitude of a single harmonic component (second, third, and so on); reported in dBc.

Integral Nonlinearity (INL)
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Maximum Conversion Rate
The maximum encode rate at which parametric testing is performed.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Noise (for Any Range within the ADC)
Noise can be calculated using the following equation:

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

where:
Z is the input impedance.
FS is the full scale of the device for the frequency in question.
SNR is the value for the particular input level.
Signal is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Output Propagation Delay
The delay between a differential crossing of ENCODE and $\overline{\text{ENCODE}}$ and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone (f_1, f_2) to the rms value of the worst third-order intermodulation product; reported in dBc. Products are located at $2f_1 - f_2$ and $2f_2 - f_1$.

Two-Tone SFDR
The ratio of the rms value of either input tone (f_1, f_2) to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second-order and third-order harmonic); reported in dBc.

EQUIVALENT CIRCUITS

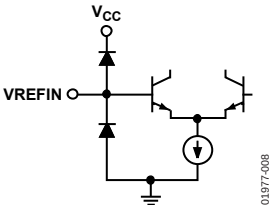

Figure 36. Voltage Reference Input Circuit

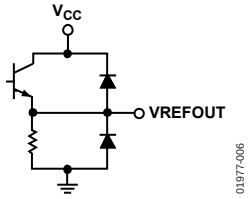

Figure 39. Voltage Reference Output Circuit

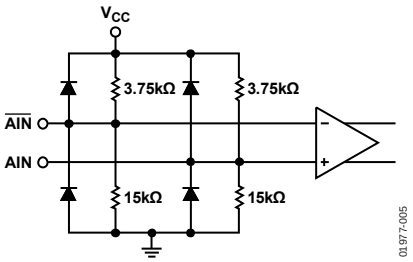

Figure 37. Analog Input Circuit

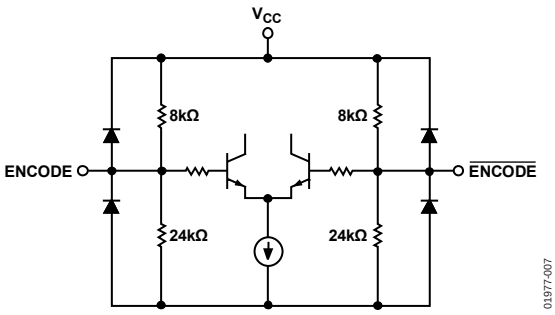

Figure 40. Encode Input Circuit

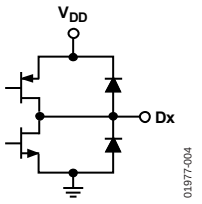

Figure 38. Digital Output Circuit

THEORY OF OPERATION

The AD9433 is a 12-bit pipeline converter that uses a switched-capacitor architecture. Optimized for high speed, this converter provides flat dynamic performance up to and beyond the Nyquist limit. DNL transitional errors are calibrated at final test to a typical accuracy of 0.25 LSB or less.

ENCODE INPUT

Any high speed ADC is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the ADC output. For this reason, considerable care has been taken in the design of the encode input of the AD9433, and the user is advised to give commensurate thought to the clock source.

The AD9433 has an internal clock duty cycle stabilization circuit that locks to the rising edge of ENCODE (falling edge of $\overline{\text{ENCODE}}$ if driven differentially) and optimizes timing internally. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter in the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. This circuit is always on and cannot be disabled by the user.

The ENCODE and $\overline{\text{ENCODE}}$ inputs are internally biased to 3.75 V (nominal) and support either differential or single-ended signals. For best dynamic performance, a differential signal is recommended. Good performance is obtained using an MC10EL16 translator in the circuit to directly drive the encode inputs (see Figure 41).

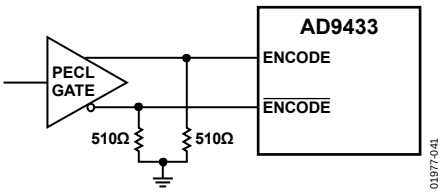

Figure 41. Using PECL to Drive the $\overline{\text{ENCODE}}$ Inputs

Often, the cleanest clock source is a crystal oscillator producing a pure, single-ended sine wave. In this configuration, or with any roughly symmetrical, single-ended clock source, the signal can be ac-coupled to the encode input. To minimize jitter, the signal amplitude should be maximized within the input range described in Table 7. The 12 kΩ resistors to ground at each of the inputs, in parallel with the internal bias resistors, set the common-mode voltage to approximately 2.5 V, allowing the maximum swing at the input. The $\overline{\text{ENCODE}}$ input should be bypassed with a capacitor to ground to reduce noise. This ensures that the internal bias voltage is centered on the encode signal. For best dynamic performance, impedances at ENCODE and $\overline{\text{ENCODE}}$ should match.

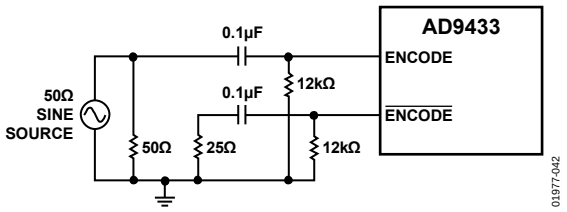

Figure 42. Single-Ended Sine Source Encode Circuit

Figure 43 shows another preferred method for clocking the AD9433. The clock source (low jitter) is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9433 to approximately 0.8 V p-p differential. This helps to prevent the large voltage swings of the clock from feeding through to other portions of the AD9433 and limits the noise presented to the encode inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically 100 Ω) is placed in series with the primary.

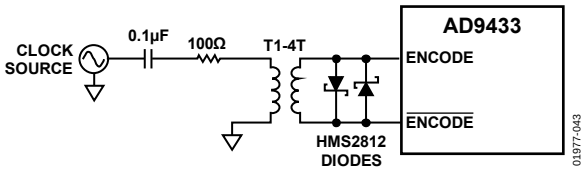

Figure 43. Transformer-Coupled Encode Circuit

ENCODE VOLTAGE LEVEL DEFINITION

The voltage level definitions for driving ENCODE and $\overline{\text{ENCODE}}$ in single-ended and differential mode are shown in Figure 44.

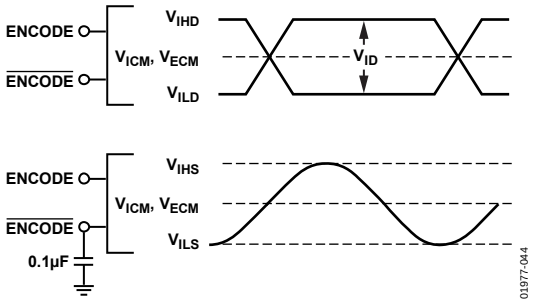

Figure 44. Differential and Single-Ended Input Levels

Table 7. Encode Inputs

Input	Min	Nominal	Max
Differential Signal Amplitude (V_{ID})	200 mV	750 mV	5.5 V
Input Voltage Range (V_{IHD}, V_{ILD}, V_{IHS}, V_{ILS})	−0.5 V		V_{CC} + 0.5 V
Internal Common-Mode Bias (V_{ICM})		3.75 V	
External Common-Mode Bias (V_{ECM})	2.0 V		4.25 V

ANALOG INPUT

The analog input to the AD9433 is a differential buffer. The input buffer is self-biased by an on-chip resistor divider that sets the dc common-mode voltage to a nominal 4 V (see the Equivalent Circuits section). Rated performance is achieved by driving the input differentially. The minimum input offset voltage is obtained when driving from a source with a low differential source impedance, such as a transformer in ac applications (see Figure 45). Capacitive coupling at the inputs increases the input offset voltage by as much as 50 mV.

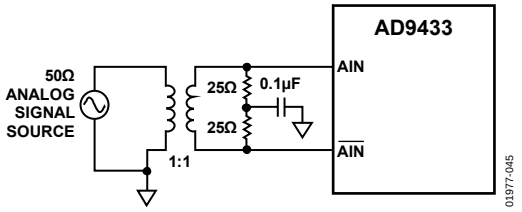

Figure 45. Transformer-Coupled Analog Input Circuit

In the highest frequency applications, two transformers connected in series may be necessary to minimize even-order harmonic distortion. The first transformer isolates and converts the signal to a differential signal, but the grounded input on the primary side degrades amplitude balance on the secondary winding. Capacitive coupling between the windings causes this imbalance. Because one input to the first transformer is grounded, there is little or no capacitive coupling, resulting in an amplitude mismatch at the output of the first transformer. A second transformer improves the amplitude balance, and thus improves the harmonic distortion. A wideband transformer, such as the ADT1-1WT from Mini-Circuits®, is recommended for these applications, because the bandwidth through the two transformers is reduced by √2.

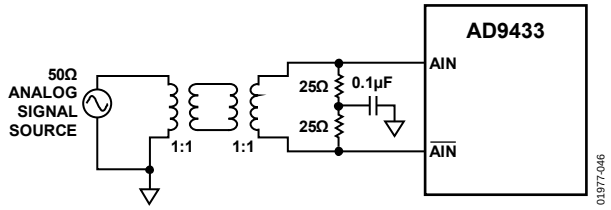

Figure 46. Driving the Analog Input with Two Transformers for Improved Even-Order Harmonics

Driving the ADC single-ended degrades performance, particularly even-order harmonics. For best dynamic performance, impedances at AIN and $\overline{\text{AIN}}$ should match. Special care was taken in the design of the analog input section of the AD9433 to prevent damage and corruption of data when the input is overdriven.

SFDR OPTIMIZATION

When set to Logic 1, the SFDR MODE pin enables a proprietary circuit that can improve the spurious-free dynamic range (SFDR) performance of the AD9433. This pin is useful in applications where the dynamic range of the system is limited by discrete spurious frequency content caused by nonlinearities in the ADC transfer function.

Enabling this circuit gives the circuit a dynamic transfer function, meaning that the voltage threshold between two adjacent output codes can change from clock cycle to clock cycle. While improving spurious frequency content, this dynamic aspect of the transfer function may be inappropriate for some time domain applications of the converter. Connecting the SFDR MODE pin to ground disables this function. The improvement in the linearity of the converter and its effect on spurious free dynamic range is shown in Figure 4 and Figure 5 and in Figure 22 and Figure 23.

DIGITAL OUTPUTS

The digital outputs are 3 V (2.7 V to 3.3 V) TTL-/CMOS-compatible for lower power consumption. The output data format is selectable through the data format select (DFS) CMOS input. DFS = 1 selects offset binary; DFS = 0 selects twos complement coding (see Table 8 and Table 9).

Table 8. Offset Binary Output Coding (DFS = 1, V_{REF} = 2.5 V)

Code	AIN – $\overline{\text{AIN}}$ (V)	Digital Output
4095	+1.000	1111 1111 1111
…	…	…
2048	0	1000 0000 0000
2047	−0.00049	0111 1111 1111
…	…	…
0	−1.000	0000 0000 0000

Table 9. Twos Complement Output Coding (DFS = 0, V_{REF} = 2.5 V)

Code	AIN – $\overline{\text{AIN}}$ (V)	Digital Output
+2047	+1.000	0111 1111 1111
…	…	…
0	0	0000 0000 0000
−1	−0.00049	1111 1111 1111
…	…	…
−2048	−1.000	1000 0000 0000

VOLTAGE REFERENCE

A stable and accurate 2.5 V voltage reference is built into the AD9433 (VREFOUT). In normal operation, the internal reference is used by strapping Pin 45 to Pin 46 and placing a 0.1 µF decoupling capacitor at VREFIN. The input range can be adjusted by varying the reference voltage applied to the AD9433. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly.

TIMING

The AD9433 provides latched data outputs, with 10 pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (see Figure 2). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9433; these transients can detract from the dynamic performance of the converter. The minimum guaranteed conversion rate of the AD9433 is 10 MSPS. At internal clock rates below 10 MSPS, dynamic performance may degrade.

APPLICATIONS INFORMATION

LAYOUT INFORMATION

A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device.

The pinout of the AD9433 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs and their supply and ground pin connections are segregated on one side of the package, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD9433 (V_{CC}, AIN, and VREF), minimal capacitive loading should be placed on these outputs.

It is recommended that a fanout of only one gate be used for all AD9433 digital outputs.

The layout of the encode circuit is equally critical and should be treated as an analog input. Any noise received on this circuitry results in corruption in the digitization process and lower overall performance. The encode clock must be isolated from the digital outputs and the analog inputs.

REPLACING THE AD9432 WITH THE AD9433

The AD9433 is pin-compatible with the AD9432, although there are two control pins on the AD9433 that are do not connect (DNC) and supply (V_{CC}) connections on the AD9432 (see Table 10).

Table 10. AD9432/AD9433 Pin Differences

Pin	AD9432	AD9433
41	DNC	DFS
42	V_{CC}	SFDR MODE

Using the AD9433 in an AD9432 pin assignment configures the AD9433 as follows:

- The SFDR improvement circuit is enabled.
- The DFS pin floats low, selecting twos complement coding for the digital outputs. (Twos complement coding is the only output coding available on the AD9432.)

Table 11 summarizes the differences between the AD9432 and AD9433 analog and encode input common-mode voltages. These inputs can be ac-coupled so that the devices can be used interchangeably.

Table 11. AD9432/AD9433 Analog and Encode Input Common-Mode Voltages

	Common-Mode Voltage	
Input Pins	**AD9432**	**AD9433**
ENCODE/$\overline{\text{ENCODE}}$	1.6 V	3.75 V
AIN/$\overline{\text{AIN}}$	3.0 V	4.0 V

OUTLINE DIMENSIONS

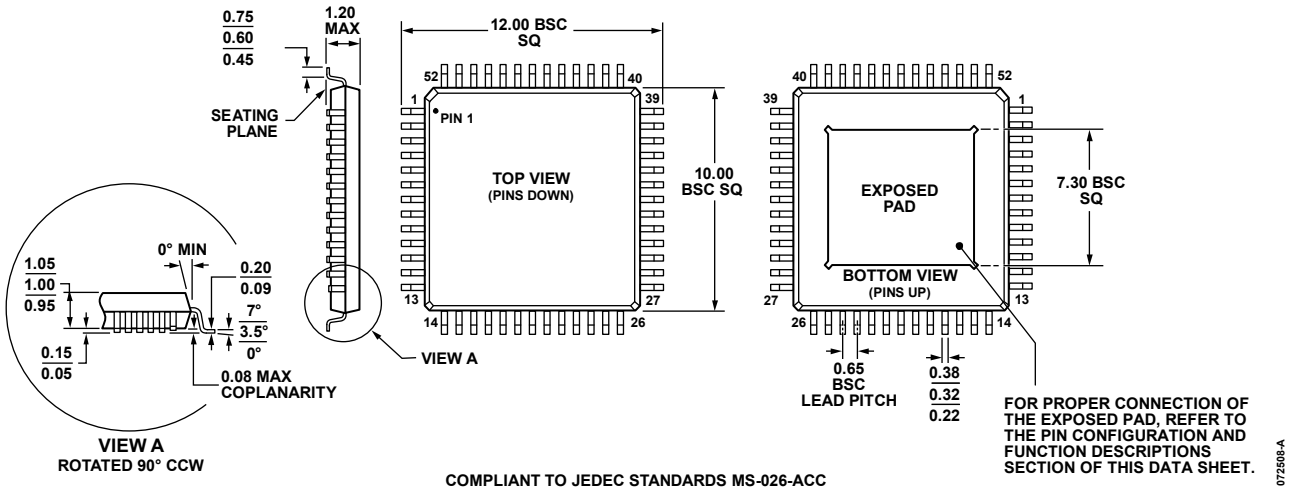

Figure 47. 52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-52-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9433BSVZ-105[1]	−40°C to +85°C	52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-52-2
AD9433BSVZ-125[1]	−40°C to +85°C	52-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-52-2

[1] Z = RoHS Compliant Part.

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